Intel® Arc™ A-Series Graphics and Intel Data Center GPU Flex Series

Open-Source Programmer's Reference Manual

For the discrete GPUs code named "Alchemist" and "Arctic Sound-M"

Volume 2c: Command Reference: Registers
Part 2 – Registers L through Z

March 2023, Revision 1.0

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L3 Allocation Control Register

L3ALLOCREG - L3 Allocation Control Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B134h
Name:	L3 Allocation Control Register
ShortName:	L3ALLOCREG
Address:	0B234h
ShortName:	L3ALLOCREG_CCS0

This register controls the allocation of various sections of the L3 cache

DWord	Bit	Description
0 L3CacheLayout: 2x2 array	31:25	**All L3 Client Pool** Access: R/W Number of ways allocated for the all client pool. This is a combined pool for all clients. **Programming Notes** When this field is non-zero, **DC Way Assignment** and **Read Only Client Pool** should be 0KB.
	24:18	**DC Way Assignment** Default Value: 0h Access: R/W Number of ways allocated for HDC. **Programming Notes** Note: This field must be 0KB if All L3 Client Pool is non-zero.
	17:11	**Read Only Client Pool** Default Value: 0h Access: R/W Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients. **Programming Notes** Note: This field must be 0KB if All L3 Client Pool is non-zero.
	10	**Reserved** Access: RO Format: MBZ

L3ALLOCREG - L3 Allocation Control Register

	9	**Reserved** Access: R/W
	8	**Reserved** Access: RO Format: MBZ
	7:1	**Reserved** Access: RO Format: MBZ
	0	**Allocation Error status** Access: RO This bit indicates a programming error in L3 allocation registers (L3ALLOCREG and L3TCCNTRLREG). 0 : Indicates no error in programming 1 : Indicates that the L3 allocation programming is incorrect.L3 will use the most recent valid allocation OR default programming.

L3 Cache Runtime ECC capture Register

L3_ECC_CAPTURE_REG - L3 Cache Runtime ECC capture Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B144h

This register shows the captured value of the ECC calculated by the internal logic for L3 writes.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**L3 Cache Latched ECC Value** Access: RO This field holds the value of the ECC generated by the L3 cache pipeline for the preceding write cycle.

L3 Cache Runtime ECC Test Control Register

L3_ECC_TEST_CTL - L3 Cache Runtime ECC Test Control Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B13Ch

This register is used to control the run time testing of the ECC logic in the L3 cache.

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21	**L3 ECC Latch Enable** Access: R/W This bit enables the latching of the ECC value generated for any write access made to the L3. The latched value of the ECC can be read from the "L3 Cache Runtime ECC capture Register". 0 – **[Default]** – Disable latching. 1 – Enable the latching
	20	**L3 ECC Override Enable** Access: R/W This bit enables the overriding of the ECC value generated for any write access made to the L3. The value in the field below will be used to override the ECC internally generated. 0 – **[Default]** – Disable override of the ECC value 1 – Enable the override of the ECC value
	19:0	**L3 ECC Override Value** Default Value: 00h Access: R/W This is the value to be used as the override for the ECC when enabled in the bit field above.

L3 Control Register

L3CNTLREG - L3 Control Register		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	07034h	
Name:	L3 Control Register	
ShortName:	L3CNTLREG	

DWord	Bit	Description
0	31:0	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

L3 Fault Register

L3FLTREG - L3 Fault Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B190h	

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:1	**Page Fault Full Client ID** Access: RO
	0	**Page Fault has Occurred** Access: RO This field indicates that a page fault has occurred, and that the full client ID found in bits [19:1] is valid.

L3 Flush Range Register

L3FLUSHRANGE - L3 Flush Range Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B174h

DWord	Bit	Description
0	31:12	**Address Low** Access: R/W Format: GraphicsAddress[31:12]
	11:9	**Reserved** Access: RO Format: MBZ
	8:3	**Address Mask** Access: R/W AM - Address Mask: The value in this field specifies the number of low order bits of the ADDR field that must be masked for the invalidation operation. This field enables software to request invalidation. Mask Value / Address Bits Masked / Pages Invalidated 0 / None / 1 1 / 12 / 2 2 / 13:12 / 4 3 / 14:12 / 8 4 / 15:12 / 16 ... / ... / ...
	2:0	**Reserved** Access: RO Format: MBZ

L3 Flush Range Register 2

L3FLUSHRANGE2 - L3 Flush Range Register 2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B178h

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:28	**L3 Flush Eviction Policy** Access: R/W This field describes the flush eviction policy for the address ranges being flushed

Value	Name	Description
0h	Flush L3 with eviction - INV **[Default]**	All modified content written to memory and L3 state is invalid
1h	Flush L3 with eviction - VLD	All modified content written to memory and L3 state is kept valid (shared state)
2h	Discard	All modified content is discarded (no write out to memory) and L3 state is invalid

DWord	Bit	Description
	27:16	**Reserved** Access: RO Format: MBZ
	15:0	**Address Upper** Access: R/W Format: GraphicsAddress[47:32]

L3 Multi Context Reserved1

L3RCS0RSVD1 - L3 Multi Context Reserved1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B168h	
ShortName:	L3RCS0RSVD1	
Address:	0B268h	
ShortName:	L3CCS0RSVD1	
DWord	**Bit**	**Description**
0	31:0	**SCRATCH** Access: R/W

L3 Multi Context Reserved2

L3 Multi Context Reserved2			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
_Custom_GTIReset:	DEV		
Address:	0B16Ch		
ShortName:	L3RCS0RSVD2		
Address:	0B26Ch		
ShortName:	L3CCS0RSVD2		
DWord	**Bit**	**Description**	
0	31:0	**SCRATCH**	
		Access:	R/W

L3Node arbiter config register

L3NODEARBCFG - L3Node arbiter config register

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 0B0B4h

L3Node arbiter configuration register

DWord	Bit	Description
0	31:28	**Reserved**
	27:25	**LNE cross read return weight** Access: R/W _Custom_GTIReset: DEV **Description**: Arbiter weight for LNE cross node read return **Value** 5 — **Name** **[Default]**
	24:22	**LNE cross eviction weight** Access: R/W _Custom_GTIReset: DEV **Description**: Arbiter weight for LNE cross node eviction **Value** 1 — **Name** **[Default]**
	21:18	**Reserved**
	17:16	**SQ hash selection control** Access: R/W _Custom_GTIReset: DEV 10: ADDR[7] 10: ADDR[7] 01: ADDR[7] 00: ^ADDR[47:9]^ADDR[7] Incf_cfg_lnib_sq_bankhash.
	15:12	**Reserved**
	11:8	**Reserved**

L3NODEARBCFG - L3Node arbiter config register

7:6 **LNIB B2B grant for preserving locality**

Access:	R/W
_Custom_GTIReset:	DEV

00: 1 grant.
01: 2 b2b grants
10: 3 b2b grants
11: Not supported
Incf_lnic_b2b_gnt.

5:4 **LSN B2B grant for preserving locality**

Access:	R/W
_Custom_GTIReset:	DEV

00: 1 grant.
01: 2 b2b grants
10: 3 b2b grants
11: Not supported
Incf_lsn_b2b_gnt.

3:2 **LNE miss and eviction B2B grant for preserving locality**

Access:	R/W
_Custom_GTIReset:	DEV

Incf_lne_arb_pri.

Value	Name	Description
0h	**[Default]**	1 grant
1h		2 b2b grant
2h		3 b2b grant
3h		4 b2b grant

1:0 **LNIC B2B grant for preserving locality**

Access:	R/W
_Custom_GTIReset:	DEV

00: 1 grant.
01: 2 b2b grants
10: 3 b2b grants
11: Not supported
Incf_lnic_b2b_gnt.

L3 Node Units Idle Status

L3_NODE_IDLE - L3 Node Units Idle Status

Register Space:	MMIO: 0/2/0
Access:	RO Variant
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B0B0h

Status register for l3 node units idle indication. Value 1 means idle

DWord	Bit	Description
0	31:10	**Reserved** Access: RO Format: MBZ
	9	**IDLE_CBE** Access: RO Variant
	8	**IDLE_LSN5** Access: RO Variant
	7	**IDLE_LSN4** Access: RO Variant
	6	**IDLE_LSN3** Access: RO Variant
	5	**IDLE_LSN2** Access: RO Variant
	4	**IDLE_LSN1** Access: RO Variant
	3	**IDLE_LSN0** Access: RO Variant
	2	**IDLE_LNIC** Access: RO Variant
	1	**IDLE_LNIB** Access: RO Variant
	0	**IDLE_LNE** Access: RO Variant

L3 Parameter Information Register

L3PARAMINFO - L3 Parameter Information Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B164h

Programming Notes

GT_L3_NUM_WAYS gives total number of ways for one L3 bank. Storage per way can be calculated as Total Storage per L3 bank / GT_L3_NUM_WAYS. L3ALLOCREG and L3TCCNTLREG can be programmed appropriately using storage/way information.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**Reserved** Access: RO Format: MBZ
	7:0	**GT_L3_NUM_WAYS** Access: RO This field indicates number of tagged ways in L3 bank which is maximum number of ways that can be allocated for cachable data.

L3 SQC register 4

L3SQCREG4 - L3 SQC register 4		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B118h	
Address:	0B218h	
ShortName:	L3SQCREG4_CCS0	
DWord	**Bit**	**Description**
0	31:21	**Reserved** Access: RO Format: MBZ
	20:7	**Reserved** Access: RO Format: MBZ
	6	**Placeholder** Access: RO
	5:0	**Reserved** Access: RO Format: MBZ

L3 SQC register 5

L3SQCREG5 - L3 SQC register 5		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B158h	
Address:	0B258h	
ShortName:	L3SQCREG5_CCS0	

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23	**Cross-Tile Partial Write Merge Enable** Default Value: 1 Access: R/W Format: enable Enables partial write merge optimization for cross-tile surfaces.
	22	**Coherent Partial Write Merge Enable** Default Value: 1 Access: R/W Format: Enable _Custom_GTIReset: DEV Enables partial write merge optimization for coherent surfaces.
	21	**Compressible Partial Write Merge Enable** Default Value: 1 Access: R/W Format: Enable _Custom_GTIReset: DEV Enables partial write merge optimization for compressible surfaces.
	20	**Reserved** Access: RO Format: MBZ
	19:10	**Reserved** Access: RO Format: MBZ

L3SQCREG5 - L3 SQC register 5		
	9:0	**L3 cache partial Write merge timer initial value** Default Value: 1FFh Default Access: R/W If partial write merging is enabled, this timer controls the window to allow partial writes to merge together. The value is first loaded when an eligible request arrives, and is reloaded every time another partial write is collapsed in to the parent **Programming Notes** The value of this register must be nonzero if any partial write merging is enabled, consisting of the CZ + L3 Partial Write Merge Enables in TCCNTLREG*, and the Coherent + Compressible Partial Write Merge Enables in LSCREG5*

L3 SQC register 6

L3SQCREG6 - L3 SQC register 6		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B15Ch	
Address:	0B25Ch	
ShortName:	L3SQCREG6_CCS0	

DWord	Bit	Description
0	31:14	**Reserved** Access: RO Format: MBZ
	13:7	**Maximum number of partial write chains** Access: R/W Value: 8h — **[Default]** Value: [4h-20h]
	6:0	**Maximum number of slots that can wait for timer to expire** Access: R/W Value: 10h — **[Default]** Value: [4h,20h]

L3 SQC register 7

L3SQCREG7 - L3 SQC register 7

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B188h

L3 register for LSQC config bits

DWord	Bit	Description
0	31:6	**Reserved** Access: RO Format: MBZ
	5	**Reserved** Access: RO Format: MBZ
	4	**Compressed Data Fill Discard Fix Disable** Default Value: 0 Access: R/W Format: Disable
	3	**Blend Fill Caching Optimization Disable** Default Value: 0 Access: R/W Format: Disable Disable special treatment for compressible cases where intent to modify is expressed. This potentially results in additional cachelines being filled in to L3.
	2	**Convert GA Ctype Disable** Access: R/W Format: Disable Value / Name / Description: 1 — All the converted GA * CTYPES (GT_GT_GA_memRd/wr/Atm) will be treated as Legacy Cytpes with L3 look up bypass. 0 **[Default]** — All the converted GA* CTYPEs (GT_GA_memRd/wr/Atm Ctypes) can be converted to L3 bound Ctypes.

L3SQCREG7 - L3 SQC register 7

1 — Convert GA Force Uncacheable Enable

Access:	R/W
Format:	Enable

Value	Name	Description
1		Converted GA* CTYPEs will be forced as global GO, uncacheable, and lookup enabled
0	**[Default]**	The cycles will follow that specified by MOCS.

0 — Force L3 Uncacheable Lookup Enable

Access:	R/W
Format:	Enable

Value	Name	Description
1		LSQC will do the Look up for all UC L3 bound Ctypes.
0	**[Default]**	Look up enable values from MOCS will be used as is.

L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B100h
Address:	0B200h
ShortName:	L3SQCREG1_CCS0

Programming Notes

Workaround - Credits between LNI/LSQC are not updated in case of Render DOP gating condition)- DOP Render clock ungating needs to happen before L3SQCREG1 is programmed and it should happen through the driver.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:17	**L3SQ General Priority Credit Initialization** Access: R/W **Description** Number of general priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. The number of general priority credits is equal to double the value written in this register. Example: [00001b = 2 credits; 00100b = 8 credits] The number of general priority credits is always greater than that of high priority credits. This implies that the sum of the programmed general priority and high priority values should be less than or equal to total slot credits Signal name: lbcf_csr_lsqc_gen_credit_init **Value** / **Name** 0100000b / **[Default]** [2h,20h] / **Programming Notes** The number of general priority credits is always greater than that of high priority credits. Total number of general and high priority credits should be less than or equal to total slot credits. This implies that the sum of the programmed general priority and high priority values should be less than or equal to lbcf_csr_lsqc_gen_credit_init + lbcf_csr_lsqc_hp_credit_init

L3SQCREG1 - L3 SQC registers 1

16:11 L3SQ High Priority Credit Initialization

Access:	R/W

Number of high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots.
The number of high priority credits is equal to double the value written in this register. Example: [00001b = 2 credits; 00100b = 8 credits]
The number of high priority credits is always lesser than that of general priority credits. This implies that the sum of the programmed general priority and high priority values should be less than or equal to total slot credits
Valid values for high priority credits can range from: [0 to 15]. Other values are reserved
Signal name: lbcf_csr_lsqc_gen_credit_init

Value	Name
000000b	**[Default]**

Programming Notes
The number of high priority credits is always lesser than that of general priority credits. Total number of general and high priority credits should be less than total slot credits. This implies that the sum of the programmed general priority and high priority values should be less than or equal to lbcf_csr_lsqc_gen_credit_init + lbcf_csr_lsqc_hp_credit_init

10 Reserved

Access:	RO
Format:	MBZ

9 Reserved

Access:	RO
Format:	MBZ

8 Error Detection Behavior Control

Access:	R/W

The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements. Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.

Value	Name	Description
0	**[Default]**	RTL does not hang on parity errors or double bit error
1		RTL enforces a hang on parity errors or double bit error

7 Reserved

Access:	RO
Format:	MBZ

L3SQCREG1 - L3 SQC registers 1

	6	**Reserved** Access: RO Format: MBZ
	5	**Flush all non coherent lines** Access: R/W **Description** The L3 will support destination based flushing for the unified sections of the cache. i.e., if we get a DC flush, even if we have a unified cache, only the lines brought in by DC will be flushed. Similarly, tile cache flushes only clean out lines brought in by the C/Z clients into the unified section. However, in order to provide a mechanism to allow for a single pass flush to clean out the entire R/W section of the cache, this mode is implemented. When a pipeline flush or a tile cache flush is received and if this bit is set, then all the modified non-coherent lines irrespective of DC/C/Z in the unified cache section will be flushed. Also, all the Shared lines in the unified cache section will be downgraded to invalid for all Non- Coherent lines. This bit will have no impact when DC and tile cache are in separate sections. Also note that this bit will not initiate the invalidation of RO lines in the cache. That is only controlled by the RO invalidation commands sent to the L3 on a per context basis. **Value** / **Name** / **Description** 0 / **[Default]** / By default, the full flush mode will be disabled.
	4:0	**Reserved** Access: RO Format: MBZ

L3 Unslice IDLE Status Register

L3_UNSL_IDLE - L3 Unslice IDLE Status Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B414h	
DWord	**Bit**	**Description**
0	31:2	**Reserved** Access: RO Format: MBZ
	1	**LSN Endpoint Unit IDLE Indication** Access: RO Variant LSN Endpoint Unit IDLE. This bit is not used and assigned to zero.
	0	**LTISEQunit Unit IDLE Indication** Access: RO Variant LTISEQunit IDLE

LANEN_DIG_TX_LBERT_CTL

LANEN_DIG_TX_LBERT_CTL

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

PHY link quality transmission test pattern control register.
This register is not accessed through regular MMIO. Refer to Display Transcoder DP2 section, DP2.0 Link Quality Checks sub-section for programming instructions.
There are instances of this register for each PHY and each lane and a broadcast write access to all lanes of each PHY.
Bit width is documented as 32 because of tool restrictions. Actual width is 16.

DWord	Bit	Description
0	31:15	**Reserved** Access: RO Format: MBZ
	14:5	**PAT0** Access: R/W Pattern for fixed pattern mode
	4	**Reserved** Access: RO Format: MBZ
	3:0	**Mode** Access: R/W

Value	Name	Description
0h	Disabled	Normal display output
1h	PRBS31	
2h	PRBS23	
3h	PRBS23 alternate	
4h	PRBS16	
5h	PRBS15	
6h	PRBS11	
7h	PRBS9	
8h	PRBS7	
9h	PAT0	
Ah	DC balanced PAT0	PAT0, ~PAT0
Bh	Fixed Pattern	Ten 0s, PAT0, ten 1s, ~PAT0

LBCF flush request

LBCFFLSHREQ - LBCF flush request

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B17Ch

This register is used by the LTI Sequencer to initiate flush flows in the L3 banks

DWord	Bit	Description
0	31:23	**Reserved** Access: RO Format: MBZ
	22:16	**Reserved** Access: RO Format: MBZ
	15:11	**Reserved** Access: RO Format: MBZ
	10	**GroupID Indication** Access: R/W Indicates whether the ID programmed in [9:5] is a GroupID or an EngineID 0 **[Default]** The ID programmed in [9:5] is an EngineID 1 The ID programmed in [9:5] is a GroupID
	9:5	**ID** Access: R/W This field either reflects the EngineID or GroupID, based on how the is_gid bit [10] is programmed. In Render Engine Reset case bit 10 will be set and a value of 00000 will indicate {RCS+CCS}
	4:0	**Flush Type** Access: R/W 0h : GT_L3_RW_FLSH : This is on per context basis and flushes non coherent DC lines. This is sent by global flush sequencer. 1h : GT_L3_TILE_FLSH : This is valid only for render context and global flush sequencer will send the request to L3

LBCFFLSHREQ - LBCF flush request				
		2h		GT_L3_GLBL_FLSH : This will flush all modified as well as RO lines of all context.
		3h		GT_L3_PM_FLSH : This will flush all the lines ignoring the context and will be sent by PM.
		4h		GT_L3_TXT_INV : This invalidates texture lines of a particular context.
		5h		GT_L3_INST_INV : This invalidates state and instruction lines of a particular context.
		6h		GT_L3_CNST_INV : This invalidates constant lines of a particular context.
		7h		GT_L3_ST_INV : This invalidates state and instruction lines of a particular context and also invalidates SARB
		8h		GT_L3_CSCB_INV : This invalidates CS command buffer for render context.
		9h		GT_L3_GEO_CACHE_INV : This invalidates vertex buffer for render context.
		Ah		GT_L3_FABRIC_FLSH : Fabric flush checks completion counter at bank and CCunit It is engine specific
		Bh		GT_L3_BANK_PMUNBLK : This will unblock LBI, PM will send this after the completion of PM flush.
		Ch		GT_L3_RO_INV :LTISEQ will send RO invalidation for any read only invalidation if any of the tex, constant, state, instruction invalidation enabled. This is per context.
		Dh		GT_L3_DISCARD_FLSH
		Eh		GT_L3_RANGE_FLSH

LBCF-LTISEQ Flush Done Message 0

LBCF_LTISEQ_FLUSH_DONE0 - LBCF-LTISEQ Flush Done Message 0

Register Space:	MMIO: 0/2/0
Access:	R/W Hardware Clear
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B494h

DWord	Bit	Description
0	31:16	**Mask** Access: R/W
	15	**BANK15 Flush Done** Access: R/W Hardware Clear
	14	**BANK14 Flush Done** Access: R/W Hardware Clear
	13	**BANK13 Flush Done** Access: R/W Hardware Clear
	12	**BANK12 Flush Done** Access: R/W Hardware Clear
	11	**BANK11 Flush Done** Access: R/W Hardware Clear
	10	**BANK10 Flush Done** Access: R/W Hardware Clear
	9	**BANK9 Flush Done** Access: R/W Hardware Clear
	8	**BANK8 Flush Done** Access: R/W Hardware Clear
	7	**BANK7 Flush Done** Access: R/W Hardware Clear
	6	**BANK6 Flush Done** Access: R/W Hardware Clear
	5	**BANK5 Flush Done** Access: R/W Hardware Clear
	4	**BANK4 Flush Done** Access: R/W Hardware Clear
	3	**BANK3 Flush Done** Access: R/W Hardware Clear

LBCF_LTISEQ_FLUSH_DONE0 - LBCF-LTISEQ Flush Done Message 0

	2	**BANK2 Flush Done** Access: R/W Hardware Clear
	1	**BANK1 Flush Done** Access: R/W Hardware Clear
	0	**BANK0 Flush Done** Access: R/W Hardware Clear

LBCF-LTISEQ Flush Done Message 1

LBCF_LTISEQ_FLUSH_DONE1 - LBCF-LTISEQ Flush Done Message 1	
Register Space:	MMIO: 0/2/0
Access:	R/W Hardware Clear
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B498h

DWord	Bit	Description
0	31:16	**Mask** Access: R/W
	15	**BANK31 Flush Done** Access: R/W Hardware Clear
	14	**BANK30 Flush Done** Access: R/W Hardware Clear
	13	**BANK29 Flush Done** Access: R/W Hardware Clear
	12	**BANK28 Flush Done** Access: R/W Hardware Clear
	11	**BANK27 Flush Done** Access: R/W Hardware Clear
	10	**BANK26 Flush Done** Access: R/W Hardware Clear
	9	**BANK25 Flush Done** Access: R/W Hardware Clear
	8	**BANK24 Flush Done** Access: R/W Hardware Clear
	7	**BANK23 Flush Done** Access: R/W Hardware Clear
	6	**BANK22 Flush Done** Access: R/W Hardware Clear
	5	**BANK21 Flush Done** Access: R/W Hardware Clear
	4	**BANK20 Flush Done** Access: R/W Hardware Clear
	3	**BANK19 Flush Done** Access: R/W Hardware Clear

LBCF_LTISEQ_FLUSH_DONE1 - LBCF-LTISEQ Flush Done Message 1		
	2	**BANK18 Flush Done** Access: R/W Hardware Clear
	1	**BANK17 Flush Done** Access: R/W Hardware Clear
	0	**BANK16 Flush Done** Access: R/W Hardware Clear

LBCF Render config save msg

LBCFRCSR - LBCF Render config save msg

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B3FCh

This register is not context saved and is written by CS unit

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16	**Render Context Save Request Mask** Access: R/W Hardware Clear Value / Name / Description 0 / default **[Default]** / Render context save request is ignored, and LBCFRCSR[0] is invalid. 1 / / LBCFRCSR[0] is valid.
	15:1	**Reserved** Access: RO Format: MBZ
	0	**Render Context save Request** Access: R/W Hardware Clear Value / Name / Description 0 / default **[Default]** / Render context save is not being requested. 1 / / Render context save is being requested. This bit is self-cleared upon sampling.

Link Capabilities

LINKCAP_0_2_0_PCI - Link Capabilities

Register Space: PCI: 0/2/0
Size (in bits): 32

Address: 0007Ch

This register provides information on the PCIe link capabilities.

DWord	Bit	Description
0	31:24	**Port Number** Default Value: 00h Access: RO _Custom_GTIReset: BUS PCIe port number for the given PCIe link.
	23	**Reserved** Access: RO Format: MBZ
	22	**ASPM Optionality Compliance** Default Value: 1b Access: RO _Custom_GTIReset: BUS This bit must be set to 1b in all Functions. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests
	21	**Link Bandwidth Notification Cap** Default Value: 0b Access: RO _Custom_GTIReset: BUS This field is reserved for PCIe endpoints.
	20	**Link Active Report Cap** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit must be 1b if component supports optional cap of reported DL_Active state.

LINKCAP_0_2_0_PCI - Link Capabilities

19	**Surprise Down Report Cap**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Set if optional capability of detecting and reporting a surprise down error condition.

18	**Clock PM**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

This bit must be hardwired to 0b.

17:15	**L1 Exit Latency**

Default Value:	000b
Access:	RO
_Custom_GTIReset:	BUS

This field indicates the L1 exit latency of the given PCIe link. The value reported indicates the length of time this port required to complete transition from ASPM L1 to L0. 000b=less than 1us.

14:12	**L0s Exit Latency**

Default Value:	000b
Access:	RO
_Custom_GTIReset:	BUS

This field indicates the L0s exit latency for the given PCIe link. The value reported indicates the length of time this port requires to complete transition from L0s to L0. 000b=less than 64ns.

11:10	**Active State PM**

Default Value:	11b
Access:	RO
_Custom_GTIReset:	BUS

This field indicates the level of ASPM supported on the given PCIe Link. Hardwired to 11 to indicate L0s and L1 supported.

9:4	**Max Link Width**

Default Value:	000001b
Access:	RO
_Custom_GTIReset:	BUS

Maximum Link Width Per IOSF spec recommendation, report x1. Encoding is 00 0001b (x1 width).

<table>
<tr><th colspan="3">LINKCAP_0_2_0_PCI - Link Capabilities</th></tr>
<tr><td></td><td>3:0</td><td>Max LInk Speed
<table>
<tr><td>Default Value:</td><td>0001b</td></tr>
<tr><td>Access:</td><td>RO</td></tr>
<tr><td>_Custom_GTIReset:</td><td>BUS</td></tr>
</table>
Max Link Speed Per IOSF Spec, report Gen1. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. The encoding is 0001b.</td></tr>
</table>

Link Capabilities 2

LINKCAP2_0_2_0_PCI - Link Capabilities 2		
Register Space:	PCI: 0/2/0	
Size (in bits):	32	
Address:	0009Ch	
This register provides information on the link capabilities 2 register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Format: MBZ
	7:1	**Supported Link Speed Vector** Default Value: 000001b 2_5GTs Access: RO _Custom_GTIReset: BUS This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. See Section 8.2.1 for further requirements. Bit definitions within this field are: Bit 0: 2.5 GT/s Bit 1: 5.0 GT/s Bit 2: 8.0 GT/s Bit 3: 16.0 GT/s Bits 6:4: RsvdP Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions
	0	**Reserved** Access: RO Format: MBZ

Link Control and Status

LINKCTRLSTS_0_2_0_PCI - Link Control and Status

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00080h

This register provides information on the PCIe link control and status.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:20	**Negotiated Link Width** Default Value: 000001b Access: RO _Custom_GTIReset: BUS Report x1 width only.
	19:16	**Current Link Speed** Default Value: 0001b Access: RO _Custom_GTIReset: BUS Report Gen1 speed only.
	15:8	**Link Active Report Cap** Default Value: 00h Access: RO _Custom_GTIReset: BUS Reserved
	7	**Reserved**
	7	**Reserved**
	6	**Reserved**
	6	**Reserved**
	5	**Retrain Link** Default Value: 0b

LINKCTRLSTS_0_2_0_PCI - Link Control and Status

		Access: RO _Custom_GTIReset: BUS Reserved
	4	**Link Disable** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit is reserved on endpoints.
	3	**Reserved**
	3	**Reserved**
	2	**Reserved** Access: RO Format: MBZ
	1:0	**Reserved**
	1:0	**Reserved**

LINKM

LINKM	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60040h-60043h
Name:	Transcoder Link M Value 1
ShortName:	TRANS_LINKM1_A
Reset:	soft
Address:	61040h-61043h
Name:	Transcoder Link M Value 1
ShortName:	TRANS_LINKM1_B
Reset:	soft
Address:	62040h-62043h
Name:	Transcoder Link M Value 1
ShortName:	TRANS_LINKM1_C
Reset:	soft
Address:	63040h-63043h
Name:	Transcoder Link M Value 1
ShortName:	TRANS_LINKM1_D
Reset:	soft

Description

This register is double buffered to update on the next MSA after LINKN is written.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**Link M value** Access: R/W This field is the link M value for external transmission in the Main Stream Attributes.

LINKN

LINKN	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60044h-60047h
Name:	Transcoder Link N Value 1
ShortName:	TRANS_LINKN1_A
Reset:	soft
Address:	61044h-61047h
Name:	Transcoder Link N Value 1
ShortName:	TRANS_LINKN1_B
Reset:	soft
Address:	62044h-62047h
Name:	Transcoder Link N Value 1
ShortName:	TRANS_LINKN1_C
Reset:	soft
Address:	63044h-63047h
Name:	Transcoder Link N Value 1
ShortName:	TRANS_LINKN1_D
Reset:	soft

Description

This register is double buffered to update on the next MSA after written. **Writes to this register arm M/N registers for this transcoder.**

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**Link N value** Access: R/W This field is the link N value for external transmission in the Main Stream Attributes and VB-ID.

LM_CTRL

LM_CTRL

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	68300h-68303h
Name:	Luminance Mapping Control
ShortName:	LM_CTRL_1_A
Reset:	soft
Address:	68B00h-68B03h
Name:	Luminance Mapping Control
ShortName:	LM_CTRL_1_B
Reset:	soft
Address:	69300h-69303h
Name:	Luminance Mapping Control
ShortName:	LM_CTRL_1_C
Reset:	soft
Address:	69B00h-69B03h
Name:	Luminance Mapping Control
ShortName:	LM_CTRL_1_D
Reset:	soft

This register controls the enhanced tone/luminance mapping LUT component. The LUT is a shared resource within each Pipe that can be bound to any of the HDR Planes.

DWord	Bit	Description
0	31	**Luminance Mapper Enable** Access: Double Buffered This will enable the tone/luminance mapper LUT component. 0b: Disabled 1b: Enabled
	30:2	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">LM_CTRL</th></tr>
<tr><td></td><td>1:0</td><td>Plane Binding
<table>
<tr><td>Access:</td><td>Double Buffered</td></tr>
</table>
This field controls which HDR Plane the tone mapping LUT is bound to.
This field is ignored if the LUT is not enabled.
<table>
<tr><th>Value</th><th>Name</th></tr>
<tr><td>00b</td><td>Plane 1</td></tr>
<tr><td>01b</td><td>Plane 2</td></tr>
<tr><td>10b</td><td>Plane 3</td></tr>
<tr><td>11b</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

LM_LUMA_COEFF

LM_LUMA_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	6830Ch-6830Fh
Name:	Luminance Mapping Coefficients
ShortName:	LM_LUMA_COEFF_1_A
Reset:	soft
Address:	68B0Ch-68B0Fh
Name:	Luminance Mapping Coefficients
ShortName:	LM_LUMA_COEFF_1_B
Reset:	soft
Address:	6930Ch-6930Fh
Name:	Luminance Mapping Coefficients
ShortName:	LM_LUMA_COEFF_1_C
Reset:	soft
Address:	69B0Ch-69B0Fh
Name:	Luminance Mapping Coefficients
ShortName:	LM_LUMA_COEFF_1_D
Reset:	soft

This register contains the coefficients to calculate the luminance of incoming pixels which is used to address into the tone-mapping LUT. The pixel luminance is calculated using the following formula:
luma = (Kr * red) + (Kg * green) + (Kb * blue)
All coefficients have a precision of 0.9. Multiply the desired coefficient by 2^9 to get programming value

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:20	**Red Coefficient** Access: Double Buffered This field contains the red coefficient (Kr) Value: 87h — Name: **[Default]** — Description: 0.2627
	19	**Reserved** Access: RO Format: MBZ

LM_LUMA_COEFF

	18:10	**Green Coefficient** Access: Double Buffered This field contains the green coefficient (Kg) Value / Name / Description: 15bh / **[Default]** / 0.6780
	9	**Reserved** Access: RO Format: MBZ
	8:0	**Blue Coefficient** Access: Double Buffered This field contains the blue coefficient (Kb) Value / Name / Description: 1eh / **[Default]** / 0.0593

LM_TONEFACT_DATA

LM_TONEFACT_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	68308h-6830Bh
Name:	Luminance Mapping Tone Factor Data
ShortName:	LM_TONEFACT_DATA_1_A
Reset:	soft
Address:	68B08h-68B0Bh
Name:	Luminance Mapping Tone Factor Data
ShortName:	LM_TONEFACT_DATA_1_B
Reset:	soft
Address:	69308h-6930Bh
Name:	Luminance Mapping Tone Factor Data
ShortName:	LM_TONEFACT_DATA_1_C
Reset:	soft
Address:	69B08h-69B0Bh
Name:	Luminance Mapping Tone Factor Data
ShortName:	LM_TONEFACT_DATA_1_D
Reset:	soft

This register is used to access the tone-map factors within the luminance mapper's LUT.
The Index Value from the LM_TONEFACT_INDEX register is the address into the LUT.
The contents of the table are uninitialized until Software loads it (i.e. the table is not resettable). Use of the table before Software has initialized it will result in non-deterministic behavior
See **Luminance Mapping LUT** page for more details (i.e. number of LUT entries)

Programming Notes

Even though this register is not double buffered, the LUT itself is double buffered on the rising edge of V. Blank.

Restriction

This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ

LM_TONEFACT_DATA		
	23:0	**Tone Mapping Factor** Access: R/W This is the tone-map factor to write to or read from the LUT. Precision of the data within the LUT is 8.16

LM_TONEFACT_INDEX

LM_TONEFACT_INDEX	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	68304h-68307h
Name:	Luminance Mapping Tone Factor Index
ShortName:	LM_TONEFACT_INDEX_1_A
Reset:	soft
Address:	68B04h-68B07h
Name:	Luminance Mapping Tone Factor Index
ShortName:	LM_TONEFACT_INDEX_1_B
Reset:	soft
Address:	69304h-69307h
Name:	Luminance Mapping Tone Factor Index
ShortName:	LM_TONEFACT_INDEX_1_C
Reset:	soft
Address:	69B04h-69B07h
Name:	Luminance Mapping Tone Factor Index
ShortName:	LM_TONEFACT_INDEX_1_D
Reset:	soft

This register controls the index into the tone/luminance mapping LUT for software updates/status of the tone factors

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ

LM_TONEFACT_INDEX

	16	**Index Auto Increment** Access: R/W This field enables the index into the LUT to auto increment for every write or read to the LM_TONEFACT_DATA register

Value	Name	Description
0b	No Increment	HW does not automatically increment index value
1b	Auto Increment	HW increments the index value with each read or write to the data register

Programming Notes

1. When auto increment is enabled, then hardware will:
   a. Increment from the current Index Value specified within this register for each read/write to the data register
   b. Automatically roll-over the Index Value to zero after it reaches the end of the table
2. If auto increment is not enabled, then it is Software's responsibility to:
   a. Update the Index Value for every access to the LUT
   b. Ensure the Index Value is within the valid range of the table (aliasing will occur if an Index Value is outside of the table's depth)

	15:8	**Reserved** Access: RO Format: MBZ
	7:0	**Index Value** Access: R/W This field controls the index into the luminance mapper's LUT.

Value	Name
[0,170]	

LNCF MOCS Register 0

LNCFCMOCS0 - LNCF MOCS Register 0

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B020h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global Go** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS0 - LNCF MOCS Register 0

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	10 ^ 16
1	11 ^ 17
2	12 ^ 18

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS0 - LNCF MOCS Register 0

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global Go

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS0 - LNCF MOCS Register 0

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 10 ^ 16 1 / 11 ^ 17 2 / 12 ^18
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 1

LNCFCMOCS1 - LNCF MOCS Register 1

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B024h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global Go** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS1 - LNCF MOCS Register 1

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	10 ^ 16
1	11 ^ 17
2	12 ^ 18

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS1 - LNCF MOCS Register 1

	7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
	6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 1 – LOWER_GOMemory **[Default]**
	5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS1 - LNCF MOCS Register 1

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 — 10 ^ 16 1 — 11 ^ 17 2 — 12 ^ 18
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h — LOWER_ESC_DISABLE 1h — LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 2

LNCFCMOCS2 - LNCF MOCS Register 2

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B028h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**
	21:20	**Upper MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

LNCFCMOCS2 - LNCF MOCS Register 2

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 **Upper MOCS Index - Skip Caching Control**

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS2 - LNCF MOCS Register 2

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS2 - LNCF MOCS Register 2

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 3

LNCFCMOCS3 - LNCF MOCS Register 3

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B02Ch

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses **Value** / **Name**: 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global Go** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 **Value** / **Name**: 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS3 - LNCF MOCS Register 3

21:20 **Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 **Upper MOCS Index - Skip Caching Control**

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS3 - LNCF MOCS Register 3

	7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
	6	**Lower Global Go** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 **[Default]** 1 – LOWER_GOMemory
	5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls 0h – LOWER_DIRECT – Use binding table index for direct EU accesses - for the rest it is reserved. 1h – LOWER_UC **[Default]** – Uncacheable 2h – LOWER_RESERVED – Reserved 3h – LOWER_WB – Writeback

LNCFCMOCS3 - LNCF MOCS Register 3

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 4

LNCFCMOCS4 - LNCF MOCS Register 4

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B030h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global Go** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 **[Default]** 1 – UPPER_GOMemory

LNCFCMOCS4 - LNCF MOCS Register 4

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB **[Default]**	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS4 - LNCF MOCS Register 4

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global Go

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS4 - LNCF MOCS Register 4

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 5

LNCFCMOCS5 - LNCF MOCS Register 5

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B034h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global Go** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS5 - LNCF MOCS Register 5

21:20 **Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 **Upper MOCS Index - Skip Caching Control**

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS5 - LNCF MOCS Register 5

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global Go

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS5 - LNCF MOCS Register 5

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 6

LNCFCMOCS6 - LNCF MOCS Register 6

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B038h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS6 - LNCF MOCS Register 6

21:20 **Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 **Upper MOCS Index - Skip Caching Control**

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS6 - LNCF MOCS Register 6

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS6 - LNCF MOCS Register 6

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 7

LNCFCMOCS7 - LNCF MOCS Register 7

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B03Ch

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS7 - LNCF MOCS Register 7

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS7 - LNCF MOCS Register 7

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_WT	Writethrough
3h	LOWER_WB	Writeback

LNCFCMOCS7 - LNCF MOCS Register 7

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 8

LNCFCMOCS8 - LNCF MOCS Register 8

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B040h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses **Value** / **Name**: 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 **Value** / **Name**: 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS8 - LNCF MOCS Register 8

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS8 - LNCF MOCS Register 8

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS8 - LNCF MOCS Register 8

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 9

LNCFCMOCS9 - LNCF MOCS Register 9

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B044h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS9 - LNCF MOCS Register 9

21:20 **Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 **Upper MOCS Index - Skip Caching Control**

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS9 - LNCF MOCS Register 9

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS9 - LNCF MOCS Register 9

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 10

LNCFCMOCS10 - LNCF MOCS Register 10

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B048h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS10 - LNCF MOCS Register 10

21:20 **Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 **Upper MOCS Index - Skip Caching Control**

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS10 - LNCF MOCS Register 10

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS10 - LNCF MOCS Register 10

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 11

LNCFCMOCS11 - LNCF MOCS Register 11

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B04Ch

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS11 - LNCF MOCS Register 11

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS11 - LNCF MOCS Register 11

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS11 - LNCF MOCS Register 11

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 12

LNCFCMOCS12 - LNCF MOCS Register 12

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B050h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 **[Default]** 1 – UPPER_GOMemory

LNCFCMOCS12 - LNCF MOCS Register 12

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB **[Default]**	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS12 - LNCF MOCS Register 12

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS12 - LNCF MOCS Register 12

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 13

LNCFCMOCS13 - LNCF MOCS Register 13

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B054h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS13 - LNCF MOCS Register 13

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS13 - LNCF MOCS Register 13

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS13 - LNCF MOCS Register 13

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 14

LNCFCMOCS14 - LNCF MOCS Register 14

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B058h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS14 - LNCF MOCS Register 14

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS14 - LNCF MOCS Register 14

	7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
	6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 1 – LOWER_GOMemory **[Default]**
	5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls 0h – LOWER_DIRECT – Use binding table index for direct EU accesses - for the rest it is reserved. 1h – LOWER_UC **[Default]** – Uncacheable 2h – LOWER_RESERVED – Reserved 3h – LOWER_WB – Writeback

LNCFCMOCS14 - LNCF MOCS Register 14

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 15

LNCFCMOCS15 - LNCF MOCS Register 15

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B05Ch

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS15 - LNCF MOCS Register 15

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS15 - LNCF MOCS Register 15

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS15 - LNCF MOCS Register 15

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 16

LNCFCMOCS16 - LNCF MOCS Register 16

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B060h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS16 - LNCF MOCS Register 16

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS16 - LNCF MOCS Register 16

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS16 - LNCF MOCS Register 16

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 17

LNCFCMOCS17 - LNCF MOCS Register 17

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B064h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS17 - LNCF MOCS Register 17

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS17 - LNCF MOCS Register 17

	7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
	6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 1 – LOWER_GOMemory **[Default]**
	5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS17 - LNCF MOCS Register 17

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 18

LNCFCMOCS18 - LNCF MOCS Register 18

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B068h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS18 - LNCF MOCS Register 18

21:20	**Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17	**Upper MOCS Index - Skip Caching Control**

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16	**Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15	**Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8	**Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS18 - LNCF MOCS Register 18

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS18 - LNCF MOCS Register 18

3:1 Lower MOCS Index - Skip Caching Control

Default Value:	7h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

0 Lower MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 19

LNCFCMOCS19 - LNCF MOCS Register 19

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B06Ch

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS19 - LNCF MOCS Register 19

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS19 - LNCF MOCS Register 19

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS19 - LNCF MOCS Register 19

3:1 Lower MOCS Index - Skip Caching Control

Default Value:	1h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

0 Lower MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 20

LNCFCMOCS20 - LNCF MOCS Register 20

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B070h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 **[Default]** 1 – UPPER_GOMemory

LNCFCMOCS20 - LNCF MOCS Register 20

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB **[Default]**	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS20 - LNCF MOCS Register 20

	7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
	6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 1 – LOWER_GOMemory **[Default]**
	5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS20 - LNCF MOCS Register 20

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 21

LNCFCMOCS21 - LNCF MOCS Register 21

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B074h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS21 - LNCF MOCS Register 21

21:20 **Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 **Upper MOCS Index - Skip Caching Control**

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS21 - LNCF MOCS Register 21

7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 1 – LOWER_GOMemory **[Default]**
5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS21 - LNCF MOCS Register 21

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 22

LNCFCMOCS22 - LNCF MOCS Register 22

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B078h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS22 - LNCF MOCS Register 22

21:20 **Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 **Upper MOCS Index - Skip Caching Control**

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 **Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 **Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 **Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS22 - LNCF MOCS Register 22

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS22 - LNCF MOCS Register 22

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 23

LNCFCMOCS23 - LNCF MOCS Register 23

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B07Ch

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS23 - LNCF MOCS Register 23

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS23 - LNCF MOCS Register 23

7 **Lower UC L3 Lookup**

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 **Lower Global GO**

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3 **[Default]**
1	LOWER_GOMemory

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS23 - LNCF MOCS Register 23

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE **[Default]**
1h	LOWER_ESC_ENABLE

LNCF MOCS Register 24

LNCFCMOCS24 - LNCF MOCS Register 24

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B080h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS24 - LNCF MOCS Register 24

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS24 - LNCF MOCS Register 24

7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 **[Default]** 1 – LOWER_GOMemory
5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS24 - LNCF MOCS Register 24

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE **[Default]** 1h / LOWER_ESC_ENABLE

LNCF MOCS Register 25

LNCFCMOCS25 - LNCF MOCS Register 25

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B084h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS25 - LNCF MOCS Register 25

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS25 - LNCF MOCS Register 25

	7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
	6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 **[Default]** 1 – LOWER_GOMemory
	5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls 0h – LOWER_DIRECT – Use binding table index for direct EU accesses - for the rest it is reserved. 1h – LOWER_UC **[Default]** – Uncacheable 2h – LOWER_RESERVED – Reserved 3h – LOWER_WB – Writeback

LNCFCMOCS25 - LNCF MOCS Register 25

3:1 Lower MOCS Index - Skip Caching Control

Default Value:	1h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

0 Lower MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 26

LNCFCMOCS26 - LNCF MOCS Register 26

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B088h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS26 - LNCF MOCS Register 26

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS26 - LNCF MOCS Register 26

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS26 - LNCF MOCS Register 26

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 27

LNCFCMOCS27 - LNCF MOCS Register 27

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B08Ch

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS27 - LNCF MOCS Register 27

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS27 - LNCF MOCS Register 27

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS27 - LNCF MOCS Register 27

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 28

LNCFCMOCS28 - LNCF MOCS Register 28

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B090h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 **[Default]** 1 – UPPER_GOMemory

LNCFCMOCS28 - LNCF MOCS Register 28

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB **[Default]**	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS28 - LNCF MOCS Register 28

	7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
	6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 **[Default]** 1 – LOWER_GOMemory
	5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls 0h – LOWER_DIRECT – Use binding table index for direct EU accesses - for the rest it is reserved. 1h – LOWER_UC **[Default]** – Uncacheable 2h – LOWER_RESERVED – Reserved 3h – LOWER_WB – Writeback

LNCFCMOCS28 - LNCF MOCS Register 28

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 7h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 29

LNCFCMOCS29 - LNCF MOCS Register 29

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B094h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 **[Default]** 1 – UPPER_GOMemory

LNCFCMOCS29 - LNCF MOCS Register 29

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC **[Default]**	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	3h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE
1h	UPPER_ESC_ENABLE **[Default]**

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS29 - LNCF MOCS Register 29

7 **Lower UC L3 Lookup**

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 **Lower Global GO**

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 **Lower MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS29 - LNCF MOCS Register 29

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 1h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target. **Bit Offset** / **Corresponding Address Bit** 0 / 9 1 / 10 2 / 11
	0	**Lower MOCS Index - Enable Skip Caching** Access: R/W Lock Enable the skip cache mechanism **Value** / **Name** 0h / LOWER_ESC_DISABLE 1h / LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 30

LNCFCMOCS30 - LNCF MOCS Register 30

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B098h

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: WO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS30 - LNCF MOCS Register 30

21:20	**Upper MOCS Index - L3 Cacheability Control**

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17	**Upper MOCS Index - Skip Caching Control**

Default Value:	0h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes
If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16	**Upper MOCS Index - Enable Skip Caching**

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15	**Lower MOCS Index Mask Bit**

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8	**Reserved**

Access:	RO
Format:	MBZ

LNCFCMOCS30 - LNCF MOCS Register 30

	7	**Lower UC L3 Lookup** Access: R/W Lock **Description**: Enable Lookup for uncacheable accesses 0 – LOWER_UCL3LKDIS 1 – LOWER_UCL3LKEN **[Default]**
	6	**Lower Global GO** Access: R/W Lock **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – LOWER_GOL3 1 – LOWER_GOMemory **[Default]**
	5:4	**Lower MOCS Index - L3 Cacheability Control** Access: R/W Lock Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index. For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC **[Default]**	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS30 - LNCF MOCS Register 30

3:1 Lower MOCS Index - Skip Caching Control

Default Value:	7h
Access:	R/W Lock

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

0 Lower MOCS Index - Enable Skip Caching

Access:	R/W Lock

Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE
1h	LOWER_ESC_ENABLE **[Default]**

LNCF MOCS Register 31

LNCFCMOCS31 - LNCF MOCS Register 31

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B09Ch

Description
Programming note: WAReprogramMOCS: Upon render reset the driver needs to reprogram the LNCF MOCS Register.

DWord	Bit	Description
0	31	**Upper MOCS Index Mask Bit** Access: RO In order to prevent overwriting the upper MOCS index of this register, this bit must be set as part of the write.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Upper UC L3 Lookup** Access: RO **Description**: Enable Lookup for uncacheable accesses 0 – UPPER_UCL3LKDIS 1 – UPPER_UCL3LKEN **[Default]**
	22	**Upper Global GO** Access: RO **Description**: Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3 0 – UPPER_GOL3 1 – UPPER_GOMemory **[Default]**

LNCFCMOCS31 - LNCF MOCS Register 31

21:20 Upper MOCS Index - L3 Cacheability Control

Access:	RO

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	UPPER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	UPPER_UC	Uncacheable
2h	UPPER_RESERVED	Reserved
3h	UPPER_WB	Writeback

19:17 Upper MOCS Index - Skip Caching Control

Default Value:	0h
Access:	RO

Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface.

Programming Notes

If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care.
If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

16 Upper MOCS Index - Enable Skip Caching

Access:	RO

Enable the skip cache mechanism

Value	Name
0h	UPPER_ESC_DISABLE **[Default]**
1h	UPPER_ESC_ENABLE

15 Lower MOCS Index Mask Bit

Access:	WO

In order to prevent overwriting the lower MOCS index of this register, this bit must be set as part of the write.

14:8 Reserved

Access:	RO
Format:	MBZ

LNCFCMOCS31 - LNCF MOCS Register 31

7 — Lower UC L3 Lookup

Access:	R/W Lock

Description
Enable Lookup for uncacheable accesses

Value	Name
0	LOWER_UCL3LKDIS
1	LOWER_UCL3LKEN **[Default]**

6 — Lower Global GO

Access:	R/W Lock

Description
Push the Go point to memory for L3 destined transaction. SW needs to program cacheability to UC for Global GO, otherwise GO point will be moved to L3

Value	Name
0	LOWER_GOL3
1	LOWER_GOMemory **[Default]**

5:4 — Lower MOCS Index - L3 Cacheability Control

Access:	R/W Lock

Memory type information used in L3. This field is combined with the additional two bits that are sent by HDC based on binding table index.
For all other L3 requesters, this field is the primary source of L3 cache controls

Value	Name	Description
0h	LOWER_DIRECT **[Default]**	Use binding table index for direct EU accesses - for the rest it is reserved.
1h	LOWER_UC	Uncacheable
2h	LOWER_RESERVED	Reserved
3h	LOWER_WB	Writeback

LNCFCMOCS31 - LNCF MOCS Register 31

	3:1	**Lower MOCS Index - Skip Caching Control** Default Value: 0h Access: R/W Lock Defines the bit values to enable caching. Outcome overrides the L3/LLC caching for the surface. **Programming Notes** If a given bit is programmed to 0, then the corresponding address bit value is treated as a don't care. If a given bit is programmed to 1, then the corresponding address bit must be 0 to cache in the target.

Bit Offset	Corresponding Address Bit
0	9
1	10
2	11

Lower MOCS Index - Enable Skip Caching

Access: R/W Lock

Enable the skip cache mechanism

Value	Name
0h	LOWER_ESC_DISABLE **[Default]**
1h	LOWER_ESC_ENABLE

LNE Arbiter configuration register

LNE_ARB_CFG - LNE Arbiter configuration register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B0E0h

DWord	Bit	Description
0	31:29	**Weight of Local Bank read return** Access: R/W Value / Name: 1h 2h **[Default]** 3h 4h
	28:26	**Weight of Gglobal URB read return** Access: R/W Value / Name: 1h 2h 3h 4h **[Default]**
	25:23	**Weight of render target read return** Access: R/W Value / Name: 1h **[Default]** 2h 3h 4h

LNE_ARB_CFG - LNE Arbiter configuration register

22:20	**Weight of local bank read return in 1 and 2 memory slice**
	Access: R/W

Value	Name
1h	**[Default]**
2h	
3h	
4h	

19:17	**Weight of cross slice read return in 1 and 2 memory slice**
	Access: R/W

Value	Name
1h	**[Default]**
2h	
3h	
4h	

16:14	**Weight of local bank read return in 4 memory slice**
	Access: R/W

Value	Name
1h	**[Default]**
2h	
3h	
4h	

13:11	**Weight of cross slice read return in 4 memory slice**
	Access: R/W

Value	Name
1h	
2h	
3h	**[Default]**
4h	

10:0	**LNE spare config bits**
	Access: R/W

LNI destination request Arbiter configuration register

LNI_DCR_SCR_ARB_CFG - LNI destination request Arbiter configuration register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B0ECh

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25:21	**Weight of NDX clients in LSN B2B DCR arbiter** Access: R/W Value / Name: 1h **[Default]**; 2h; 3h; 4h
	20:16	**Weight of LNGP/SARB in LSN B2B DCR arbiter** Access: R/W Value / Name: 1h **[Default]**; 2h; 3h; 4h; 6h; 8h; 0ch; 0fh
	15:13	**Reserved** Access: RO Format: MBZ

LNI_DCR_SCR_ARB_CFG - LNI destination request Arbiter configuration register

	12:10	**Weight of all clients in CBE, URB B2B arbiter** Access: R/W **Value** / **Name** 1h / **[Default]** 2h 3h 4h
	9:5	**Weight of NDX clients in bank B2B DCR arbiter** Access: R/W **Value** / **Name** 1h / **[Default]** 2h 3h 4h
	4:0	**Weight of LNGP/SARB in bank B2B DCR arbiter** Access: R/W **Value** / **Name** 1h / **[Default]** 2h 3h 4h 6h 8h 0ch 0fh

LNI LNGP request source conflict resolution Arbiter configuration register

LNI_LNGP_SCR_ARB_CFG - LNI LNGP request source conflict resolution Arbiter configuration register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B0E8h

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:12	**Weight of Local read request in 1 and 2 memory slice config in source conflict resolution arbiter** Access: R/W
	11:8	**Weight of cross slice request in 1 and 2 memory slice config in source conflict resolution arbiter** Access: R/W

15:12 — Weight of Local read request in 1 and 2 memory slice config in source conflict resolution arbiter

Value	Name
1h	**[Default]**
2h	
3h	
4h	
6h	
9h	

11:8 — Weight of cross slice request in 1 and 2 memory slice config in source conflict resolution arbiter

Value	Name
1h	**[Default]**
2h	
3h	
4h	
6h	

LNI_LNGP_SCR_ARB_CFG - LNI LNGP request source conflict resolution Arbiter configuration register

	7:4	**Weight of Local read request in 4 memory slice config in source conflict resolution arbiter** Access: R/W **Value** / **Name** 1h: **[Default]** 2h: 3h: 4h:
	3:0	**Weight of cross slice request in 4 memory slice config in source conflict resolution arbiter** Access: R/W **Value** / **Name** 1h: **[Default]** 2h: 3h: 04h: 06h: 08h:

LNI NDX request source conflict resolution Arbiter configuration register

LNI_NDX_SCR_ARB_CFG - LNI NDX request source conflict resolution Arbiter configuration register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B0E4h

DWord	Bit	Description
0	31:27	**Weight of Local read request in 1 and 2 memory slice config in source conflict resolution arbiter** Access: R/W **Value** / **Name** 1h / **[Default]** 2h 3h 4h 6h 9h
	26:22	**Weight of cross slice request in 1 and 2 memory slice config in source conflict resolution arbiter** Access: R/W **Value** / **Name** 1h / **[Default]** 2h 3h 4h 6h

LNI_NDX_SCR_ARB_CFG - LNI NDX request source conflict resolution Arbiter configuration register

	21:17	**Weight of Local read request in 4 memory slice config in source conflict resolution arbiter** Access: R/W Value: 1h **[Default]**; 2h; 3h; 4h
	16:12	**Weight of cross slice request in 4 memory slice config in source conflict resolution arbiter** Access: R/W Value: 1h **[Default]**; 2h; 3h; 04h; 06h; 08h
	11:9	**Weight of Local completion in 1 and 2 memory slice config in source conflict resolution arbiter** Default Value: 1h Access: R/W
	8:6	**Weight of cross slice completion in 1 and 2 memory slice config in source conflict resolution arbiter** Default Value: 2h Access: R/W
	5:3	**Weight of Local completion in 4 memory slice config in source conflict resolution arbiter** Default Value: 1h Access: R/W
	2:0	**Weight of cross completion in 4 memory slice config in source conflict resolution arbiter** Default Value: 6h Access: R/W

LNI Second Arbiter configuration register in 1 and 2 MEM slice CFG

LNI_SND_ARB_CFG_NON_4MEMSL - LNI Second Arbiter configuration register in 1 and 2 MEM slice CFG

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32
_Custom_GTIReset: DEV

Address: 0B0B8h

DWord	Bit	Description
0	31:28	**Weight of Local CBE request in 1 and 2 memory slice config in CBE vs local arbiter** Access: R/W **Value** / **Name** 1h / **[Default]** 2h 3h 4h
	27:24	**Weight of Local bank fifo request in 1 and 2 memory slice config in CBE vs local arbiter** Access: R/W **Value** / **Name** 1h 2h 3h / **[Default]** 4h
	23:20	**Weight of Local LBK and CBE request in 1 and 2 memory slice config in cross vs local arbiter** Access: R/W **Value** / **Name** 1h / **[Default]** 2h 3h 4h

LNI_SND_ARB_CFG_NON_4MEMSL - LNI Second Arbiter configuration register in 1 and 2 MEM slice CFG

19:15 Weight of Cross slice request in 1 and 2 memory slice config in cross vs local arbiter

Access:	R/W

Value	Name
1h	**[Default]**
2h	
3h	
4h	

14:12 Weight of Local bank request in 1 and 2 memory slice config in LSN cross slice LNI arbiter

Access:	R/W

Value	Name
3h	**[Default]**

11:9 Weight of Cross slice CBE request in 1 and 2 memory slice config in LSN cross slice LNI arbiter

Default Value:	1h
Access:	R/W

8:5 Weight of Local GURB request in 1 and 2 memory slice config in cross vs local URB arbiter

Default Value:	1h
Access:	R/W

4 Disable Global URB stall fix

Access:	R/W

Value	Name
0h	**[Default]**

3:0 Weight of Cross slice Global URB request in 4 memory slice config in cross vs local URB arbiter

Access:	R/W

Value	Name
6h	**[Default]**

LNI Second Arbiter configuration register in 4 MEM slice CFG

LNI_SND_ARB_CFG_4MSL - LNI Second Arbiter configuration register in 4 MEM slice CFG

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B0BCh

DWord	Bit	Description
0	31:28	**Weight of Local CBE request in 4 memory slice config in CBE vs local arbiter** Access: R/W Value / Name: 1h **[Default]** 2h 3h 4h
	27:24	**Weight of Local bank fifo request in 4 memory slice config in CBE vs local arbiter** Access: R/W Value / Name: 1h 2h 3h **[Default]** 4h
	23:20	**Weight of Local LBK and CBE request in 4 memory slice config in cross vs local arbiter** Access: R/W Value / Name: 1h **[Default]** 2h 3h 4h

LNI_SND_ARB_CFG_4MSL - LNI Second Arbiter configuration register in 4 MEM slice CFG

	19:15	**Weight of Cross slice request in 4 memory slice config in cross vs local arbiter** Access: R/W **Value** / **Name** 6h 9h 0ch
	14:12	**Weight of Local bank request in 4 memory slice config in LSN cross slice LNI arbiter** Access: R/W **Value** / **Name** 3h **[Default]**
	11:9	**Weight of Cross slice CBE request in 4 memory slice config in LSN cross slice LNI arbiter** Default Value: 1h Access: R/W
	8:5	**Weight of Local GURB request in 4 memory slice config in cross vs local URB arbiter** Default Value: 1h Access: R/W
	4	**Disable Global URB stall fix** Access: R/W **Value** / **Name** 0h **[Default]**
	3:0	**Weight of Cross slice Global URB request in 4 memory slice config in cross vs local URB arbiter** Access: R/W **Value** / **Name** 6h **[Default]**

Load Indirect Base Vertex

3DPRIM_BASE_VERTEX - Load Indirect Base Vertex	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02440h-02443h
Name:	Load Indirect Base Vertex
ShortName:	3DPRIM_BASE_VERTEX_RCSUNIT_BE_GEOMETRY
Address:	18440h-18443h
Name:	Load Indirect Base Vertex
ShortName:	3DPRIM_BASE_VERTEX_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Base Vertex** Access: R/W Format: S31 This register is used to store the Base Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Extended Parameter 0

3DPRIM_XP0 - Load Indirect Extended Parameter 0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02690h-02693h
Name:	Load Indirect Extended Parameter 0
ShortName:	3DPRIM_XP0_RCSUNIT_BE_GEOMETRY
Address:	18690h-18693h
Name:	Load Indirect Extended Parameter 0
ShortName:	3DPRIM_XP0_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Extended Parameter 0** Access: R/W Format: U32 **Description** This register is used to store the Extended Parameter 0 of the 3D_PRIMITIVE command when Load Indirect Enable is set. This register is used to store the Extended Parameter 0 of the 3D_PRIMITIVE or 3DMESH_1D or 3DMESH_3D commands when Load Indirect Enable is set.

Load Indirect Extended Parameter 1

3DPRIM_XP1 - Load Indirect Extended Parameter 1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02694h-02697h
Name:	Load Indirect Extended Parameter 1
ShortName:	3DPRIM_XP1_RCSUNIT_BE_GEOMETRY
Address:	18694h-18697h
Name:	Load Indirect Extended Parameter 1
ShortName:	3DPRIM_XP1_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Extended Parameter 1** Access: R/W Format: U32 **Description** This register is used to store the Extended Parameter 1 of the 3D_PRIMITIVE command when Load Indirect Enable is set. This register is used to store the Extended Parameter 1 of the 3D_PRIMITIVE command or the Thread Group Count Y of the 3DMESH_3D command when Load Indirect Enable is set.

Load Indirect Extended Parameter 2

3DPRIM_XP2 - Load Indirect Extended Parameter 2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02698h-0269Bh
Name:	Load Indirect Extended Parameter 2
ShortName:	3DPRIM_XP2_RCSUNIT_BE_GEOMETRY
Address:	18698h-1869Bh
Name:	Load Indirect Extended Parameter 2
ShortName:	3DPRIM_XP2_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Extended Parameter 2** Access: R/W Format: U32 **Description** This register is used to store the Extended Parameter 2 of the 3D_PRIMITIVE command when Load Indirect Enable is set. This register is used to store the Extended Parameter 2 of the 3D_PRIMITIVE command or the Thread Group Count Z of the 3DMESH_3D command when Load Indirect Enable is set.

Load Indirect Instance Count

3DPRIM_INSTANCE_COUNT - Load Indirect Instance Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02438h-0243Bh
Name:	Load Indirect Instance Count
ShortName:	3DPRIM_INSTANCE_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18438h-1843Bh
Name:	Load Indirect Instance Count
ShortName:	3DPRIM_INSTANCE_COUNT_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Instance Count** Access: R/W This register is used to store the Instance Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Starting Thread Group ID

3DMESH_STARTING_TGID - Load Indirect Starting Thread Group ID

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	026F4h-026F7h

DWord	Bit	Description
0	31:0	**Starting Thread Group ID** Access: R/W Format: U32 This register is used to store the Starting Thread Group ID of the 3DMESH command when Indirect Parameter Enable is set.

Load Indirect Start Instance

3DPRIM_START_INSTANCE - Load Indirect Start Instance	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0243Ch-0243Fh
Name:	Load Indirect Start Instance
ShortName:	3DPRIM_START_INSTANCE_RCSUNIT_BE_GEOMETRY
Address:	1843Ch-1843Fh
Name:	Load Indirect Start Instance
ShortName:	3DPRIM_START_INSTANCE_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Start Vertex** Access: R/W Format: U32 This register is used to store the Start Instance of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Start Vertex

3DPRIM_START_VERTEX - Load Indirect Start Vertex	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02430h-02433h
Name:	Load Indirect Start Vertex
ShortName:	3DPRIM_START_VERTEX_RCSUNIT_BE_GEOMETRY
Address:	18430h-18433h
Name:	Load Indirect Start Vertex
ShortName:	3DPRIM_START_VERTEX_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Start Vertex** Access: R/W Format: U32 This register is used to store the Start Vertex of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Load Indirect Thread Group Count

3DMESH_TG_COUNT - Load Indirect Thread Group Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	026F0h-026F3h

DWord	Bit	Description
0	31:0	**Thread Group Count** Access: R/W Format: U32 This register is used to store the Thread Group Count of the 3DMESH command when Indirect Parameter Enable is set.

Load Indirect Vertex Count

3DPRIM_VERTEX_COUNT - Load Indirect Vertex Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02434h-02437h
Name:	Load Indirect Vertex Count
ShortName:	3DPRIM_VERTEX_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18434h-18437h
Name:	Load Indirect Vertex Count
ShortName:	3DPRIM_VERTEX_COUNT_POCSUNIT_BE_GEOMETRY

DWord	Bit	Description
0	31:0	**Vertex Count** Access: R/W Format: U32 This register is used to store the Vertex Count of the 3D_PRIMITIVE command when Load Indirect Enable is set.

Local Memory Bar

LMEMBAR_0_2_0_PCI - Local Memory Bar

Register Space:	PCI: 0/2/0
Size (in bits):	64
Address:	00018h

The Local Memory Bar is used by S/W to access Gfx Gdie local memory.

DWord	Bit	Description
0	63:39	**Memory Base Address** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [63:39].
	38	**512GB Address Mask** Default Value: 0 Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE. RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 512GB
	37	**256GB Address Mask** Default Value: 0 Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE. RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 256GB
	36	**128GB Address Mask** Default Value: 0 Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE. RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 128GB

LMEMBAR_0_2_0_PCI - Local Memory Bar

	35	**64GB Address Mask** Default Value: 0 Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE. RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 64GB
	34	**32 GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE. RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 32GB
	33	**16 GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE. RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 16GB
	32	**8 GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE. RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 8GB
	31	**4 GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE.RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 4 GB

LMEMBAR_0_2_0_PCI - Local Memory Bar

30	**2 GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE.RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 2GB
29	**1 GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE.RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 1GB
28	**512MB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE.RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 512MB
27	**256 MB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of PF_RESZ_CTRL.PFBARSIZE.RO and force to zero when PF_RESZ_CTRL.PFBARSIZE >= 256MB
26:4	**Address Mask** Default Value: 00000000000000000000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s to indicate at least 128MB address range.

LMEMBAR_0_2_0_PCI - Local Memory Bar

	3	**Prefetchable Memory** Default Value: 1b Access: RO _Custom_GTIReset: BUS Hardwired to 1 to enable prefetching.
	2:1	**Memory Type** Default Value: 10b Access: RO _Custom_GTIReset: BUS Hardwired to 2h to indicate 64 bit base address.
	0	**Memory/IO Space** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 to indicate memory space.

Local Memory Configuration

LMEM_CFG - Local Memory Configuration

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CF58h

This register configures Local Memory related functionality in GAM.

DWord	Bit	Description
0	31	**Local Memory Enable** Default Value: 1b Enabled Access: R/W Enables Local Memory functionality in GAM. If Local Memory is not enabled, then the Local Memory bit in the page tables is ignored, and all PPGTT and GGTT translation addresses are interpreted as Guest Physical Addresses (GPA) that require VTd translation (assuming VTd is enabled). If Local Memory is enabled, then GPA are translated through the Local Memory Translation Table (LMTT) instead of VTd.
	30:0	**LMTT Directory Ptr** Default Value: 00b Access: R/W Base address offset of the LMTT Directory in Local Memory, in multiples of 64KB. Bits above LM_HAW are no used.

Lock register for Bank

L3BANKLOCK - Lock register for Bank

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B160h

This is a basic register template

DWord	Bit	Description
0	31	**Lockdown L3BANKLOCK for writes** Default Value: 0h Access: R/W 0 : (default) All bits of L3BANKLOCK (offset 0xB160) register are R/W 1 : All bits of L3BANKLOCK (offset 0xB160) register are RO Once written to 1, the lock is set for all of 0B160 and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock Control is 0B160h bit 31
	30:17	**Reserved** Access: RO Format: MBZ
	16:15	**Reserved** Access: RO Format: MBZ
	14	**Lockdown L3SQCREG7 for writes** Access: R/W Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Value / Name / Description 0 / **[Default]** / 1 / / All bits of L3SQCREG7 (offset 0xB188) register are RO
	13	**Lockdown L3_ECC_TEST_CTL for writes** Access: R/W Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Value / Name / Description 0 / **[Default]** / 1 / / All bits of L3_ECC_TEST_CTL (offset 0xB13C) and URB_ECC_TEST_CTL (offset 0xB148) registers are RO.

L3BANKLOCK - Lock register for Bank

12 — Lockdown L3SQCREG3 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of L3SQCREG3 (offset 0xB108) register are RO.

11:10 — Reserved

Access:	RO
Format:	MBZ

9 — Lockdown SCRATCH1 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of SCRATCH1 (offset 0xB11C) register are RO.

8 — Lockdown LTCDREG2 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of LTCDREG2 (offset 0xB110) register are RO.

7 — Lockdown L3SQCREG2 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	
1		All bits of L3SQCREG2 (offset 0xB104) register are RO.

6 — Lockdown L3SCRATCH3 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0	default **[Default]**	All bits of L3SCRATCH3 (offset 0xB154) register are R/W
1		Bits [10:4] of L3SCRATCH3 (offset 0xB154) register are RO.

L3BANKLOCK - Lock register for Bank

5 — Lockdown L3SCRATCH2 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	**[Default]**	(default) All bits of L3SCRATCH2;(offset 0xB140) register are R/W
1		All bits of L3SCRATCH2 offset 0xB140) register are RO

4 — Lockdown L3SQCREG1 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	Default **[Default]**	All valid bits of L3SQREG1 (offset 0xB100) register are R/W
1		All valid bits of L3SQREG1 (offset 0xB100) register are R/W (no locking effect)

3 — Lockdown LTCDREG for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	**[Default]**	(default) All bits of LTCDREG (offset 0xB120) register are R/W
1		All bits of LTCDREG (offset 0xB120) register are RO

2 — Lockdown L3SQCREG4 for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	**[Default]**	(default) All bits of L3SQREG4 (offset 0xB118) register are R/W
1		All bits of L3SQREG4 (offset 0xB118) register are R/W (no locking effect)

1 — Lockdown L3CHMD for writes

Access:	R/W

Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).

Value	Name	Description
0h	**[Default]**	(default) All bits of L3CHMD (offset 0xB114) register are R/W
1		All bits of L3CHMD (offset 0xB114) register are RO

L3BANKLOCK - Lock register for Bank

	0	**Lockdown L3CNTLREG1 for writes** Access: R/W Once Lock Control 0xB160h bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). **Value** / **Name** / **Description** 0h / **[Default]** / (default) - All bits of L3CNTLREG1 (offset 0xB10C) register are R/W 1 / / All bits of L3CNTLREG1 (offset 0xB10C) register are RO

Lock register for Node

L3NODELOCK - Lock register for Node		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B0ACh	
This is a basic register template		
DWord	**Bit**	**Description**
0	31	**Lockdown L3NODELOCK** Default Value: 0h Access: R/W 0 : (default) All bits of L3NODELOCK (offset 0xB0AC) register are R/W 1 : All bits of L3NODELOCK (offset 0xB0AC) register are RO Once written to 1, the lock is set for all of 0xB0AC and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock Control is 0B0ACh bit 31
	30:4	**Reserved** Access: RO Format: MBZ
	3:2	**Reserved** Access: RO Format: MBZ
	1	**Lockdown TC/vc sel, LSN arb pri sel** Default Value: 0h Access: R/W 0 : (default) bits is R/W 1 : bit is RO Once Lock Control 0B0ACh bit 31 is written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock).
	0	**Reserved** Access: RO Format: MBZ

LPFC FUSA Register

LPFC_FUSA - LPFC FUSA Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B480h

Functional Safety Register. LPFC collects updates of single and double bit errors from all LBCF in ECC Checker Mode.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Double bit error indication from Bank 7** Access: R/W Double Error detection indication from Bank7.
	14	**Single bit error indication from Bank 7** Access: R/W Single Error detection indication from Bank7.
	13	**Double bit error indication from Bank 6** Access: R/W Double Error detection indication from Bank6.
	12	**Single bit error indication from Bank 6** Access: R/W Single Error detection indication from Bank6.
	11	**Double bit error indication from Bank 5** Access: R/W Double Error detection indication from Bank5.
	10	**Single bit error indication from Bank 5** Access: R/W Single Error detection indication from Bank5.

LPFC_FUSA - LPFC FUSA Register

	9	**Double bit error indication from Bank 4** Access: R/W Double Error detection indication from Bank4.
	8	**Single bit error indication from Bank 4** Access: R/W Single Error detection indication from Bank4.
	7	**Double bit error indication from Bank 3** Access: R/W Double Error detection indication from Bank3.
	6	**Single bit error indication from Bank 3** Access: R/W Single Error detection indication from Bank3.
	5	**Double bit error indication from Bank 2** Access: R/W Double Error detection indication from Bank2.
	4	**Single bit error indication from Bank 2** Access: R/W Single Error detection indication from Bank2.
	3	**Double bit error indication from Bank 1** Access: R/W Double Error detection indication from Bank1.
	2	**Single bit error indication from Bank 1** Access: R/W Single Error detection indication from Bank1.
	1	**Double bit error indication from Bank 0** Access: R/W Double Error detection indication from Bank0.
	0	**Single bit error indication from Bank 0** Access: R/W Single Error detection indication from Bank0.

LPFC FUSA Register1

LPFC_FUSA1 - LPFC FUSA Register1

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B484h

Functional Safety Register. LPFC collects updates of single and double bit errors from all LBCF in ECC Checker Mode.

DWord	Bit	Description
0	31:16	**Mask** Access: R/W
	15	**Double bit error indication from Bank 15** Access: R/W Double Error detection indication from Bank15.
	14	**Single bit error indication from Bank 15** Access: R/W Single Error detection indication from Bank15.
	13	**Double bit error indication from Bank 14** Access: R/W Double Error detection indication from Bank14.
	12	**Single bit error indication from Bank 14** Access: R/W Single Error detection indication from Bank14.
	11	**Double bit error indication from Bank 13** Access: R/W Double Error detection indication from Bank13.
	10	**Single bit error indication from Bank 13** Access: R/W Single Error detection indication from Bank13.
	9	**Double bit error indication from Bank 12** Access: R/W Double Error detection indication from Bank12.

LPFC_FUSA1 - LPFC FUSA Register1

	8	**Single bit error indication from Bank 12** Access: R/W Single Error detection indication from Bank12.
	7	**Double bit error indication from Bank 11** Access: R/W Double Error detection indication from Bank11.
	6	**Single bit error indication from Bank 11** Access: R/W Single Error detection indication from Bank11.
	5	**Double bit error indication from Bank 10** Access: R/W Double Error detection indication from Bank10.
	4	**Single bit error indication from Bank 10** Access: R/W Single Error detection indication from Bank10.
	3	**Double bit error indication from Bank 9** Access: R/W Double Error detection indication from Bank9.
	2	**Single bit error indication from Bank 9** Access: R/W Single Error detection indication from Bank9.
	1	**Double bit error indication from Bank 8** Access: R/W Double Error detection indication from Bank8.
	0	**Single bit error indication from Bank 8** Access: R/W Single Error detection indication from Bank8.

LPFC FUSA Register2

LPFC_FUSA2 - LPFC FUSA Register2

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B488h

Functional Safety Register. LPFC collects updates of single and double bit errors from all LBCF in ECC Checker Mode.

DWord	Bit	Description
0	31:16	**Mask** Access: R/W
	15	**Double bit error indication from Bank 23** Access: R/W Double Error detection indication from Bank23.
	14	**Single bit error indication from Bank 23** Access: R/W Single Error detection indication from Bank23.
	13	**Double bit error indication from Bank 22** Access: R/W Double Error detection indication from Bank22.
	12	**Single bit error indication from Bank 22** Access: R/W Single Error detection indication from Bank22.
	11	**Double bit error indication from Bank 21** Access: R/W Double Error detection indication from Bank21.
	10	**Single bit error indication from Bank 21** Access: R/W Single Error detection indication from Bank21.
	9	**Double bit error indication from Bank 20** Access: R/W Double Error detection indication from Bank20.

LPFC_FUSA2 - LPFC FUSA Register2

	8	**Single bit error indication from Bank 20** Access: R/W Single Error detection indication from Bank20.
	7	**Double bit error indication from Bank 19** Access: R/W Double Error detection indication from Bank19.
	6	**Single bit error indication from Bank 19** Access: R/W Single Error detection indication from Bank19.
	5	**Double bit error indication from Bank 18** Access: R/W Double Error detection indication from Bank18.
	4	**Single bit error indication from Bank 18** Access: R/W Single Error detection indication from Bank18.
	3	**Double bit error indication from Bank 17** Access: R/W Double Error detection indication from Bank17.
	2	**Single bit error indication from Bank 17** Access: R/W Single Error detection indication from Bank17.
	1	**Double bit error indication from Bank 16** Access: R/W Double Error detection indication from Bank16.
	0	**Single bit error indication from Bank 16** Access: R/W Single Error detection indication from Bank16.

LPFC FUSA Register3

LPFC_FUSA3 - LPFC FUSA Register3

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B48Ch

Functional Safety Register. LPFC collects updates of single and double bit errors from all LBCF in ECC Checker Mode.

DWord	Bit	Description
0	31:16	**Mask** Access: R/W
	15	**Double bit error indication from Bank 31** Access: R/W Double Error detection indication from Bank31.
	14	**Single bit error indication from Bank 31** Access: R/W Single Error detection indication from Bank31.
	13	**Double bit error indication from Bank 30** Access: R/W Double Error detection indication from Bank30.
	12	**Single bit error indication from Bank 30** Access: R/W Single Error detection indication from Bank30.
	11	**Double bit error indication from Bank 29** Access: R/W Double Error detection indication from Bank29.
	10	**Single bit error indication from Bank 29** Access: R/W Single Error detection indication from Bank29.
	9	**Double bit error indication from Bank 28** Access: R/W Double Error detection indication from Bank28.

LPFC_FUSA3 - LPFC FUSA Register3

	8	**Single bit error indication from Bank 28** Access: R/W Single Error detection indication from Bank28.
	7	**Double bit error indication from Bank 27** Access: R/W Double Error detection indication from Bank27.
	6	**Single bit error indication from Bank 27** Access: R/W Single Error detection indication from Bank27.
	5	**Double bit error indication from Bank 26** Access: R/W Double Error detection indication from Bank26.
	4	**Single bit error indication from Bank 26** Access: R/W Single Error detection indication from Bank26.
	3	**Double bit error indication from Bank 25** Access: R/W Double Error detection indication from Bank25.
	2	**Single bit error indication from Bank 25** Access: R/W Single Error detection indication from Bank25.
	1	**Double bit error indication from Bank 24** Access: R/W Double Error detection indication from Bank24.
	0	**Single bit error indication from Bank 24** Access: R/W Single Error detection indication from Bank24.

LSN Arbitration Priority Register 0

LSN_ARBPRI - LSN Arbitration Priority Register 0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0B0D0h

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:12	**LSN Virtual Channel 1 Traffic Class Channel 1 Priority Value** Access: R/W **Description**: This value is 'm' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LSN Virtual Channel 1 cycles. Value: 1 — **[Default]** Value: [1,15]
	11:8	**LSN Virtual Channel 1 Traffic Class Channel 0 Priority Value** Access: R/W **Description**: This value is 'n' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LSN Virtual Channel 1 cycles. Value: 1 — **[Default]** Value: [1,15]
	7:4	**LSN Virtual Channel 0 Traffic Class Channel 1 Priority Value** Access: R/W This value is 'm' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LSN Virtual Channel 0 cycles. Value: 1 — **[Default]** Value: [1,15]

LSN_ARBPRI - LSN Arbitration Priority Register 0

	3:0	**LSN Virtual Channel 0 Traffic Class Channel 0 Priority Value** Access: R/W **Description** This value is 'n' in the n:m priority scheme for TCC0 vs. TCC1 arbitration on LSN Virtual Channel 0 cycles. **Value** / **Name** 1 / **[Default]** [1,15] /

LSN Miscellaneous Configuration

LSN_MISC - LSN Miscellaneous Configuration

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0B0CCh

DWord	Bit	Description
0	31:6	**Reserved** Access: RO Format: MBZ
	4	**LSN Egress Pipeline Clock Gating Enable** Access: R/W Value 1 **[Default]**: Enable fub-level clock gating of the LSN egress pipeline. Value 0: Disable fub-level clock gating of the LSN egress pipeline.
	3	**LSN Smart Gating for Slice-Bound Memory Fill Repeaters Disable** Access: R/W Value 1 **[Default]**: Disable the smart gating of slice-bound memory fill repeaters. Value 0: Allow smart-gating for slice-bound memory fill repeaters.
	2	**LSN Conservative Arbitration Control** Access: R/W Controls whether LSN uses a more conservative form of arbitration by removing assumptions about packet arrival Value 1: Cycles are only eligible for arbitration in the pipeline after arrival of all packets of the cycle. Value 0 **[Default]**: Cycles are eligible for arbitration after the arrival of the first packet of the cycle.

LSN_MISC - LSN Miscellaneous Configuration

1 — GAFS Return Simple Arbitration Control

Access:	R/W

Enables simple arbitration between upstream LSN busses when returning GAFS-bound read returns. This arbitration uses a continuously running counter to select two busses for GAFS-bound read returns.

Value	Name	Description
1	SIMPLE	Enable simple (always running) arbitration
0	PRIORITY **[Default]**	Enable priority-based arbitration

0 — LSN Cross-Slice Virtual Channel Arbitration Control

Access:	R/W

Controls whether to use round-robin or fixed priority arbitration between cross-slice virtual channels

Value	Name	Description
1	RR_PRI	Enable round-robin priority between VC1 and VC0
0	FIXED_PRI **[Default]**	Enable fixed priority between VC1 and VC0. VC1 will always take higher priority

LSN Slice Client Virtual Channel Assignment

LSN_SLCVC - LSN Slice Client Virtual Channel Assignment

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0B0C8h

DWord	Bit	Description
0	31:28	**Local LNI vs Cross Slice Completion arbitration weightage** Access: R/W **Value / Name / Description** 1h / **[Default]** / 1:1 between LNI and cross slice completion 2h / / 1:2 between LNI and cross slice completion 3h / / 1:3 between LNI and cross slice completion 4h / / 1:4 between LNI and cross slice completion
	27:24	**XSL weight in Local vs Cross Slice arbitration weightage** Access: R/W **Value / Name** 1h / **[Default]** 2h / 3h / 4h / 5h /
	23:20	**LNE weight in Local vs Cross Slice arbitration weightage** Access: R/W **Value / Name** 1h / **[Default]** 2h / 3h / 4h / 5h /

LSN_SLCVC - LSN Slice Client Virtual Channel Assignment

	19:16	**LNI weight in local vs Cross Slice arbitration weightage** Access: R/W **Value** / **Name** 1h: **[Default]** 2h: 3h: 4h: 5h:
	15:14	**Reserved** Access: RO Format: MBZ
	13:10	**Reserved** Access: RO Format: MBZ
	9	**Traffic Class Channel ID for L3 Cycles** Access: R/W **Value** / **Name** 0: **[Default]**
	8	**Virtual Channel ID for L3 Cycles** Default Value: 0 Access: R/W
	7:4	**Reserved** Access: RO Format: MBZ
	3	**Traffic Class Channel ID for Upstream L3-Bound Read Returns** Access: R/W **Value** / **Name** 1: **[Default]**
	2	**Virtual Channel ID for Upstream L3-Bound Read Returns** Default Value: 1 Access: R/W
	1:0	**Reserved** Access: RO Format: MBZ

LTISEQ CBE Flush Req

LTISEQ_CBE_FLUSH_REQ - LTISEQ CBE Flush Req

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0D880h

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:16	**Mask bit for CBE flush/inv/disacrd** Access: R/W
	15:3	**Reserved** Access: RO Format: MBZ
	2	**RCU render discard flush indidcation to CBE** Access: R/W
	1	**CBE Invalidation** Access: R/W
	0	**CBE flush** Access: R/W

LTR Extended Capability Header

LTR_CAPHDR_0_2_0_PCI - LTR Extended Capability Header

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00400h

Latency Tolerance Reporting (LTR) capability allows SW to provide latency information to components with upstream ports

DWord	Bit	Description
0	31:20	**Next Capability Offset** Access: RO _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list (0x000 - EOL) Value: 000000000000b — Name: **[Default]**
	19:16	**Version** Default Value: 0001b Access: RO _Custom_GTIReset: BUS Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000011000b Access: RO _Custom_GTIReset: BUS Hardwired to 0018h which is the PCI Express Extended Cap ID for the LTR.

LUT_3D_CTL

LUT_3D_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled

Address:	490A4h-490A7h
Name:	Pipe A 3D LUT Control
ShortName:	LUT_3D_CTL_A
Reset:	soft

Address:	491A4h-491A7h
Name:	Pipe B 3D LUT Control
ShortName:	LUT_3D_CTL_B
Reset:	soft

DWord	Bit	Description
0	31	**LUT 3D Enable** Access: Double Buffered This field enables the 3D LUT. Value / Name: 0b – Disable 1b – Enable **Programming Notes** 3D LUT can be enabled/disabled at any time irrespective of when the pipe is enabled/disabled. Program the Bit 10 of register 420b0h to 1b to ensure that the 3D LUT functionality gets enabled on the first frame after the pipe turns on.
	30	**New LUT Ready** Access: R/W Set This bit must be set to '1' after all the 3D LUT entries are programmed. This bit will get cleared by hardware after the LUT buffer is loaded in to the internal working RAM. Value / Name / Description: 0b – New LUT not ready – New LUT is not yet ready/hardware finished loading the LUT buffer in to internal working RAM. 1b – New LUT Ready – New LUT is ready. **Restriction** Once set, only hardware is allowed to clear this bit. Software cannot clear this bit.

LUT_3D_CTL

	29	**Allow DB Stall** Access: R/W This field controls whether double buffer updates are allowed to be stalled for the 3D LUT registers that are double buffered. Updates to the LUT entries, triggered by New LUT Ready, do not get double buffer stalled. **Value** / **Name** 0b: Not Allowed 1b: Allowed **[Default]**
	28:0	**Reserved** Access: RO Format: MBZ

LUT_3D_DATA

LUT_3D_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	490ACh-490AFh
Name:	Pipe A 3D LUT Data
ShortName:	LUT_3D_DATA_A
Reset:	soft
Address:	491ACh-491AFh
Name:	Pipe B 3D LUT Data
ShortName:	LUT_3D_DATA_B
Reset:	soft

These are the 3D LUT entries. The 3D LUT Index Value indicates the 3D LUT location to be accessed through this register.
Even though this specific register is not double buffered, the 3D LUT table that this register accesses is (i.e. this register updates the table's back buffer). The double buffering point for the table (after DB'ing is armed) is the start of V. Blank or the Pipe is disabled

Restriction
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:0	**LUT 3D Entry** Access: R/W 3D LUT entry value programmed as R10G10B10.

LUT_3D_INDEX

LUT_3D_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	490A8h-490ABh
Name:	Pipe A 3D LUT Index
ShortName:	LUT_3D_INDEX_A
Reset:	soft
Address:	491A8h-491ABh
Name:	Pipe B 3D LUT Index
ShortName:	LUT_3D_INDEX_B
Reset:	soft

This index controls access to the pre-double buffered array of 3D LUT entries.
Even though this specific register is not double buffered, the 3D LUT table that this register accesses is (i.e. this register updates the table's back buffer). The double buffering point for the table (after DB'ing is armed) is the start of V. Blank or the Pipe is disabled

DWord	Bit	Description
0	31:14	**Reserved** Access: RO Format: MBZ
	13	**Index Auto Increment** Access: R/W This field enables the index value to auto increment on each read or write to the data register.. Value: 0b — Name: No Increment Value: 1b — Name: Auto Increment
	12:0	**Index Value** Access: R/W This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. Value: [0,4912] — Name:

MAILBOX0

MAILBOX0 - MAILBOX0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	120800h	
This register contains bits 31:0 of the generic descriptor, fetched from the invalidate queue for GT.		

DWord	Bit	Description
0	31:0	**DATA** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS This field contains bits 31:0 of the generic descriptor, fetched from the invalidate queue for GT.

MAILBOX1

MAILBOX1 - MAILBOX1

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	120804h

This register contains bits 63:32 of the generic descriptor, fetched from the invalidate queue for GT.

DWord	Bit	Description
0	31:0	**DATA** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS This field contains bits 63:32 of the generic descriptor, fetched from the invalidate queue for GT.

MAILBOX2

MAILBOX2 - MAILBOX2		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	120808h	
This register contains bits 95:64 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	**Bit**	**Description**
0	31:0	**DATA** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS This field contains bits 95:64 of the generic descriptor, fetched from the invalidate queue for GT.

MAILBOX3

MAILBOX3 - MAILBOX3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	12080Ch	
This register contains bits 127:96 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	**Bit**	**Description**
0	31:0	**DATA** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS This field contains bits 127:96 of the generic descriptor, fetched from the invalidate queue for GT.

Primary Latency Timer

MLT2_0_2_0_PCI - Primary Latency Timer		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	0000Dh	
The IGD does not support the programmability of the primary latency timer because it does not perform bursts.		
DWord	**Bit**	**Description**
0	7:0	**Primary Latency Timer Count Value** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s.

Primary Tile TileInterrupt

MSTR_TILE_INTR - Primary Tile TileInterrupt

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 190008h

Interrupt bits indicating one of the underlying graphics tiles has an interrupt

DWord	Bit	Description
0	31	**Primary Interrupt** Default Value: 0b Access: R/W _Custom_GTIReset: DEV This is the primary control for graphics interrupts. This must be enabled for any of these interrupts to propagate to PCI device 2 interrupt processing.
	30:4	**Reserved** Access: RO Format: MBZ
	3	**T3 Interrupt** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: DEV
	2	**T2 Interrupt** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: DEV
	1	**T1 Interrupt** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: DEV
	0	**T0 Interrupt** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: DEV

Maximum Latency

MAXLAT_0_2_0_PCI - Maximum Latency		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	0003Fh	
The Integrated Graphics Device has no requirement for the settings of Latency Timers.		
DWord	**Bit**	**Description**
0	7:0	**Maximum Latency Value** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.

Maximum License request in GT C0 window

GT_MAX_LIC_REQ - Maximum License request in GT C0 window

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0A604h
Name:	Maximum License request in GT C0 window
ShortName:	GT_MAX_LIC_REQ

This is RO register that reflects the max count for each of the fields in any given GT C0 window. The values will be reset when in GT C6 and the capture will start all over again in the next GT C0 window

DWord	Bit	Description
0	31:20	**Reserved**
	19:16	**Max Render Slices Requested** Default Value: 0000b Access: RO _Custom_GTIReset: DEV This field stores the maximum slice count that has been requested for in a specific GT C0 window. This field will only get updated if a new request for license, in terms of number of slices, is greater than the previously granted one
	15:11	**Max subslices requested** Access: RO _Custom_GTIReset: DEV This field stores the maximum subslice count that has been requested for in a specific GT C0 window. This field will only get updated if a new request for license, in terms of number of subslices, is greater than the previously granted one
	10:8	**Max Media Slices Requested** Access: RO _Custom_GTIReset: DEV This field stores the maximum Media slice count that has been requested for in a specific GT C0 window. This field will only get updated if a new request for license, in terms of number of Media slices, is greater than the previously granted one
	7:0	**Max EU Pairs Requested** Access: RO _Custom_GTIReset: DEV

Max No Snoop Latency Register

MAX_NOSNP_LAT_0_2_0_PCI - Max No Snoop Latency Register

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00406h

Latency Tolerance Reporting (LTR) capability: Provides the no-maximum snoop latency that a device is permitted to request
SW should set this to the platform's supported max latency or less

DWord	Bit	Description
0	15:13	**Reserved** Access: RO Format: MBZ
	12:10	**Max No Snoop LatencyScale** Default Value: 000b Access: R/W _Custom_GTIReset: BUS Provides a scale for the value contained within the Max no snoop Latency Value field
	9:0	**Max No Snoop LatencyValue** Default Value: 0000000000b Access: R/W _Custom_GTIReset: BUS Max no snoop latency a device is permitted to request

Max Snoop Latency Register

MAX_SNP_LAT_0_2_0_PCI - Max Snoop Latency Register

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00404h

Latency Tolerance Reporting (LTR) capability: Provides the maximum snoop latency that a device is permitted to request
SW should set this to the platform's supported max latency or less

DWord	Bit	Description
0	15:13	**Reserved** Access: RO Format: MBZ
	12:10	**Max Snoop LatencyScale** Default Value: 000b Access: R/W _Custom_GTIReset: BUS Provides a scale for the value contained within the Max snoop Latency Value field
	9:0	**Max Snoop LatencyValue** Default Value: 0000000000b Access: R/W _Custom_GTIReset: BUS Max snoop latency a device is permitted to request

MBC Control Register

MBCTL - MBC Control Register

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 0907Ch

MBC Control Register

DWord	Bit	Description
0	31:18	**ECORSVD** Access: R/W _Custom_GTIReset: BUS ECO purposes Reserved
	17	**U2C Global PMON Enable Override** Default Value: 1b Access: R/W _Custom_GTIReset: BUS U2C Performance Monitor Global Enable Override 0 - U2C Global PMON needs to be enabled for performance monitors to be enabled (default) 1 - Overrride U2C Global PMON Enable is ignored in enabled performance monitor counters
	16	**VCR Fuse Writes as Posted** Access: R/W _Custom_GTIReset: BUS Non-posted fuse fetching is NOT supported. Only posted is allowed (the default). 0 - MBCunit sends VCR Fuse Writes as Non-posted. 1 - MBCunit sends VCR Fuse Writes as posted.
	15:8	**Reserved** Access: RO Format: MBZ
	7	**Disable Wait for SQemtpy in MAE** Access: R/W _Custom_GTIReset: BUS 0 - Wait for SQempty for MAE update Flow. 1 - MBC MAE update FSM does not wait for the SQempty to complete the FSM.
	6	**Reserved**

MBCTL - MBC Control Register

	5:4	**Reserved** Access: RO Format: MBZ
	3	**Context Fetch Needed** Access: R/W _Custom_GTIReset: BUS Context Fetch Needed for Power Exits. 0 - Context Fetch Not Needed. 1 - Context Fetch Needed for Power Exits (CPD Entry).
	2:0	**Reserved** Access: RO Format: MBZ

MBUS_ABOX_CTL

MBUS_ABOX_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45038h-4503Bh
Name:	MBus ABox 0 Control
ShortName:	MBUS_ABOX_CTL0
Reset:	soft
Address:	45048h-4504Bh
Name:	MBus ABox 1 Control
ShortName:	MBUS_ABOX_CTL1
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b: Disabled 1b: Enabled
	30:27	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	26:22	**B2B Transactions Max** Access: R/W This fields indicates the number of back to back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b. 10: **[Default]** [1-31]
	21:20	**BW Credits** Default Value: 1h Access: R/W BW credits are used by the Arbiter to initiate write cycles when performing VRH read-modified-writes to the display buffer.

MBUS_ABOX_CTL

	19:16	**B Credits** Default Value: 1h Access: R/W B credits are used by the Arbiter to initiate read cycles when performing VRH read-modified-writes to the display buffer.
	15:14	**Reserved** Access: RO Format: MBZ
	13	**Regulate B2B Transactions** Access: R/W This field controls the regulation of back to back transactions from this ring stop. 0b: Disable 1b: Enable **[Default]**
	12:8	**BT Credits Pool2** Default Value: 10h Access: R/W BT credits are used by the Arbiter to request trackers from the Display Buffer.
	7:5	**B2B Transactions Delay** Access: R/W This field indicates the number of wait cycles after the maximum back to back transactions is sent. [0-7]: 2: **[Default]**
	4:0	**BT Credits Pool1** Default Value: 10h Access: R/W BT credits are used by the Arbiter to request trackers from the Display Buffer.

MBUS_BBOX_CTL

MBUS_BBOX_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	45040h-45043h
Name:	MBUS Bbox Control
ShortName:	MBUS_BBOX_CTL_S0
Reset:	soft

Address:	45044h-45047h
Name:	MBUS Bbox Control
ShortName:	MBUS_BBOX_CTL_S1
Reset:	soft

Address:	44390h-44393h
Name:	MBUS Bbox Control
ShortName:	MBUS_BBOX_CTL_S2
Reset:	soft

Address:	44394h-44397h
Name:	MBUS Bbox Control
ShortName:	MBUS_BBOX_CTL_S3
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b: Disabled 1b: Enabled
	30:27	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	26:25	**Reserved** Access: RO Format: MBZ

MBUS_BBOX_CTL

24:20 B2B Transactions Max

Access:	R/W

This fields indicates the number of back to back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b.

Value	Name
16	**[Default]**
[1-31]	

19:17 B2B Transactions Delay

Access:	R/W

This field indicates the number of wait cycles after the maximum back to back transactions is sent.

Value	Name
[0-7]	
1	**[Default]**

16 Regulate B2B Transactions

Access:	R/W

This field controls the regulation of back to back transactions from this ring stop.

Value	Name
0b	Disable
1b	Enable **[Default]**

15:0 Reserved

Access:	RO
Format:	MBZ

MBUS_DBOX_CTL

MBUS_DBOX_CTL

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled

Address:	7003Ch-7003Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_A
Reset:	soft

Address:	7103Ch-7103Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_B
Reset:	soft

Address:	7203Ch-7203Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_C
Reset:	soft

Address:	7303Ch-7303Fh
Name:	Pipe MBus DBox Control
ShortName:	PIPE_MBUS_DBOX_CTL_D
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b – Disabled 1b – Enabled
	30:27	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	26:25	**Reserved** Access: RO Format: MBZ

MBUS_DBOX_CTL

24:20 B2B Transactions Max

Access:	Double Buffered

This fields indicates the number of back to back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b.

Value	Name
16	**[Default]**
[1-31]	

19:17 B2B Transactions Delay

Access:	Double Buffered

This field indicates the number of wait cycles after the maximum back to back transactions is sent.

Value	Name
[0-7]	
1	**[Default]**

16 Regulate B2B Transactions

Access:	Double Buffered

This field controls the regulation of back to back transactions from this ring stop.

Value	Name
0b	Disable
1b	Enable **[Default]**

15:14 BW Credits

Access:	Double Buffered

BW credits are used by the display pipe to write color clear data to DBUF.

Value	Name
1h	**[Default]**

13 Reserved

Access:	RO
Format:	MBZ

12:8 B Credits

Access:	Double Buffered

B credits are used by the display pipe to request data from display buffer.

Value	Name
0Ch	**[Default]**

7:5 Reserved

Access:	RO
Format:	MBZ

MBUS_DBOX_CTL

	4	**Reserved** Access: RO Format: MBZ
	3:0	**A Credits** Access: Double Buffered A credits are used by the display pipe to make data/TLB/VTd/MCS requests to Arbiter. **Value** / **Name** 2h / 2 credits **[Default]**

MBUS_UBOX_CTL

MBUS_UBOX_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4503Ch-4503Fh
Name:	MBus UBox 0 Control
ShortName:	MBUS_UBOX_CTL0
Reset:	soft

DWord	Bit	Description
0	31	**Status** Access: RO This field indicates if the box is enabled. 0b – Disabled 1b – Enabled
	30:27	**Ring Stop Address** Access: RO This field indicates the address of the box in the ring.
	26:25	**Reserved** Access: RO Format: MBZ
	24:20	**B2B Transactions Max** Access: R/W This fields indicates the number of back to back transactions that can be added to either to top or bottom of the ring when 'Regulate Transactions' bit is 1b. 16 – **[Default]** [1-31]
	19:17	**B2B Transactions Delay** Access: R/W This field indicates the number of wait cycles after the maximum back to back transactions is sent. [0-7] 1 – **[Default]**

MBUS_UBOX_CTL

16	**Regulate B2B Transactions** Access: R/W This field controls the regulation of back to back transactions from this ring stop. 0b: Disable 1b: Enable **[Default]**
15:7	**Reserved** Access: RO Format: MBZ
6:4	**KVM Sprite A Credits** Default Value: 1 Access: R/W A Credits used by KVM to make data requests to Arbiter.
3	**Reserved** Access: RO Format: MBZ
2:0	**VGA B Credits** Default Value: 4 Access: R/W B credits used by VGA to request data from Display Buffer.

MCPG1 Hysteresis Time Free

OAG_MCPG1_HYSTERESIS_TIME_FREE - MCPG1 Hysteresis Time Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBB4h

This register counts the time that MCPG hysteresis time is accumulating for media slice 1.This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

MCR Packet Control

MCRPKT_CTRL - MCR Packet Control

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIReset: BUS

Address: 00FDCh-00FDFh

DWord	Bit	Description
0	31	**MULTICAST** Access: R/W Value determines the multicast value driven to MCR. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request. Value: 1b — Name: Multicast **[Default]** Value: 0b — Name: Unicast **Programming Notes** SLICEID and DUAL_SUBSLICEID are used in Unicast but ignored for Multicast.
	30:27	**SLICEID** Access: R/W Value determines the slice ID driven to MCR. Value: 0000b — Name: **[Default]** Value: [0001b,1111b] — Name: **Programming Notes** Values must be in range of slices and subslices in the configuration.
	26:24	**DUAL_SUBSLICEID** Access: R/W Value determines the dual-subslice ID (or l3_bank) driven to MCR. Value: 000b — Name: **[Default]** Value: [001b,111b] — Name: **Programming Notes** Values must be in range of slices and subslices in the configuration.

MCRPKT_CTRL - MCR Packet Control		
	23:0	**Reserved** Access: RO Format: MBZ

MCR Packet Control 0

MCRPKT_CTRL_MCFG - MCR Packet Control 0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	00FD0h-00FD3h

DWord	Bit	Description
0	31	**MULTICAST MCFG** Default Value: 1b Access: R/W Value determines the multicast value driven to MCR for accesses to MCFG. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.
	30:27	**SLICEID MCFG** Default Value: 0000b Access: R/W Value driven on packet field Slice ID targeting MCFG.
	26:24	**DUAL_SUBSLICEID MCFG** Default Value: 000b Access: R/W Value determines the SQIDI ID driven on packet field Dual-Subslice ID targeting MCFG.
	23:0	**Reserved** Access: RO Format: MBZ

MCR Packet Control 1

MCRPKT_CTRL_SFHW - MCR Packet Control 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00FD4h-00FD7h	

DWord	Bit	Description
0	31	**MULTICAST SF HW** Default Value: 1b Access: R/W Value determines the multicast value driven to MCR for accesses to SF from HW source. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.
	30:27	**SLICEID SF HW** Default Value: 0000b Access: R/W Value driven on packet field Slice ID targeting SF from HW source.
	26:24	**DUAL_SUBSLICEID SF HW** Default Value: 000b Access: R/W Value determines the SQIDI ID driven on packet field Dual-Subslice ID targeting SF from HW source.
	23:0	**Reserved** Access: RO Format: MBZ

MCR Packet Control 2

MCRPKT_CTRL_SF - MCR Packet Control 2		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00FD8h-00FDBh	

DWord	Bit	Description
0	31	**MULTICAST SF** Default Value: 1b Access: R/W Value determines the multicast value driven to MCR for accesses to SF. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.
	30:27	**SLICEID SF** Default Value: 0000b Access: R/W Value driven on packet field Slice ID targeting SF.
	26:24	**DUAL_SUBSLICEID SF** Default Value: 000b Access: R/W Value determines the SQIDI ID driven on packet field Dual-Subslice ID targeting SF.
	23:0	**Reserved** Access: RO Format: MBZ

MCR Packet Control 4

MCRPKT_CTRL_GAM - MCR Packet Control 4		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00FE0h-00FE3h	
Steering value for GAM MMIO access. If the Host MMIO access is to UID=GAM, this steering register is used.		

DWord	Bit	Description
0	31	**MULTICAST** Default Value: 1b Access: R/W Value determines the multicast value driven to MCR. 0 - not multicast 1 - multicast The usage model is that the value is returned to the default (1), after completion of the unicast request.
	30:27	**SLICEID** Default Value: 0001b Access: R/W Value determines the slice ID driven to MCR.
	26:24	**DUAL_SUBSLICEID** Default Value: 000b Access: R/W Value determines the dual-subslice ID. Not used for GAM MMIO accesses.
	23:0	**Reserved** Access: RO Format: MBZ

MDRB Context Base 1

MDRB_CTXBASE1 - MDRB Context Base 1

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00DC8h

RC6 Save Location
NOTE: This register is not used since MDRB unit no longer exists.

DWord	Bit	Description
0	31:6	**MDRB Memory Base Low** Access: R/W Lock _Custom_GTIReset: BUS This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1
	5:1	**Reserved** Access: RO Format: MBZ
	0	**Ctx Base is Enabled** Access: R/W Lock _Custom_GTIReset: BUS 1'b0 : The MDRB base has not been enabled, so don't do the MDRB context save (This is default value and BIOS has to program it to enable context save) 1'b1 : The MDRB base has been enabled, so go ahead with the context save

MDRB Context Base 2

MDRB_CTXBASE2 - MDRB Context Base 2		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00DCCh	
RC6 Base Location NOTE: This register is not used since MDRB unit is no more there.		
DWord	**Bit**	**Description**
0	31:0	**MDRB Memory Base High** Access: R/W Lock _Custom_GTIReset: BUS This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1

MED0HCP0PowerGoodDelay

MED0HCP0_PG_DLY - MED0HCP0PowerGoodDelay		
Register Space:	MMIO: GTTMMADR	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	**Bit**	**Description**
0	31:16	**Power Good Delay** Default Value: 00C8h PWRGOOD_DLY Value Access: R/W
	15:0	**RAMP Delay** Default Value: 00C8h RAMP_DLY Value Access: R/W

MED0MFX0PowerGoodDelay

MED0MFX0_PG_DLY - MED0MFX0PowerGoodDelay		
Register Space:	MMIO: GTTMMADR	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		

DWord	Bit	Description
0	31:16	**Power Good Delay** Default Value: 00C8h PWRGOOD_DLY Value Access: R/W
	15:0	**RAMP Delay** Default Value: 00C8h RAMP_DLY Value Access: R/W

MED0PowerGoodDelay

MED0_PG_DLY - MED0PowerGoodDelay		
Register Space:	MMIO: GTTMMADR	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		

DWord	Bit	Description
0	31:16	**Power Good Delay** Default Value: 00C8h PWRGOOD_DLY Value Access: R/W
	15:0	**RAMP Delay** Default Value: 00C8h RAMP_DLY Value Access: R/W

MED1HCP0PowerGoodDelay

MED1HCP0_PG_DLY - MED1HCP0PowerGoodDelay		
Register Space:	MMIO: GTTMMADR	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	**Bit**	**Description**
0	31:16	**Power Good Delay** Default Value: 00C8h PWRGOOD_DLY Value Access: R/W
	15:0	**RAMP Delay** Default Value: 00C8h RAMP_DLY Value Access: R/W

MED1MFX0PowerGoodDelay

MED1MFX0_PG_DLY - MED1MFX0PowerGoodDelay		
Register Space:	MMIO: GTTMMADR	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		
DWord	**Bit**	**Description**
0	31:16	**Power Good Delay** Default Value: 00C8h PWRGOOD_DLY Value Access: R/W
	15:0	**RAMP Delay** Default Value: 00C8h RAMP_DLY Value Access: R/W

MED1PowerGoodDelay

MED1_PG_DLY - MED1PowerGoodDelay		
Register Space:	MMIO: GTTMMADR	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
IA/Context savable by MGSR/punit		

DWord	Bit	Description
0	31:16	**Power Good Delay** Default Value: 00C8h PWRGOOD_DLY Value Access: R/W
	15:0	**RAMP Delay** Default Value: 00C8h RAMP_DLY Value Access: R/W

Media BONUS2 Reg

MEDIASPCBONUS2 - Media BONUS2 Reg		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 24098h		
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

MEDIASPCBONUS2 - Media BONUS2 Reg

	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Media Die Recovery

MED_DIE_RECOVERY - Media Die Recovery

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	12298h
Name:	VCS Media Die Recovery
ShortName:	VCS_MED_DIE_RECOVERY

This register is stored in the VCS but is used in the HWM unit. This register programs the die recovery override and engine ID's.

DWord	Bit	Description
0	31:12	**Reserved** Access: RO Format: MBZ
	11:9	**Forced Next Engine ID** Access: R/W This field is the next engine ID.
	8	**Force Next Engine ID** Access: R/W The bit forces the next engine ID.
	7:4	**Reserved** Access: RO Format: MBZ
	3:1	**Forced Previous Engine ID** Access: R/W This field is the previous engine ID.
	0	**Force Previous Engine ID** Access: R/W The bit forces the previous engine ID.

Media FIFO Messaging Register for Shadow Register Unit

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	080E4h
Name:	Media FIFO Messaging Register for Shadow Register Unit
ShortName:	MSG_FIFO_MGSR_MEDIA

Register that has the ACK information, back from MGSR as to whether a specific VD/VE Box has been blocked/unblocked
0 -- Box has been blocked
1 -- Box has been unblocked
Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To set bit0, for example, the data would be 0x0001_0001.
To clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16.
Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:12	**Reserved** Access: RO Format: MBZ
	11	**Acknowledge that Media FIFO has been Blocked for VEBOX3** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VEBOX3 1'b0 : Media FIFO Block Ack for VEBOX3(default) 1'b1 : Media FIFO Unblock Ack VEBOX3 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	10	**Acknowledge that Media FIFO has been Blocked for VEBOX2** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VEBOX2 1'b0 : Media FIFO Block Ack for VEBOX2(default) 1'b1 : Media FIFO Unblock Ack VEBOX2 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	9	**Acknowledge that Media FIFO has been Blocked for VEBOX1**

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

		Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VEBOX1 1'b0 : Media FIFO Block Ack for VEBOX1(default) 1'b1 : Media FIFO Unblock Ack VEBOX1 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	8	**Acknowledge that Media FIFO has been Blocked for VEBOX0** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VEBOX0 1'b0 : Media FIFO Block Ack for VEBOX0(default) 1'b1 : Media FIFO Unblock Ack VEBOX0 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	7	**Acknowledge that Media FIFO has been Blocked for VDBOX7** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VDBOX7 1'b0 : Media FIFO Block Ack for VDBOX7(default) 1'b1 : Media FIFO Unblock Ack VDBOX7 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	6	**Acknowledge that Media FIFO has been Blocked for VDBOX6** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VDBOX6 1'b0 : Media FIFO Block Ack for VDBOX6(default) 1'b1 : Media FIFO Unblock Ack VDBOX6 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	5	**Acknowledge that Media FIFO has been Blocked for VDBOX5** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VDBOX5 1'b0 : Media FIFO Block Ack for VDBOX5(default) 1'b1 : Media FIFO Unblock Ack VDBOX5 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.

MSG_FIFO_MGSR_MEDIA - Media FIFO Messaging Register for Shadow Register Unit

	4	**Acknowledge that Media FIFO has been Blocked for VDBOX4** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VDBOX4 1'b0 : Media FIFO Block Ack for VDBOX4(default) 1'b1 : Media FIFO Unblock Ack VDBOX4 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	3	**Acknowledge that Media FIFO has been Blocked for VDBOX3** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VDBOX3 1'b0 : Media FIFO Block Ack for VDBOX3(default) 1'b1 : Media FIFO Unblock Ack VDBOX3 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	2	**Acknowledge that Media FIFO has been Blocked for VDBOX2** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VDBOX2 1'b0 : Media FIFO Block Ack for VDBOX2(default) 1'b1 : Media FIFO Unblock Ack VDBOX2 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	1	**Acknowledge that Media FIFO has been Blocked for VDBOX1** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VDBOX1 1'b0 : Media FIFO Block Ack for VDBOX1(default) 1'b1 : Media FIFO Unblock Ack VDBOX1 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.
	0	**Acknowledge that Media FIFO has been Blocked for VDBOX0** Access: R/W _Custom_GTIReset: BUS Acknowledge that MEDIA FIFO has been Blocked for VDBOX0 1'b0 : Media FIFO Block Ack for VDBOX0(default) 1'b1 : Media FIFO Unblock Ack VDBOX0 Note that the block request goes to MGSR, and MGSR responds to GPM with the blocked ack.

Media PFET control register with lock

MEDIASPCPFETCTL - Media PFET control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24088h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of MEDIA PFETCTL register are R/W 1 = All bits of MEDIA PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.

MEDIASPCPFETCTL - Media PFET control register with lock

	21:19	**Delay from enabling secondary PFETs to power good.** Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns **Value**: 101b — **Name**: **[Default]**
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock _Custom_GTIReset: BUS Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock _Custom_GTIReset: BUS PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Media Power Context Save request

MEDIAPGCTXREQ - Media Power Context Save request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24084h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Media Power Down FSM control register with lock

MEDIASPCPOWERDNFSMCTL - Media Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24090h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of MEDIA1 POWERDNFSMCTL register are R/W 1 = All bits of MEDIA1 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow

MEDIASPCPOWERDNFSMCTL - Media Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

MEDIASPCPOWERDNFSMCTL - Media Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Media Power Gate Control Request

MEDIAPGCTLREQ - Media Power Gate Control Request

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24080h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS Media1 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS Media1 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Media Power on FSM control register with lock

MEDIASPCPOWERUPFSMCTL - Media Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2408Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of MEDIA1 POWERUPFSMCTL register are R/W 1 = All bits of MEDIA1 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Firewall OFF

MEDIASPCPOWERUPFSMCTL - Media Power on FSM control register with lock

	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Media unit Level Clock Gating override during rstflow 94B0

MEDMISCCP94B0 - Media unit Level Clock Gating override during rstflow 94B0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	094B0h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**misccp Clock Gating Disable during rstflow** Access: R/W _Custom_GTIReset: BUS misccp Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

MEMRR_BASE_LSB

MEMRR_BASE_LSB - MEMRR_BASE_LSB

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	108340h

The EMRR range is used to protect Xucode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address. It functions in tandem with the EMRR mask register.

DWord	Bit	Description
0	31:12	**RANGE_BASE** Default Value: 0000000h Access: RO _Custom_GTIReset: BUS This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.
	11:4	**Reserved** Access: RO Format: MBZ
	3	**CONFIGURED** Default Value: 0h Access: RO _Custom_GTIReset: BUS This bitfield is required to enable the PRMRR range
	2:0	**Reserved** Access: RO Format: MBZ

MEMRR_BASE_MSB

MEMRR_BASE_MSB - MEMRR_BASE_MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	108344h	
The EMRR range is used to protect Xucode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address. It functions in tandem with the EMRR mask register.		
DWord	**Bit**	**Description**
0	31:0	**RANGE_BASE** Default Value: 000h Access: RO _Custom_GTIReset: BUS This field corresponds to bits 63:12 of the base address memory range which is allocated to EMRR memory.

MEMRR_MASK_LSB

MEMRR_MASK_LSB - MEMRR_MASK_LSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	108380h	
This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.		
DWord	**Bit**	**Description**
0	31:12	**RANGE_BASE** Default Value: 0000000h Access: RO _Custom_GTIReset: BUS This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.
	11	**RANGE_EN** Default Value: 0b Access: RO _Custom_GTIReset: BUS Indicates whether the EMRR range is enabled and valid.
	10	**LOCK** Default Value: 0b Access: RO _Custom_GTIReset: BUS Setting this bit locks all writeable settings in this register, including itself.
	9:0	**Reserved** Access: RO Format: MBZ

MEMRR_MASK_MSB

MEMRR_MASK_MSB - MEMRR_MASK_MSB	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	108384h

This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.

DWord	Bit	Description
0	31:0	**RANGE_MASK** Default Value: 000h Access: RO _Custom_GTIReset: BUS This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.

MESH Invocation Counter

MESH_INVOCATION_COUNT - MESH Invocation Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	026E0h
Name:	MESH Invocation Counter
ShortName:	MESH_INVOCATION_COUNT

The **MESH_INVOCATION_COUNT** accumulates API-level MeshShader invocations dispatched by the pipeline. For each MeshShader ThreadGroup dispatched, this register is incremented by the thread group size. This register does not count EU thread dispatches.
SW shall comprehend that a pipeline flush is required to ensure that preceding MeshShader work is included in the register value.

DWord	Bit	Description
0	63:32	**MESH Invocation Count UDW** Access: R/W Number of patch objects processed by the MESH stage. Updated only when MESH Enable and MESH Statistics Enable are set in 3DSTATE_MESH
	31:0	**MESH Invocation Count LDW** Access: R/W Number of patch objects processed by the MESH stage. Updated only when MESH Enable and MESH Statistics Enable are set in 3DSTATE_MESH

MESH Invocation Counter per Slice

MESH_INVOCATION_COUNT_SLICE - MESH Invocation Counter per Slice

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

Address:	065C0h-065C7h
Name:	MESH Invocation Counter per Slice
ShortName:	MESH_INVOCATION_COUNT_SLICE_SVGUNIT

Address:	175C0h-175C7h
Name:	MESH Invocation Counter per Slice
ShortName:	MESH_INVOCATION_COUNT_SLICE_SVGRUNIT

The**MESH_INVOCATION_COUNT** accumulatesAPI-level MeshShader invocations dispatched by the pipeline per Gslice. For each MeshShader ThreadGroup dispatched in that Gslice, this register is incremented by the thread group size. This register doesnotcount EU thread dispatches.
SW shall comprehend that a pipeline flush is required to ensure that preceding MeshShader work is included in the register value.

DWord	Bit	Description
0..1	63:32	**MESH Invocation Count UDW in Slice** Access: R/W Number of patch objects processed by the MESH stage within the slice. Updated only when MESH Enable and MESH Statistics Enable are set in 3DSTATE_MESH
	31:0	**MESH Invocation Count LDW in Slice** Access: R/W Number of patch objects processed by the MESH stage within the slice. Updated only when MESH Enable and MESH Statistics Enable are set in 3DSTATE_MESH

Message Address

MA_0_2_0_PCI - Message Address		
Register Space:	PCI: 0/2/0	
Size (in bits):	64	
Address:	000B0h	
This register contains the Message Address for MSIs sent by the device.		
DWord	**Bit**	**Description**
0	63:32	**Message Address Field MSB** Default Value: 0x00000000 Access: R/W _Custom_GTIReset: BUS Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
	31:2	**Message Address Field LSB** Default Value: 0x00000000 Access: R/W _Custom_GTIReset: BUS Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
	1:0	**Force Dword Align** Default Value: 00b Access: RO _Custom_GTIReset: BUS Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.

Message Control

MC_0_2_0_PCI - Message Control

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	000AEh

Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

DWord	Bit	Description
0	15:9	**Reserved** Access: RO Format: MBZ
	8	**Per Vector Mask Capable** Default Value: 1b Access: RO _Custom_GTIReset: BUS SR-IOV requires this capability.
	7	**64 Bit Capable** Access: RO _Custom_GTIReset: BUS Description: Hardwired to 01 to indicate that the function is capable of generating a 64-bit memory address. Value: 1b — Name: **[Default]**
	6:4	**Multiple Message Enable** Default Value: 000b Access: R/W _Custom_GTIReset: BUS System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. Value: Number of requests000: 1001: 2010: 4011: 8100: 16101: 32110: Reserved111: Reserved

MC_0_2_0_PCI - Message Control

	3:1	**Multiple Message Capable** Default Value: 000b Access: RO _Custom_GTIReset: BUS System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.
	0	**MSI Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Controls the ability of this device to generate MSIs.

Message Data

MD_0_2_0_PCI - Message Data		
Register Space:	PCI: 0/2/0	
Size (in bits):	16	
Address:	000B8h	
This register contains the Message Data for MSIs sent by the device.		
DWord	**Bit**	**Description**
0	15:0	**MESSDATA** Default Value: 0000000000000000b Access: R/W _Custom_GTIReset: BUS Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

Message Signaled Interrupts Capability ID

MSI_CAPID_0_2_0_PCI - Message Signaled Interrupts Capability ID

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	000ACh

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

DWord	Bit	Description
0	15:8	**Pointer to Next Capability** Default Value: 11010000b Access: RO _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list.
	7:0	**Capability ID** Default Value: 00000101b Access: RO _Custom_GTIReset: BUS This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.

MFC_AVC_CABAC_INSERTION_COUNT

AVC_CABAC_INSERTION_COUNT - MFC_AVC_CABAC_INSERTION_COUNT	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	128ACh

This register stores the count in bytes of **CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.**

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Insertion Count** Access: RO Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter

MFC_VIN_AVD_ERROR_CNTR - MFC_AVC Bitstream Decoding Front-End Parsing Logic Error Counter		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	12804h	
DWord	**Bit**	**Description**
0 avd_error_flagsR[31:0]	31:0	**Reserved** Access: RO Format: MBZ

MFC Image Status Control

MFC_IMAGE_STATUS_CONTROL - MFC Image Status Control		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128B8h	
This register stores the suggested data for next frame in multi-pass.		
DWord	**Bit**	**Description**
0	31:24	**Cumulative slice delta QP** Access: RO
	23:16	**QP Value** Access: RO suggested slice QP delta value for frame level Rate control. This value can be +ve or -ve
	15	**QP-Polarity Change** Access: RO Cumulative slice delta QP polarity change.
	14:13	**Num-Pass Polarity Change** Access: RO Number of passes after cumulative slice delta QP polarity changes.
	12	**Reserved**
	11:8	**Total Num-Pass** Access: RO
	7:4	**Reserved** Access: RO Format: MBZ
	3	**Missing Huffman Code** Access: RO Jpeg HW encoder reports if Huffman table entry is missing.
	2	**Panic** Access: RO Panic triggered to avoid too big packed file.
	1	**Frame Bit Count** Access: RO Frame Bit count over-run/under-run flag
	0	**Max Conformance Flag** Access: RO Max Macroblock conformance flag or Frame Bit count over-run/under-run

MFC Image Status Mask

MFC_IMAGE_STATUS_MASK - MFC Image Status Mask		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128B4h	
This register stores the image status(flags).		
DWord	**Bit**	**Description**
0	31:0	**Control Mask** Access: RO Control Mask for dynamic frame repeat.

MFC QP Status Count

MFC_QUP_CT - MFC QP Status Count		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128BCh	
This register stores the suggested QP COUNTS in multi-pass.		
DWord	**Bit**	**Description**
0	31:24	**Cumulative QP Adjust** Access: RO Format: U8 Cumulative QP adjustment after multiple passes. If there is no need to multi-pass, this value would be zero. (This is in sign magnitude form).
	23:0	**Cumulative QP** Access: RO Format: U24 Cumulative QP for all MB of a Frame (Can be used for computing average QP).

MFD Error Status

MFD_ERROR_STATUS - MFD Error Status	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C0800h
ShortName:	MFD_ERROR_STATUS_VCS0
Description:	For VDBox0
Address:	1C4800h
ShortName:	MFD_ERROR_STATUS_VCS1
Description:	For VDBox1
Address:	1D0800h
ShortName:	MFD_ERROR_STATUS_VCS2
Description:	For VDBox2
Address:	1D4800h
ShortName:	MFD_ERROR_STATUS_VCS3
Description:	For VDBox3
Address:	1E0800h
ShortName:	MFD_ERROR_STATUS_VCS4
Description:	For VDBox4
Address:	1E4800h
ShortName:	MFD_ERROR_STATUS_VCS5
Description:	For VDBox5
Address:	1F0800h
ShortName:	MFD_ERROR_STATUS_VCS6
Description:	For VDBox6
Address:	1F4800h
ShortName:	MFD_ERROR_STATUS_VCS7
Description:	For VDBox7

This register stores the error status flags and count reports by the bit-stream decoder. This register is not part of hardware context save and restore. Driver should read the content prior to starting a new batch/frame.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ

MFD_ERROR_STATUS - MFD Error Status

	19:16	**AVC Short Format Error Flags** Access: RO Exists If: // AVC Short Format == Ture Bit-stream error detected by VLD short format bit-stream decoder**.** These flags are reset at the beginning of a frame and updated until starting of another frame. [19] Slice Type SE Error Flag Invalid Slice Type SE [18] MMCO SE Error Flag Invalid memory management control operation SE. MMCO Loop does not end (mmco control != 0) even after all MMCO SEs are decoded OR MMCO SEs are still being decoded and MMCO SE loop end (mmco control == 0) is hit [17] Reordering IDC Error Flag Syntax Element modification_of_pic_nums_idc >= 6 OR modification_of_pic_nums_idc != 3 (end of reordering loop) but reordering count has already hit maximum value [16] Premature bitstream end is hit before finishing slice header decode
	15:0	**Bit-stream Error flags** Access: RO Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True Bitstream error detected by the VLD bit-stream decoder. These flags are reset at the beginning of a frame and updated until starting of another frame. AVC CAVLC: Please refer to AVC CAVLC table for each bit field AVC CABAC: Please refer to AVC CABAC table for each bit field VC1: Please refer to VC1 table for each bit field MPEG2: Please refer to MPEG2 table for each bit field

MFD Picture Parameter

MFD_PICTURE_PARAM - MFD Picture Parameter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	1C0820h
ShortName:	MFD_PICTURE_PARAM_VCS0
Description:	For VDbox0

Address:	1C4820h
ShortName:	MFD_PICTURE_PARAM_VCS1
Description:	For VDbox1

Address:	1D0820h
ShortName:	MFD_PICTURE_PARAM_VCS2
Description:	For VDbox2

Address:	1D4820h
ShortName:	MFD_PICTURE_PARAM_VCS3
Description:	For VDbox3

Address:	1E0820h
ShortName:	MFD_PICTURE_PARAM_VCS4
Description:	For VDbox4

Address:	1E4820h
ShortName:	MFD_PICTURE_PARAM_VCS5
Description:	For VDbox5

Address:	1F0820h
ShortName:	MFD_PICTURE_PARAM_VCS6
Description:	For VDbox6

Address:	1F4820h
ShortName:	MFD_PICTURE_PARAM_VCS7
Description:	For VDbox7

DWord	Bit	Description
0	31:0	**Reserved** Access: RO Format: MBZ

MFX Frame BitStream SE/BIN Count

MFX_SE_BIN_CT - MFX Frame BitStream SE/BIN Count	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C086Ch
ShortName:	MFX_SE_BIN_CT_VCS0
Description:	For VDBox0
Address:	1C486Ch
ShortName:	MFX_SE_BIN_CT_VCS1
Description:	For VDBox1
Address:	1D086Ch
ShortName:	MFX_SE_BIN_CT_VCS2
Description:	For VDBox2
Address:	1D486Ch
ShortName:	MFX_SE_BIN_CT_VCS3
Description:	For VDBox3
Address:	1E086Ch
ShortName:	MFX_SE_BIN_CT_VCS4
Description:	For VDBox4
Address:	1E486Ch
ShortName:	MFX_SE_BIN_CT_VCS5
Description:	For VDBox5
Address:	1F086Ch
ShortName:	MFX_SE_BIN_CT_VCS6
Description:	For VDBox6
Address:	1F486Ch
ShortName:	MFX_SE_BIN_CT_VCS7
Description:	For VDBox7

This register stores the number of BINs (AVC CABAC) and SEs (CAVLD, VLD) decoded in a frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:0	**MFX Frame Bit-stream SE/BIN Count** Access: RO Total number of BINs/SEs decoded in current frame. This number is used with frame performance count to derive Bin/clk or SE/clk.

MFX Frame Macroblock Count

MFX_MB_COUNT - MFX Frame Macroblock Count

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C0868h
ShortName:	MFX_MB_COUNT_VCS0
Description:	For VDBox0
Address:	1C4868h
ShortName:	MFX_MB_COUNT_VCS1
Description:	For VDBox1
Address:	1D0868h
ShortName:	MFX_MB_COUNT_VCS2
Description:	For VDBox2
Address:	1D4868h
ShortName:	MFX_MB_COUNT_VCS3
Description:	For VDBox3
Address:	1E0868h
ShortName:	MFX_MB_COUNT_VCS4
Description:	For VDBox4
Address:	1E4868h
ShortName:	MFX_MB_COUNT_VCS5
Description:	For VDBox5
Address:	1F0868h
ShortName:	MFX_MB_COUNT_VCS6
Description:	For VDBox6
Address:	1F4868h
ShortName:	MFX_MB_COUNT_VCS7
Description:	For VDBox7

This register stores the number of Macro-blocks decoded/encoded in current frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:20	**MBZ** Access: RO Exists If: // JPEG == True Format: MBZ

MFX_MB_COUNT - MFX Frame Macroblock Count

		This field is currently reserved
	31:16	**Intra MB Count** Access: RO Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True Format: U16
	19:0	**JPEG Block Count** Access: RO Exists If: // JPEG == True Format: U20 This 20-bit field indicates the number of 8x8 blocks within the JPEG frame. This field is clear at the start of decoding a new frame.
	15:0	**Number of MB Concealment** Access: RO Exists If: // AVC CAVLC, AVC CABAC, VC1 and MPEG2 == True This 16-bit field indicates the number of MB is concealed by hardware. This field is clear at the start of decoding a new frame.

MFX Frame Row-Stored/BitStream Read Count

MFX_ROW_PER_BS_COUNT - MFX Frame Row-Stored/BitStream Read Count

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	12880h

This register stores the total number of row-stored/bit-stream read requests made by the pre-fetch engine per frame. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**MFX row-stored/bit-stream read request Count** Access: RO Total number of row-stored/bit-stream read requests sent by the memory pre-fetch engine per frame.

MFX PAK MPEG TS STATUS

MFX_PAK_MPEG_TS_STATUS - MFX PAK MPEG TS STATUS

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	12950h

This register stores MPEGTS packet status information

DWord	Bit	Description
0	31:28	**Next Continuity Center** Access: RO Format: U4 HW will update the continuity counter the next MPEGTS packet stream for this stream ID needs to place in the bitstream.
	27:16	**Reserved** Access: RO Format: MBZ
	15:0	**MPEGTS Packet Count** Access: RO Format: U16 This field counts the total number of written MPEGTS video packets by PAK HW. The PES header (which contains the PCR and PTS value) is included in this count as well.

MFX Pipeline Status Flags

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C0838h
ShortName:	MFX_STATUS_FLAGS_VCS0
Description:	For VDBox0
Address:	1C4838h
ShortName:	MFX_STATUS_FLAGS_VCS1
Description:	For VDBox1
Address:	1D0838h
ShortName:	MFX_STATUS_FLAGS_VCS2
Description:	For VDBox2
Address:	1D4838h
ShortName:	MFX_STATUS_FLAGS_VCS3
Description:	For VDBox3
Address:	1E0838h
ShortName:	MFX_STATUS_FLAGS_VCS4
Description:	For VDBox4
Address:	1E4838h
ShortName:	MFX_STATUS_FLAGS_VCS5
Description:	For VDBox5
Address:	1F0838h
ShortName:	MFX_STATUS_FLAGS_VCS6
Description:	For VDBox6
Address:	1F4838h
ShortName:	MFX_STATUS_FLAGS_VCS7
Description:	For VDBox7

This register stores the various pipeline status flags. This register is not part of hardware context save and restore.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

16	**MFX Active** Access: RO Frame decoding/encoding is in progress. Set on frame start; clear on frame end.
15:10	**Reserved** Access: RO Format: MBZ
9	**Streamout Enable** Access: RO
8	**Reserved** Access: RO
7	**Post Deblocking Mode Enable** Access: RO
6	**Pre Deblocking Mode Enable** Access: RO
5	**Decoder Mode Select** Access: RO

Value	Name
0	Configure the MFD Engine for VLD Mode
1	Configure the MFD Engine for IT Mode

4	**Codec Select** Access: RO

Value	Name
0	Decode
1	Encode

3:2	**Video Mode** Access: RO

Value	Name
00b	MPEG2
01b	VC1
10b	AVC
11b	JPEG

MFX_STATUS_FLAGS - MFX Pipeline Status Flags

	1	**Decoder Short Format Mode** Access: RO Value / Name / Description 0 / / AVC/VC1 Short Format Mode is in use 1 / / AVC/VC1 Long Format Mode is in use
	0	**Stitch Mode** Access: RO Value / Name / Description 0b / / Not in Stitch Mode 1b / / In the Special Stitch Mode

MFX SFC LOCK Request

MFX_SFC_LOCK_REQUEST - MFX SFC LOCK Request

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	1C088Ch
ShortName:	MFX_SFC_LOCK_REQUEST_VCS0
Description:	For VDBox0

Address:	1C488Ch
ShortName:	MFX_SFC_LOCK_REQUEST_VCS1
Description:	For VDBox1

Address:	1D088Ch
ShortName:	MFX_SFC_LOCK_REQUEST_VCS2
Description:	For VDBox2

Address:	1D488Ch
ShortName:	MFX_SFC_LOCK_REQUEST_VCS3
Description:	For VDBox3

Address:	1E088Ch
ShortName:	MFX_SFC_LOCK_REQUEST_VCS4
Description:	For VDBox4

Address:	1E488Ch
ShortName:	MFX_SFC_LOCK_REQUEST_VCS5
Description:	For VDBox5

Address:	1F088Ch
ShortName:	MFX_SFC_LOCK_REQUEST_VCS6
Description:	For VDBox6

Address:	1F488Ch
ShortName:	MFX_SFC_LOCK_REQUEST_VCS7
Description:	For VDBox7

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**MFX_SFC_Forced_Lock** Access: R/W Format: U1

MFX_SFC_LOCK_REQUEST - MFX SFC LOCK Request		
		This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells MFX that a software reset is going to happen. MFX then issues a forced lock to SFC. If SFC is currently locked to MFX, SFC should not unlock itself from MFX. If SFC is NOT currently locked to MFX, SFC should not accept the lock request from MFX. Driver needs to clear this bit after the software reset sequence is complete.

MFX SFC LOCK Status

MFX_SFC_LOCK_STATUS - MFX SFC LOCK Status	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C0890h
ShortName:	MFX_SFC_LOCK_STATUS_VCS0
Description:	For VDbox0
Address:	1C4890h
ShortName:	MFX_SFC_LOCK_STATUS_VCS1
Description:	For VDbox1
Address:	1D0890h
ShortName:	MFX_SFC_LOCK_STATUS_VCS2
Description:	For VDBox2
Address:	1D4890h
ShortName:	MFX_SFC_LOCK_STATUS_VCS3
Description:	For VDBox3
Address:	1E0890h
ShortName:	MFX_SFC_LOCK_STATUS_VCS4
Description:	For VDBox4
Address:	1E4890h
ShortName:	MFX_SFC_LOCK_STATUS_VCS5
Description:	For VDBox5
Address:	1F0890h
ShortName:	MFX_SFC_LOCK_STATUS_VCS6
Description:	For VDBox6
Address:	1F4890h
ShortName:	MFX_SFC_LOCK_STATUS_VCS7
Description:	For VDBox7

DWord	Bit	Description
0	31:2	**Reserved** Access: RO Format: MBZ

MFX_SFC_LOCK_STATUS - MFX SFC LOCK Status

	1	**MFX_SFC_Forced_Act** Access: RO Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that MFX has received MFX_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert MFX_SFC_Forced_Lock as well.
	0	**MFX_SFC_Usage** Access: RO Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to MFX. This bit should be set after SFC accepts the lock request from MFX. This bit should be clear once SFC finishes the workload and unlocked from MFX. In case a reset happens on MFX, this bit must be reset once a new workload is received

MGCMD

MGCMD - MGCMD

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	108300h

Mirror GT hardware uses for Vtd state.

DWord	Bit	Description
0	31	**TE** Access: RO _Custom_GTIReset: BUS 0: Disable Vtd DMA remapping 1: Enable Vtd DMA remapping
	30:26	**Reserved** Access: RO Format: MBZ
	25	**IRE** Access: RO _Custom_GTIReset: BUS No HW usage model. 0: Disable interrupt-remapping hardware 1: Enable interrupt-remapping hardware
	24:0	**Reserved** Access: RO Format: MBZ

MGSR GTI PD Control

GTIPD_CTRL - MGSR GTI PD Control

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
CrashLogSaved:	true
CrashLogVisibility:	cspec
Address:	00E04h-00E07h

DWord	Bit	Description
0	31:16	**Mask Bits** Access: RO Mask bits apply to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.
	15:6	**Reserved** Access: RO Format: MBZ
	5:4	**Reserved** Access: RO Format: MBZ
	3	**Reserved** Access: RO Format: MBZ
	2	**Render Unblock** Default Value: 0b Block Access: R/WC Render unblock (1) or block (0)
	1	**Reserved** Access: RO Format: MBZ
	0	**GT Unblock** Default Value: 0b Block Access: R/WC GT unblock (1) or block (0)

MGSR Media PD Control

MEDIAPD_CTRL - MGSR Media PD Control

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
CrashLogSaved:	true
CrashLogVisibility:	cspec
Address:	00E00h-00E03h

DWord	Bit	Description
0	31:16	**Mask Bits** Access: RO Mask bits applied to [15:0] of same register. If mask is set to 1, corresponding bit in [15:0] is written. If mask is set to 0, corresponding bit in [15:0] is unaffected.
	15:12	**Reserved** Access: RO Format: MBZ
	11:8	**VEBOX Unblock** Default Value: 0b Access: R/WC VEBOX unblock indications for VEBOX[3:0] (1) or block (0)
	7:0	**VDBOX Unblock** Default Value: 0b Access: R/WC VDBOX unblock indications for VDBOX[7:0] (1) or block (0) VDBOX[1:0] reside in Media slice0, VDBOX[3:2] in slice1, VDBOX[5:4] in slice2, VDBOX[7:6] in slice3

MGSR Programmable Shadow 0

PROGSHADOW_0 - MGSR Programmable Shadow 0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00EE0h-00EE3h	
DWord	**Bit**	**Description**
0	31:26	**Reserved** Access: RO Format: MBZ
	25:0	**Shadow Address** Default Value: 00000h Access: R/W Programmable shadow register address.

MGSR Programmable Shadow 1

PROGSHADOW_1 - MGSR Programmable Shadow 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00EE4h-00EE7h	
DWord	**Bit**	**Description**
0	31:26	**Reserved** Access: RO Format: MBZ
	25:0	**Shadow Address** Default Value: 00000h Access: R/W Programmable shadow register address.

MI_SET_PREDICATE_RESULT

MI_SET_PREDICATE_RESULT - MI_SET_PREDICATE_RESULT	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	023B8h-023BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_RCSUNIT_CTX
Address:	223B8h-223BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_BCSUNIT_CTX
Address:	1C03B8h-1C03BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VCSUNIT0_CTX
Address:	1C43B8h-1C43BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VCSUNIT1_CTX
Address:	1C83B8h-1C83BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VECSUNIT0_CTX
Address:	1D03B8h-1D03BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VCSUNIT2_CTX
Address:	1D43B8h-1D43BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VCSUNIT3_CTX
Address:	1D83B8h-1D83BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VECSUNIT1_CTX
Address:	1E03B8h-1E03BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VCSUNIT4_CTX
Address:	1E43B8h-1E43BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VCSUNIT5_CTX

Address:	1E83B8h-1E83BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VECSUNIT2_CTX
Address:	1F03B8h-1F03BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VCSUNIT6_CTX
Address:	1F43B8h-1F43BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VCSUNIT7_CTX
Address:	1F83B8h-1F83BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_VECSUNIT3_CTX
Address:	1A3B8h-1A3BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_CCSUNIT0_CTX
Address:	1C3B8h-1C3BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_CCSUNIT1_CTX
Address:	1E3B8h-1E3BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_CCSUNIT2_CTX
Address:	263B8h-263BBh
Name:	MI_SET_PREDICATE_RESULT
ShortName:	MI_SET_PREDICATE_RESULT_CCSUNIT3_CTX

This register is engine context save/restored on a context switch.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: PBC

	0	**SET_PREDICATE_RESULT** This field gets set/reset based on the condition evaluated during execution of MI_SET_PREDICATE command. **Value** / **Name** / **Description** 00b / **[Default]** / Predication is not enabled due to MI_SET_PREDICATE command. 01b / / Predication is enabled due to MI_SET_PREDICATE command execution. All subsequent commands executed from ring buffer and batch buffer will get predicated (NOOPed) except for the MI_SET_PREDICTE command itself and the predication does not get applied to command executed from context restore or workaround batch buffers. The following commands are exception and will get predicated only if their command header has Predication Enabled else executed as usual. • MI_BATCH_BUFFER_START • MI_BATCH_BUFFER_END • MI_CONDITIONAL_BATCH_BUFFER_END

Minimum Grant

MINGNT_0_2_0_PCI - Minimum Grant		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	0003Eh	
The Integrated Graphics Device has no requirement for the settings of Latency Timers.		
DWord	**Bit**	**Description**
0	7:0	**Minimum Grant Value** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s because the IGD does not burst as a PCI compliant primary.

Minute IA Force Fence

MIA_FORCE_FENCE - Minute IA Force Fence

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Programming Notes
Write by MinIAto issue a fence. Written value is not stored.
Write to this register by the core will trigger GUC Hardware to do following sequencing Stall the core interface. Check for all prior writes generated by the core are completed and to global observable point. Un-Stall the core interface.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Reserved** Access: RO Format: MBZ

Minute IA Force TLB Invalidate

MIA_INV_TLB - Minute IA Force TLB Invalidate

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Programming Notes

Write to issue a TLB invalidate or Fence write. Written value is not stored.

Write to this register by the core will trigger GUC Hardware to do following sequencing
Stall the core interface.
Check for all prior writes generated by the core are completed and to global observable point.
TLB invalidation generation and completion to memory interface.
Un-Stall the core interface.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Reserved** Access: RO Format: MBZ

Mirror FUSE A

MIRROR_FUSE_A - Mirror FUSE A		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Mirror Register for Fuses in INF domain.		
DWord	**Bit**	**Description**
0	31:1	**Reserved** Access: RO Reserved
	0	**Reserved** Access: RO Format: MBZ

Mirror GT C6 entry Count

MIRROR_GT_C6_ENTRY_COUNT - Mirror GT C6 entry Count	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00DACh
Name:	Mirror GT C6 entry Count
ShortName:	MIRROR_GT_C6_ENTRY_COUNT

This register holds the mirrored value, from OA, of the number of GT C6 entries that have happened

DWord	Bit	Description
0	31:0	**Count for number of C6 entries** Access: R/W _Custom_GTIReset: BUS Mirror the number of times that GT has entered C6

Mirror of DPRB LSB

DPRB_LSB - Mirror of DPRB LSB		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 090E8h		
DWord	**Bit**	**Description**
0	31:20	**DPRBASE** Access: RO _Custom_GTIReset: BUS 1MB aligned base of DMA Protected Memory Range
	19:0	**Spares** Access: RO _Custom_GTIReset: BUS

Mirror of DPRB MSB

DPRB_MSB - Mirror of DPRB MSB		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 090ECh		
DWord	**Bit**	**Description**
0	31:0	**DPRBASE** Access: RO _Custom_GTIReset: BUS Reserved

Mirror of DSMBASE LSB

DSMB_LSB - Mirror of DSMBASE LSB		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 090D0h		
DSM Base		
DWord	**Bit**	**Description**
0	31:20	**DSM Base Register LSB** Access: RO _Custom_GTIReset: BUS This register contains the base address of stolen DRAM memory.
	19:0	**Spares** Access: RO _Custom_GTIReset: BUS

Mirror of DSMBASE MSB

DSMB_MSB - Mirror of DSMBASE MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	090D4h	
DSM Base		
DWord	**Bit**	**Description**
0	31:0	**DSM Base Register** Access: RO _Custom_GTIReset: BUS This register contains the base address of stolen DRAM memory.

Mirror of EMRR Base LSB

EMRRBASE_LSB - Mirror of EMRR Base LSB		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 09200h		
Mirror of EMRR Base		
DWord	**Bit**	**Description**
0	31:12	**EMRR Base LSB** Access: RO _Custom_GTIReset: BUS EMRR Base Value.
	11:0	**Spares** Access: RO _Custom_GTIReset: BUS

Mirror of EMRR Base MSB

EMRRBASE_MSB - Mirror of EMRR Base MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09204h	
Mirror of EMRR Base		
DWord	**Bit**	**Description**
0	31:0	**EMRR Base MSB** Access: RO _Custom_GTIReset: BUS EMRR Base Value.

Mirror of EU Enable Fuses

MIRROR_EU_ENABLE - Mirror of EU Enable Fuses		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09134h	

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:0	**EU Enable Fuses** Access: RO _Custom_GTIReset: BUS **Description**: One Bit per pair of EUs In a DSS. Enable/Disable the same EU#s in all the DSS. **Programming Notes**: Bit values of 1 indicate enabled; Bit values of 0 indicate disabled.

Mirror of FUSE1 Control DW

FUSE1 - Mirror of FUSE1 Control DW		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0911Ch	
DWord	**Bit**	**Description**
0	31	**Spares** Access: RO _Custom_GTIReset: BUS
	30:29	**Reserved** Access: RO Format: MBZ
	28	**VA DISABLE** Access: RO _Custom_GTIReset: BUS
	27:24	**SFC DISABLE** Access: RO _Custom_GTIReset: BUS
	23:21	**SPARE_23_21** Access: RO
	20	**HUC AUTH BYPASS** Access: RO _Custom_GTIReset: BUS This fuse works for both Micro Controllers present in Media pipeline.
	19	**HUC DISABLE** Access: RO _Custom_GTIReset: BUS This fuse works for both Micro Controllers present in Media pipeline.
	18	**Reserved**
	17:16	**Spares1** Access: RO _Custom_GTIReset: BUS
	15	**Authentication Bypass** Access: RO _Custom_GTIReset: BUS
	14	**Reserved**

FUSE1 - Mirror of FUSE1 Control DW

	13	**Spares2** Access: RO _Custom_GTIReset: BUS
	12	**Reserved**
	11	**SPARE_11** Access: RO _Custom_GTIReset: BUS
	10:9	**Spares3** Access: RO _Custom_GTIReset: BUS
	8	**VME IME Enable** Access: RO _Custom_GTIReset: BUS
	7	**VME CRE Enable** Access: RO _Custom_GTIReset: BUS
	6:5	**Media Decode** Access: RO _Custom_GTIReset: BUS Applicable to Media - Fuse to disable VIN from processing media_objs or turn off the entire crclk tree trunk.
	4	**SPARE_4** Access: RO
	3	**Reserved**
	2	**Spares4** Access: RO _Custom_GTIReset: BUS
	1:0	**Media Encode** Access: RO _Custom_GTIReset: BUS Applicable to Media - One fuse to disable VIN from processing Pak_obj. Second fuse to disable VME.

Mirror of Fuse 3 control DW

FUSE3 - Mirror of Fuse 3 control DW		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09118h	
FUSE MIRROR 3		
DWord	**Bit**	**Description**
0	31:29	**Reserved** Access: RO Format: MBZ
	28	**Reserved** Access: RO Format: MBZ
	27:26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23:16	**Reserved** Access: RO Format: MBZ
	15:8	**GT Memory Device Enable Fuse** Access: RO Reflects the value of the Memory Device Enable fuse. When '1', the corresponding memory device is enabled; when '0' it is disabled. [8] = Memory Device 0 [9] = Memory Device 1 ... [15] = Memory Device 7
	7:4	**Reserved** Access: RO Format: MBZ

FUSE3 - Mirror of Fuse 3 control DW		
	3:0	**GT MEML3 ENABLE** Access: RO _Custom_GTIReset: BUS Each bit per MEM slice bit 0 - M-slice0 bit 1- M- slice1 bit 2- M- slice2 bit 3- M- slice3

Mirror of Global Command Register

GCMD - Mirror of Global Command Register

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 090CCh

DWord	Bit	Description
0	31	**Translation Enable** Access: RO _Custom_GTIReset: BUS Software writes to this field to request hardware to enable/disable DMA-remapping hardware. 0: Disable DMA-remapping hardware. 1: Enable DMA-remapping hardware. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. Before enabling (or re-enabling) DMA-remapping hardware through this field, software must: • Setup the DMA-remapping structures in memory. • Flush the write buffers (through WBF field), if write buffer flushing is reported as required. • Set the root-entry table pointer in hardware (through SRTP field). • Perform global invalidation of the context-cache and global invalidation of IOTLB • If advanced fault logging supported, setup fault log pointer (through SFL field) and enable advanced fault logging (through EAFL field). Refer to Section 9 for detailed software requirements. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight translated DMA read/write requests queued within the root complex before completing the translation enable command and reflecting the status of the command through the TES field in the GSTS_REG. Value returned on read of this field is undefined.
	30	**Set Root Table Pointer** Access: RO _Custom_GTIReset: BUS Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address register. Hardware reports the status of the "root table pointer set" operation through the RTPSfield in the Global Status register. The root table pointer set operation must be performed before enabling or re-enabling(after disabling) DMA remapping through the TE field. After a "root table pointer set" operation, software must globally invalidate the context cache and then globally invalidate the IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not any stale cached entries.

GCMD - Mirror of Global Command Register

While DMA remapping is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer.
Clearing this bit has no effect. The value returned on a read of this field is undefined.

29 **Set Fault Log**

Access:	RO
_Custom_GTIReset:	BUS

This field is valid only for implementations supporting advanced fault logging.
Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register.
Hardware reports the status of the fault log set operation through the FLS field in the Global Status register.
The fault log pointer must be set before enabling advanced fault logging (through EAFL field).Once advanced fault logging is enabled, the fault log pointer may be updated through this fieldwhile DMA remapping is active.
Clearing this bit has no effect.
The value returned on read of this field is undefined.

28 **Enable Fault Logging**

Access:	RO
_Custom_GTIReset:	BUS

This field is valid only for implementations supporting advanced fault logging.
Software writes to this field to request hardware to enable or disable advanced fault logging.
0: Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers.
1: Enable use of memory-resident fault log.
When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through SFL field) before enabling advanced fault logging.
Hardware reports the status of the advanced fault logging enable operation through the AFLSfield in the Global Status register.
Value returned on read of this field is undefined.

GCMD - Mirror of Global Command Register

27 **Write Buffer Flush**

Access:	RO
_Custom_GTIReset:	BUS

This bit is valid only for implementations requiring write buffer flushing.
Software sets this field to request hardware to flush the root-complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers.
Refer to Section 11.1 for details on write-buffer flushing requirements.
Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register.
Clearing this bit has no effect.
Value returned on read of this field is undefined.

26 **Queued Invalidation Enable**

Access:	RO
_Custom_GTIReset:	BUS

This field is valid only for implementations supporting queued invalidations.
Software writes to this field to enable or disable queued invalidations.
0: Disable queued invalidations.
1: Enable use of queued invalidations.
Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register.
Refer to Section 6.2.2 for software requirements for enabling/disabling queued invalidations.
The value returned on a read of this field is undefined.

25 **Interrupt Remapping Enable**

Access:	RO
_Custom_GTIReset:	BUS

This field is valid only for implementations supporting interrupt remapping.
0: Disable interrupt-remapping hardware
1: Enable interrupt-remapping hardware
Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register.
There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all.
Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register.
The value returned on a read of this field is undefined.

GCMD - Mirror of Global Command Register

	24	**Set Interrupt Remap Table Pointer** Access: RO _Custom_GTIReset: BUS This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address register. Hardware reports the status of the interrupt remapping table pointer set operation through the IRTPS field in the Global Status register. The interrupt remap table pointer set operation must be performed before enabling or re-enabling(after disabling) interrupt-remapping hardware through the IRE field. After an interrupt remap table pointer set operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
	23	**Compatibility Format Interrupt** Access: RO _Custom_GTIReset: BUS This field is valid only for Intel(R)64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel(R)64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Legacy Interrupt Mode is active. 0: Block Compatibility format interrupts. 1: Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. Refer to Section 5.4.1 for details on Compatibility Format interrupt requests. The value returned on a read of this field is undefined. This field is not implemented on Itanium(TM) implementations.
	22:0	**Spares** Access: RO _Custom_GTIReset: BUS

Mirror of GMCH Graphics Control Register

MGGC - Mirror of GMCH Graphics Control Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09094h

Mirror of GMCH Graphics Control Register.

DWord	Bit	Description
0	31:16	**Spares** Access: RO _Custom_GTIReset: BUS
	15:8	**Graphics Mode Select** Default Value: 3h Access: RO _Custom_GTIReset: BUS This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 0h: No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO),and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. 1h-4h: Reserved. 5h-Dh: DVMT (UMA) mode, memory pre-allocated for frame buffer, in quantities as shown in the Encoding table. Eh-Fh: Reserved. NOTE: This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set. This register is also LT lockable. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.

MGGC - Mirror of GMCH Graphics Control Register

	7:6	**GTT Graphics Memory Size** Access: RO _Custom_GTIReset: BUS This field selects the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware derives the base of GSM from DSM only using the GSM size programmed in the register. 0h: No memory pre-allocated. GTT cycles (Mem and IO) are not claimed. 1h: 2 MB of memory pre-allocated for GTT. 2h: 4 MB of memory pre-allocated for GTT. 3h: 8 MB of memory pre-allocated for GTT. Hardware functionality in case of programming this value to Reserved is not guaranteed. This register is locked and becomes Read Only when the D_LCK bit in the SMRAMC register is set.
	5:3	**Spares2** Access: RO _Custom_GTIReset: BUS
	2	**Versatile Acceleration Mode Enable** Access: RO _Custom_GTIReset: BUS Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
	1	**IGD VGA Disable** Access: RO _Custom_GTIReset: BUS 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register)pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override(CAPID0[46] = 1) or via a register (DEVEN[3] = 0). This register is locked by LT lock.
	0	**Spares3** Access: RO _Custom_GTIReset: BUS

Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)

GTTMMADR_LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09124h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with 2MBof that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.
For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.
The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter.
The allocation is for 4MB and the base address is defined by bits [38:22].

DWord	Bit	Description
0	31:22	**Memory Base Address (LSB - 31:22 of 38:22)** Access: RO _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO andGlobal GTT table aperture (2MB for MMIO and 2 MB for GTT).
	21:4	**Spares** Access: RO _Custom_GTIReset: BUS
	3	**Prefetchable Memory** Access: RO _Custom_GTIReset: BUS Hardwired to 0 to prevent prefetching.
	2:1	**Memory Type** Access: RO _Custom_GTIReset: BUS 00b: To indicate 32 bit base address. 01b: Reserved. 10b: To indicate 64 bit base address. 11b: Reserved.

GTTMMADR_LSB - Mirror of Graphics Translation Table and Memory Mapped Range Address (31:0)		
	0	**Memory I/O Space** Access: RO _Custom_GTIReset: BUS Hardwired to 0 to indicate memory space.

Mirror of Graphics Translation Table and Memory Mapped Range Address UDW

GTTMMADR_MSB - Mirror of Graphics Translation Table and Memory Mapped Range Address UDW

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09128h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 4 MB combined for MMIO and Global GTT aperture, with2MB of that used by MMIO and 2MB used by GTT. GTTADR begins at (GTTMMADR + 2 MB) while the MMIO base address is the same as GTTMMADR.
For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area.
The device snoops writes to this region in order to invalidate any cached translations within the various TLBs implemented on-chip. There are some exceptions to this - see GTT-TLB in the Programming Interface chapter.
The allocation is for 4MB and the base address is defined by bits [38:22].

DWord	Bit	Description
0	31:7	**Spares** Access: RO _Custom_GTIReset: BUS
	6:0	**Memory Base Address (MSB - 38:32 of 38:22)** Access: RO _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [38:22]. 4MB combined for MMIO and Global GTT table aperture (2MB for MMIO and 2 MB for GTT).

Mirror of GSMBASE LSB

GSMB_LSB - Mirror of GSMBASE LSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	090D8h	
This register contains the base address of stolen DRAM memory for the GTT.		
DWord	**Bit**	**Description**
0	31:20	**GSM Base** Access: RO _Custom_GTIReset: BUS This register contains the base address of stolen DRAM memory for the GTT.
	19:0	**Spares** Access: RO _Custom_GTIReset: BUS

Mirror of GSMBASE MSB

GSMB - Mirror of GSMBASE MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	090DCh	
This register contains the base address of stolen DRAM memory for the GTT.		
DWord	**Bit**	**Description**
0	31:0	**GSM Base** Access: RO _Custom_GTIReset: BUS This register contains the base address of stolen DRAM memory for the GTT.

Mirror of GT Compute DSS Enable Fuses

MIRROR_GT_COMPUTE_DSS_ENABLE - Mirror of GT Compute DSS Enable Fuses

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09144h

DWord	Bit	Description
0	31:0	**GT COMPUTE DSS Enable Fuses**

Default Value:	ffffffffh Default Value
Access:	RO
_Custom_GTIReset:	BUS

Description

DSS Enable Fuses - depicts which DSSs are enabled to be used for COMPUTE
Encoding:-
32'h0000 = All Dual Sub-Slices Disabled
Note: Encoding starts with bit 0 mapped to DSS0 and goes on up to bit 31 as per the Project's Number of total DSS
bit0 - DSS 0
bit1 - DSS 1
Likewise,bit31- DSS 31

Programming Notes

Bit values of 1 indicate DSS Enabled.
Bit values of 0 indicate DSS Disabled.

Mirror of GT Geometry DSS Enable Fuses

MIRROR_GT_GEOMETRY_DSS_ENABLE - Mirror of GT Geometry DSS Enable Fuses

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0913Ch

DWord	Bit	Description
0	31:0	**GT GEOMETRY DSS Enable Fuses** Default Value: ffffffffh Default Value Access: RO _Custom_GTIReset: BUS **Description** DSS Enable Fuses - depicts which DSSs are enabled to be used for Geometry Encoding:- 32'h0000 = All Dual Sub-Slices Disabled Note: Encoding starts with bit 0 mapped to DSS0 and goes on up to bit 31 as per the Project's Number of total DSS bit0 - DSS 0 bit1 - DSS 1 Likewise,bit31- DSS 31 **Programming Notes** Bit values of 1 indicate DSS Enabled. Bit values of 0 indicate DSS Disabled.

Mirror of GT VEBOX and VDBOX Enable

MIRROR_GT_VEBOX_VDBOX_ENABLE - Mirror of GT VEBOX and VDBOX Enable

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09140h

Mirror of GT VEBOX and VDBOX Enable

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:16	**GT VEBOX ENABLE** Access: RO _Custom_GTIReset: BUS VEBOX config fuses encoding:- bit 0 = VEBOX 0 bit 1 = VEBOX 1 bit 2 = VEBOX 2 bit 3 = VEBOX 3 **Programming Notes** Bit values of 1indicate enabled. Bit values of 0indicate disabled.
	15:8	**Reserved** Access: RO Format: MBZ
	7:0	**GT VDBOX ENABLE** Access: RO _Custom_GTIReset: BUS VDBOX config fuses encoding:- bit 0 = VDBOX 0 bit 1 = VDBOX 1 .. bit 7 = VDBOX 7 **Programming Notes** Bit values of 1 indicate enabled. Bit values of 0 indicate disabled.

Mirror of PCICMD MAE/BME

PCICMD - Mirror of PCICMD MAE/BME		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0912Ch	
DWord	**Bit**	**Description**
0	31:11	**Spare** Access: R/W _Custom_GTIReset: BUS
	10	**Interrupt Disable** Access: R/W _Custom_GTIReset: BUS This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages are not sent to DMI. GSA Implementation: When 1, blocks the sending of an MSI interrupt and blocks the sending of a Line interrupt.(The interrupt status is not blocked from being reflected in the INTSTS bit.) When 0, permits the sending of an MSI interrupt or Line interrupt.
	9	**Fast Back to Back** Access: R/W _Custom_GTIReset: BUS Not Implemented. Hardwired to 0.
	8	**SERR Enable** Access: R/W _Custom_GTIReset: BUS Not Implemented. Hardwired to 0.
	7	**Address/Data Stepping Enable** Access: R/W _Custom_GTIReset: BUS Not Implemented. Hardwired to 0.
	6	**Parity Error Enable** Access: R/W _Custom_GTIReset: BUS Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.

PCICMD - Mirror of PCICMD MAE/BME

5	**Video Pallete Snooping** Access: R/W _Custom_GTIReset: BUS This bit is hardwired to 0 to disable snooping.
4	**Memory Write and Invalidate Enable** Access: R/W _Custom_GTIReset: BUS Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	**Special Cycle Enable** Access: R/W _Custom_GTIReset: BUS This bit is hardwired to 0. The IGD ignores Special cycles.
2	**Bus Primary Enable** Access: R/W _Custom_GTIReset: BUS 0: Disable IGD bus primary. 1: Enable the IGD to function as a PCI compliant primary. GSA Implementation: When 0, blocks the sending of MSI interrupts. When 1, permits the sending of above. (Note: See descriptions of the INTDIS, MSE, and INTSTS bits.)
1	**Memory Access Enable** Access: R/W _Custom_GTIReset: BUS This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	**I/O Access Enable** Access: R/W _Custom_GTIReset: BUS This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

Mirror of PMR HIGH LIMIT (31-0)

PMRHLIMIT_LSB - Mirror of PMR HIGH LIMIT (31-0)

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	090C0h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled.
When the LT CMD.LOCK.PMRC command is invoked, this register is locked (treated as RO). When the LT CMD.UNLOCK.PMR Command is invoked, this register is unlocked (treated as RW). Refer to Chapter 12 for security considerations.
This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as 0 in the Capability register).
The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1's to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register are decoded by hardware as all 1s.
The protected high-memory base & limit registers function as follows.
Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2^^(N+1) bytes.
Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region.

DWord	Bit	Description
0	31:20	**PMR HIGH LIMIT (LSB - 31:20 of 38:20)** Access: RO _Custom_GTIReset: BUS This register specifies the last host physical address of the DMA-protected high-memory region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.
	19:0	**Spares** Access: RO _Custom_GTIReset: BUS

Mirror of PMR HIGH LIMIT 63-32

PMRHLIMIT_MSB - Mirror of PMR HIGH LIMIT 63-32

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	090C4h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled.
When the LT CMD.LOCK.PMRC command is invoked, this register is locked (treated as RO). When the LT CMD.UNLOCK.PMRC command is invoked, this register is unlocked (treated as RW). Refer to Chapter 12 for security considerations.
This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as 0 in the Capability register).
The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register are decoded by hardware as all 1s.
The protected high-memory base & limit registers function as follows.
Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2^^(N+1) bytes.
Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region.

DWord	Bit	Description
0	31:7	**Spares** Access: RO _Custom_GTIReset: BUS
	6:0	**PMR HIGH LIMIT (MSB - 38:32 of 38:20)** Access: RO _Custom_GTIReset: BUS This register specifies the last host physical address of the DMA-protected high-memory region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.

Mirror of Protected Memory Enable Register

PMEN - Mirror of Protected Memory Enable Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	090ACh

Register to enable the DMA-protected memory regions set up through the PLMBASE, PLMLIMT, PHMBASE, and PHMLIMIT registers. This register is always treated as RO (0) for implementations not supporting protected memory regions (PLMR and PHMR fields reported as 0 in the Capability register).
Protected memory regions may be used by software to securely initialize remapping structures in memory. Refer to Chapter 12 for security considerations.

DWord	Bit	Description
0	31	**Enable Protected Memory Region** Access: RO _Custom_GTIReset: BUS This field controls DMA accesses to the protected low-memory and protected high-memory regions. 0: DMA accesses to protected memory regions are handled as follows: • If DMA remapping is not enabled, DMA requests (including those to protected regions) are not blocked. • If DMA remapping is enabled, DMA requests are translated per the programming of the DMA remapping structures. Software may program the DMA-remapping structures to allow or block DMA to the protected memory regions. 1: DMA accesses to protected memory regions are handled as follows: • If DMA remapping is not enabled, DMA requests to protected memory regions are blocked. These DMA requests are not recorded or reported as DMA-remapping faults. • If DMA remapping is enabled, hardware may or may not block DMA to the protected memory region(s).Software must not depend on hardware protection of the protected memory regions, and must ensure the DMA-remapping structures are properly programmed to not allow DMA to the protected memory regions. • Hardware reports the status of the protected memory enable/disable operation through the PRS field in this register. Hardware implementations supporting DMA draining must drain any in-flight translated DMA requests queued within the Root-Complex before indicating the protected memory region as enabled through the PRS field.
	30:1	**Spares** Access: RO _Custom_GTIReset: BUS

PMEN - Mirror of Protected Memory Enable Register

	0	**Protected Region Status** Access: RO _Custom_GTIReset: BUS This field indicates the status of protected memory region(s): 0: Protected memory region(s) disabled. 1: Protected memory region(s) enabled.

Mirror of RC0 Hysterisis free

MIRROR_RC0_HYSTERISIS_FREE - Mirror of RC0 Hysterisis free		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	00D94h	
Name:	Mirror of RC0 Hysterisis free	
ShortName:	MIRROR_RC0_HYSTERISIS_FREE	
Mirror of RC0 Hysterisis free from OA register DB84h		
DWord	**Bit**	**Description**
0	31:0	**Count RC0 Hysterisis free** Access: R/W _Custom_GTIReset: BUS

Mirror RC0 Any Engine Busy Free

MIRROR_RC0_ANY_ENGINE_BUSY_FREE - Mirror RC0 Any Engine Busy Free	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D90h
Name:	Mirror RC0 Any Engine Busy Free
ShortName:	MIRROR_RC0_ANY_ENGINE_BUSY_FREE
This register mirrors the count from OA register DB80h	

DWord	Bit	Description
0	31:0	**Count for RC0 Any Engine Busy Free** Access: R/W _Custom_GTIReset: BUS Mirror RC0 Any Engine Busy Free by OA

Mirror RC0 wake count free

MIRROR_RC0_WAKE_COUNT_FREE - Mirror RC0 wake count free	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D98h
Name:	Mirror RC0 wake count free
ShortName:	MIRROR_RC0_WAKE_COUNT_FREE
Access:	R/W

This mirrors the OA register DB88h

DWord	Bit	Description
0	31:0	**Count for RC0 wake count free** Access: R/W _Custom_GTIReset: BUS

Mirror Rc6 post hysterisis overhead free

MIRROR_RC6_POST_HYSTERISIS_OVERHEAD_FREE - Mirror Rc6 post hysterisis overhead free	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00DA0h
Name:	Mirror Rc6 post hysterisis overhead free
ShortName:	MIRROR_RC6_POST_HYSTERISIS_OVERHEAD_FREE
This is the mirror from OA for register DB90h	

DWord	Bit	Description
0	31:0	**Count for Mirror Rc6 post hysterisis overhead free** Access: R/W _Custom_GTIReset: BUS

Mirror rc6 pre Engine wake overhead free

MIRROR_RC6_PRE_ENGINE_WAKE_OVERHEAD_FREE - Mirror rc6 pre Engine wake overhead free	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D9Ch
Name:	Mirror rc6 pre Engine wake overhead free
ShortName:	MIRROR_RC6_PRE_ENGINE_WAKE_OVERHEAD_FREE

Mirrors the OA register DB8Ch

DWord	Bit	Description
0	31:0	**Count for rc6 pre Engine wake overhead free** Access: R/W _Custom_GTIReset: BUS

Misc Clocking Reset Control Registers

MISCCPCTL - Misc Clocking Reset Control Registers

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09424h

Miscellaneous Clocking / Reset Control Registers

DWord	Bit	Description
0	31	**clock gate control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of MISCCPCTL register are R/W 1 = All bits of MISCCPCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:25	**Bonus ECO bits** Access: R/W _Custom_GTIReset: BUS Bonus ECO bits
	24	**Reserved**
	23:20	**DOP clock gating enable for VEbox clks** Access: R/W _Custom_GTIReset: BUS Controls the Enabling of the DOP-level Vebox (cv0clk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	19:16	**DOP clock gating enable for SFC media clks** Access: R/W _Custom_GTIReset: BUS Controls the Enabling of the DOP-level SFC (csfcclk) Clock Gating in media1 via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	15:8	**DOP clock gate enable for Media Clocks** Access: R/W _Custom_GTIReset: BUS Controls the Enabling of the DOP-level Render (cmclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled

MISCCPCTL - Misc Clocking Reset Control Registers

7	**DOP clock gating enable for posh clks**

Access:	R/W
_Custom_GTIReset:	BUS

Controls the Enabling of the DOP-level posh (cposclk) Clock Gating via PM event messages
1 - Clock gating is enabled
0 - Clock gating is disabled

6	**DOP clock gating enable for Media ampler clks**

Access:	R/W
_Custom_GTIReset:	BUS

Controls the Enabling of the DOP-level Media sampler (scmsclk) Clock Gating via PM event messages
1 - Clock gating is enabled
0 - Clock gating is disabled

5	**WIDI1 DOP clock gating enable**

Access:	R/W
_Custom_GTIReset:	BUS

Controls the Enabling of the DOP-level Media sampler (cw1clk) Clock Gating via PM event messages
1 - Clock gating is enabled
0 - Clock gating is disabled

4	**DOP CLock gating Enable for Widi 0 clocks**

Access:	R/W
_Custom_GTIReset:	BUS

Controls the Enabling of the DOP-level Render (cwclk) Clock Gating via PM event messages
1 - Clock gating is enabled
0 - Clock gating is disabled

3	**DOP Clcok gating enable for GUC clocks**

Access:	R/W
_Custom_GTIReset:	BUS

Controls the Enabling of the DOP-level Render (cpclk) Clock Gating via PM event messages
1 - Clock gating is enabled
0 - Clock gating is disabled

Workaround
SW is required to disable clock gating to converge timing.

	2	**DOP clock gating Enable for Fix clocks (cfclk)** Access: R/W _Custom_GTIReset: BUS Controls the Enabling of the DOP-level Render (cfclk/cf2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	1	**DOP Clock Gating Enable for Render Clocks** Access: R/W _Custom_GTIReset: BUS Controls the Enabling of the DOP-level Render (crclk/cr2xclk) Clock Gating via PM event messages 1 - Clock gating is enabled 0 - Clock gating is disabled
	0	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved

MISC CTX control register

MISCCTXCTL - MISC CTX control register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0942Ch	

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Context Restore ACk indication from Csunit** Access: R/W Set _Custom_GTIReset: BUS Context Restore ACk indication from Csunit 1'b1 : Csunit has completed restoring CPunits adress space Once set, CPunit hardware clears this bit after sending the ctx save ack done message to CS 1'b0 : Csunit has NOT completed restoring CPunits adress space **Workaround** SW is required to disable clock gating to converge timing.

Miscellaneous Message Register 0 for GTI Doorbell Unit

DRBMISC0 - Miscellaneous Message Register 0 for GTI Doorbell Unit

Register Space: MMIO: 0/2/0
Size (in bits): 32
_Custom_GTIIsContextSaved: true

Address: 01980h

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Context Save Mask** Default Value: 001bh Access: WO _Custom_GTIReset: BUS When context save (a read) is in progress, mask is forced to particular value to save off messages that need to be retained across an RC6 event.
	15:7	**Reserved** Access: RO Format: MBZ
	6	**U2CDATPERR** Default Value: 0 Access: RO _Custom_GTIReset: BUS A one indicates that Data Parity Error was detected.
	5	**U2CADDPERR** Default Value: 0 Access: RO _Custom_GTIReset: BUS A one indicates that Address Parity Error was detected.
	4:0	**Reserved** Access: R/W Hardware Clear _Custom_GTIReset: BUS

Misc Reset Control Register

RSTCTL - Misc Reset Control Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09420h

Miscellaneous reset control registers.

DWord	Bit	Description
0	31:4	**Reserved** Access: RO _Custom_GTIReset: BUS Reserved
	3:2	**Reset Staggering Period Control** Access: R/W _Custom_GTIReset: BUS Reset assertion staggering period between reset domains during FLR and soft-resets: 00: 6 csclk staggering reset assertion staggering 01: 12 cs clocks 10: 18 cs clocks 11: 24 cs clocks
	1:0	**Reset Residency Control** Access: R/W _Custom_GTIReset: BUS Reset assertion residency period for FLR and soft-resets. "00" : 8 cs clocks "01" : 16 cs clocks "10" : 32 cs clocks "11" : 64 cs clocks

Mode Register for GAB

GAB_MODE - Mode Register for GAB

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

The GAB_MODE register contains information that controls configurations in the GAB.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask _Custom_GTIReset: DEV
	15:10	**System Memory Throttle Rate** Access: R/W _Custom_GTIReset: DEV These bits define throttle rate. It defines the number of bubbles that are inserted between BLT cycles when system memory threshold is reached. Value: 16 — Name: **[Default]** Value: 0,15 Value: 17, 63
	9	**Reserved** Access: R/W
	8:7	**Reserved** Access: R/W Format: PBC

GAB_MODE - Mode Register for GAB

6 — Disable Hashing on BCS

Access:	R/W
_Custom_GTIReset:	DEV

Two command ports (P0 and P1) from BLT to GAM are address hashed. BLB to GAB has two ports and address hashing is done internal to BLB. BCS to GAB is a single command port, and GAB address hashes the BCS requests into P0 and P1.

Value	Name	Description
0b	**[Default]**	BCS traffic is hashed onto P0 and P1
1b		BCS traffic is sent only on P0 (no hashing)

Programming Notes

When PendQ hashing control is disabled in GAM BLT Module, BCS hashing in GAB must also be disabled by setting this bit to '1. If this is not followed, there can be memory ordering violations on BCS transactions.

5:3 — BLB Arbitration Priority

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

2:0 — BCS Arbitration Priority

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

Mode Register for GAC

GAC_MODE - Mode Register for GAC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1C00A0h-1C00A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT_BE0
Address:	1C40A0h-1C40A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT_BE1
Address:	1D00A0h-1D00A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT_BE2
Address:	1D40A0h-1D40A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT_BE3
Address:	1E00A0h-1E00A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT_BE4
Address:	1E40A0h-1E40A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT_BE5
Address:	1F00A0h-1F00A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT_BE6
Address:	1F40A0h-1F40A3h
Name:	Mode Register for GAC
ShortName:	GAC_MODE_VCSUNIT_BE7

The GAC_MODE register contains information that controls configurations in the GAC.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask _Custom_GTIReset: BUS

GAC_MODE - Mode Register for GAC

	15:1	**Reserved** Access: RO Format: MBZ
	0	**GACunit VCS Fence Performance fix Override** Access: R/W Format: Disable _Custom_GTIReset: BUS

Value	Name	Description
0	**[Default]**	Performance fix **enabled** to block client credits until VCS fence advances.
1		Performance fix to block credits until VCS fence advances, **disabled.** Fence will not block input traffic from clients and will advance only after ingress FIFOs are empty (Legacy behavior.)

Mode Register for GAFS

GAFS_MODE - Mode Register for GAFS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0212Ch

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Format: Mask Masks: These bits serve as write enables for bits 15:0. If this register is written with any of these bits clear the corresponding bit in the field 15:0 will not be modified. Reading these bits always returns 0s.
	15:13	**Reserved** Access: R/W Format: PBC
	12:11	**CLR0 clients ROB low priority threshold Control** Access: R/W This bit field is used to control the threshold at which CLR0 clients will move to the low priority group in the GAFS ROB arbiter.

Value	Name	Description
00b	**[Default]**	Low priority threshold value = 'd12
01b		Low priority threshold value = 'd24
10b		Low priority threshold value = 'd36
11b		Low priority threshold value = 'd48

	10	**Reserved** Access: R/W Format: PBC

GAFS_MODE - Mode Register for GAFS

9	**Min Alloc Configuration** Access: R/W This field can be used to adjust min alloc settings in the read ROB structure in GAFS. This is used in conjunction with bit [2] of this register. {Bit[9], Bit[2]} = 2'b00 : Original values {Bit[9], Bit[2]} = 2'b01 : Override original values to gain 12 ROB locations for generic use {Bit[9], Bit[2]} = 2'b10 :Override original values to gain 22 ROB locations for generic use {Bit[9], Bit[2]} = 2'b11 : Original values **Programming Notes** This bit must be programmed to 1 for achieving performance targets.
8:3	**Reserved** Access: R/W Format: PBC
2	**Min Alloc Configuration control0** Access: R/W This field can be used to adjust min alloc settings in the read ROB structure in GAFS. This is used in conjunction with bit [9] of this register. {Bit[9], Bit[2]} = 2'b00 : Original values {Bit[9], Bit[2]} = 2'b01 : Override original values to gain 12 ROB locations for generic use {Bit[9], Bit[2]} = 2'b10 :Override original values to gain 22 ROB locations for generic use {Bit[9], Bit[2]} = 2'b11 : Original values **Programming Notes** This bit must be programmed to 0 for achieving performance targets.
1:0	**Reserved** Access: R/W Format: PBC

Mode Register for Software Interface

MI_MODE - Mode Register for Software Interface	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0209Ch-0209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_RCSUNIT_CTX
Address:	2209Ch-2209Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_BCSUNIT_CTX
Address:	1C009Ch-1C009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT0_CTX
Address:	1C409Ch-1C409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT1_CTX
Address:	1C809Ch-1C809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT0_CTX
Address:	1D009Ch-1D009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT2_CTX
Address:	1D409Ch-1D409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT3_CTX
Address:	1D809Ch-1D809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT1_CTX
Address:	1E009Ch-1E009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT4_CTX
Address:	1E409Ch-1E409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT5_CTX

MI_MODE - Mode Register for Software Interface

Address:	1E809Ch-1E809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT2_CTX

Address:	1F009Ch-1F009Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT6_CTX

Address:	1F409Ch-1F409Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VCSUNIT7_CTX

Address:	1F809Ch-1F809Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_VECSUNIT3_CTX

Address:	1A09Ch-1A09Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_CCSUNIT0_CTX

Address:	1C09Ch-1C09Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_CCSUNIT1_CTX

Address:	1E09Ch-1E09Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_CCSUNIT2_CTX

Address:	2609Ch-2609Fh
Name:	Mode Register for Software Interface
ShortName:	MI_MODE_CCSUNIT3_CTX

The MI_MODE register contains information that controls software interface aspects of the Memory Interface function.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask A 1 in a bit in this field allows the modification of the corresponding bit in Bits 15:0

MI_MODE - Mode Register for Software Interface

15 **Suspend Flush**

Access:	R/W
Format:	U1

Value	Name	Description
0h	No Delay **[Default]**	HW will not delay flush, this bit will get cleared by MI_SUSPEND_FLUSH as well
1h	Delay Flush	Suspend flush is active

Programming Notes
This should only be written to from the ring using MI_SUSPEND_FLUSH. It is considered undefined if written by software through MMIO

14 **RCS POSH LRCA Disable**

Source:	RenderCS
Access:	R/W
Exists If:	//RCS

This bit controls the context save of the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA as part of the RCS context image. This primary purpose of this bit is for backward compatibility for the render context image.

Value	Name	Description
1		RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA in context image as NOOPs.
0	**[Default]**	RCS saves the MI_LOAD_REGISTER_IMM command corresponding to POSH_LRCA as part of the context image.

13 **Disable MI_SET_CONTEXT for Execution List**

Access:	R/W
Format:	U1

Value	Name	Description
0h	Allow **[Default]**	Allow MI_SET_CONTEXT in Execlist mode
1h	Disable	Disable MI_SET_CONTEXT in Execlist Mode

MI_MODE - Mode Register for Software Interface

12 **Nested Batch Buffer Enable**

Access:	R/W

This bit is used to enable or disable third level batch buffer and associated functionality.

Value	Name	Description
0		HW will only support first level, second level, chained first level and chained second level batch buffer. Nested Level Batch Buffer field must be set in MI_BATCH_BUFFER_START command programmed in a second level batch buffer to infer as a chained second level batch buffer.
1	**[Default]**	HW will support first level, second level, third level, chained first level, chained second level and chained third level batch buffer. Nested Level Batch Buffer field must not be set in MI_BATCH_BUFFER_START command programmed in a second level batch buffer to infer a chained second level batch buffer and similarly for chained third level batch buffer.

Programming Notes
This bit must be only programmed from a ring buffer and must not be programmed from a batch buffer. This bit must be static for a given context and remain same through out the life time of a given context.

11 **Invalidate UHPTR enable**

Source:	RenderCS, VideoCS, VideoCS2, VideoEnhancementCS
Access:	R/W
Exists If:	//RCS, VCS, VECS, BCS
Format:	Enable

If bit set H/W clears the valid bit of UHPTR (2134h, bit 0) when current active head pointer is equal to UHPTR.

10 **Atomic Read Return for MI_COPY_MEM_MEM**

Access:	R/W
Format:	U1

Value	Name	Description
0h	Disable **[Default]**	Hardware does a regular memory fence write to complete the write to the destination address before moving to the next instruction.
1h	Enable	Hardware does Atomic Move with Read Return to complete the write to the destination address before moving to the next instruction.

MI_MODE - Mode Register for Software Interface

9 **Rings Idle**

Access:	R/W
Format:	U1

Read Only Status bit

Value	Name	Description
0h	Not Idle **[Default]**	Parser not Idle or Ring Arbiter not Idle.
1h	Idle	Parser Idle and Ring Arbiter Idle.

Programming Notes
Writes to this bit are not allowed.

8 **Stop Rings**

Access:	R/W
Format:	U1

Value	Name	Description
0h	**[Default]**	Normal Operation.
1h		Parser is turned off and Ring arbitration is turned off.

Programming Notes
Software must set this bit to force the Rings and Command Parser to Idle. Software must read a 1 in the Ring Idle bit after setting this bit to ensure that the hardware is idle.
Software must clear this bit for Rings to resume normal operation.

7:5 **Reserved**

Access:	R/W
Format:	PBC

4:2 **Reserved**

Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Access:	R/W
Format:	PBC

4:1	**Predicate Enable** Source: RenderCS Access: R/W This field gets set when "MI_SET_PREDICATE" command is parsed by render command streamer. Predicate Disable is the default mode of operation.

Value	Name	Description
0h	Predicate Disable	Predication is Disabled and RCS will process commands as usual.
1h	Predicate on Result2 clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is clear.
2h	Predicate on Result2 set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT_2 is set.
3h	Predicate on Result clear	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is clear.
4h	Predicate on Result set	Following Commands will be NOOPED by RCS only if the MI_PREDICATE_RESULT is set.
5h	Predicate when two or more slices enabled	Following Commands will be NOOPED by RCS only when one slice is enabled, NOOPED when more than one slice is enabled.
6h	Predicate when one or three slices enabled	Following Commands will be Executed by RCS only when two slices are enabled, NOOPED when one or three slices are enabled.
7h	Predicate when one or two slices enabled	Following Commands will be Executed by RCS only when all the three slices are enabled, NOOPED when less than three slices are enabled.
8h	Execute when four slices are enabled	Following Commands will be Executed by RCS only when all the four slices are enabled.
9h	Execute when five slices are enabled	Following Commands will be Executed by RCS only when all the five slices are enabled.
Ah	Execute when six slices are enabled	Following Commands will be Executed by RCS only when all the six slices are enabled.
Bh	NOOP in RenderCS	When RenderCS parses MI_SET_PREDICATE command with Predicate Enable set to NOOP in RenderCS, RenderCS NOOPs all the subsequent commands parsed unconditionally until the predication is disabled/modified using MI_SET_PREDICATE command. Other command streamers (non RenderCS) on parsing MI_SET_PREDICATE command with Predicate Enable set to NOOP in RenderCS dont take any action and is equivalent to parsing MI_NOOP command.
Ch	NOOP	

	8h, 9h, Ah	Reserved	
	Dh, Eh	Reserved	
	Fh	Predicate Always	Following Commands will be NOOPED by RCS unconditionally.

Programming Notes
SW must use MI_SET_PREDICATE instead of MMIO access.

1 **Reserved**

Source:	VideoCS, VideoCS2, VideoEnhancementCS
Access:	R/W
Format:	PBC

1 **Reserved**

Source:	BlitterCS
Access:	R/W
Format:	PBC

0 **Reserved**

Source:	CommandStreamer
Access:	R/W
Format:	PBC

MSG_FBC_REND_STATE

MSG_FBC_REND_STATE

Register Space:	Inbound Message
Access:	WO
Size (in bits):	32
Address:	50380h-50383h
Name:	FBC Render State
ShortName:	MSG_FBC_REND_STATE_A
Reset:	soft

Sent from GT to North Display

DWord	Bit	Description
0	31:3	**Reserved** Access: RO Format: MBZ
	2	**Nuke** Access: WO This bit indicates that render wants FBC to nuke the compressed buffer. 0b – Not Nuke 1b – Nuke
	1	**Cache Clean** Access: WO This bit indicates that render has flushed the cache, so all previous modifications have been committed to memory and can be recompressed. 0b – Not Cache Clean 1b – Cache Clean
	0	**Reserved** Access: RO Format: MBZ

MSI Mask Bits

MSI_MASK_0_2_0_PCI - MSI Mask Bits

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	000BCh

This register contains the MSI Mask Bits

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Mask Bit for Vector 0** Default Value: 0b Access: R/W _Custom_GTIReset: BUS For each Mask bit that is set, the function is prohibited from sending the associated message.

MSI Pending Bits

MSI_PEND_0_2_0_PCI - MSI Pending Bits

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	000C0h

This register contains the MSI Pending Bits

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Pending Bit for Vector 0** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS For each Pending bit that is set, the function has a pending associated message. If this bit is set when the corresponding vector's Mask bit is cleared, the function will send an MSI and then clear the Pending bit.

Multi Context Control Register

MLTICTXCTL - Multi Context Control Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B170h

Masked register for Multi Context

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Mask bits for each corresponding bit in [15:0]
	15:14	**Reserved** Access: RO Format: MBZ
	13:4	**Reserved** Access: RO Format: MBZ
	3	**Reserved** Access: RO Format: MBZ
	2	**3D on Render** Access: R/W 3D_ON_RENDER: When set, the L3 will use Render config values, else compute config values.
	1:0	**Reserved** Access: RO Format: MBZ

Multi Tile Configuration

MTCFG - Multi Tile Configuration

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 101800h

This register is used for multi-tile configurations. It contains the tile number and tile count.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**Tile Count** Default Value: 00h Access: R/W _Custom_GTIReset: BUS Tile Count 0h=Single tile (Root tile only) 1h= Reserved (Not supported configuration) 2h=Reserved (Not supported configuration) 3h= Reserved (Not supported configuration) 4h to FFh=Reserved (not supported) Reset value is based on input straps.
	7:0	**Tile Number** Default Value: 00h Access: R/W _Custom_GTIReset: BUS Tile number assignment (ie. this is my tile number). 0h=Root tile 1h= Reserved (Not supported configuration) 2h= Reserved (Not supported configuration) 3h= Reserved (Not supported configuration) 4h to FFh=Reserved (not supported) Reset value is based on input straps.

NDE_RSTWRN_OPT

NDE_RSTWRN_OPT

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	46408h-4640Bh
Name:	North Display Reset Warn Options
ShortName:	NDE_RSTWRN_OPT
Reset:	global

This register is used to control the display behavior on receiving a Reset Warning or FLR.

DWord	Bit	Description
0	31:7	**Reserved** Access: RO Format: MBZ
	6	**Reserved** Access: RO Format: MBZ
	5	**Reserved** Access: R/W
	4	**RST PCH Handshake En** Access: R/W This field enables the handshake with south display when processing the reset. This applies to all types of DE resets. By default it is disabled and the north display will not wait for south display to acknowledge the reset. "PCH" here refers to the south display, which is always present even when the south display is in the same SoC as north display. **Value** / **Name** 0b – Disable 1b – Enable **Programming Notes** This must be programmed as part of the display initialization sequence.
	3:0	**Reserved** Access: RO Format: MBZ

NONPIPE_ISOCREQ

NONPIPE_ISOCREQ	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	45230h-45237h
Name:	Non Pipe Isoch Request
ShortName:	NONPIPE_ISOCREQ
Reset:	soft

This register is used to trigger an IsocReq that is not associated with a pipe. When enabled, the write to DWord 1 (higher address DWord) of this register triggers an IsocReq to be sent with the last written values from both DWords.

DWord	Bit	Description
0	31:16	**LTR** Access: R/W This field specifies the latency tolerance (LTR) in microseconds.
	15:0	**Bandwidth** Access: R/W This field specifies the bandwidth requirement in multiples of 100 MB/s.
1	31	**Enable** Access: R/W This field enables IsocReq to be sent when DWord 1 of this register is written. Value: 1b — Name: Enable Value: 0b — Name: Disable
	30:8	**Reserved** Access: RO Format: MBZ
	7:0	**Delay** Access: R/W This field specifies the downwards transition delay in milliseconds.

NOP Identification Register

NOPID - NOP Identification Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02094h-02097h
Name:	NOP Identification Register
ShortName:	NOPID_RCSUNIT_CTX
Address:	22094h-22097h
Name:	NOP Identification Register
ShortName:	NOPID_BCSUNIT_CTX
Address:	1C0094h-1C0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT0_CTX
Address:	1C4094h-1C4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT1_CTX
Address:	1C8094h-1C8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT0_CTX
Address:	1D0094h-1D0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT2_CTX
Address:	1D4094h-1D4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT3_CTX
Address:	1D8094h-1D8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT1_CTX
Address:	1E0094h-1E0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT4_CTX
Address:	1E4094h-1E4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT5_CTX

NOPID - NOP Identification Register

Address:	1E8094h-1E8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT2_CTX

Address:	1F0094h-1F0097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT6_CTX

Address:	1F4094h-1F4097h
Name:	NOP Identification Register
ShortName:	NOPID_VCSUNIT7_CTX

Address:	1F8094h-1F8097h
Name:	NOP Identification Register
ShortName:	NOPID_VECSUNIT3_CTX

Address:	1A094h-1A097h
Name:	NOP Identification Register
ShortName:	NOPID_CCSUNIT0_CTX

Address:	1C094h-1C097h
Name:	NOP Identification Register
ShortName:	NOPID_CCSUNIT1_CTX

Address:	1E094h-1E097h
Name:	NOP Identification Register
ShortName:	NOPID_CCSUNIT2_CTX

Address:	26094h-26097h
Name:	NOP Identification Register
ShortName:	NOPID_CCSUNIT3_CTX

The NOPID register contains the Noop Identification value specified by the last MI_NOOP instruction that enabled this register to be updated.

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21:0	**Reserved** Access: R/W

Number Of VFs

SRIOV_NUMOFVFS_0_2_0_PCI - Number Of VFs		
Register Space: PCI: 0/2/0 Size (in bits): 32		
Address: 00330h		
Number of VFs enabled by the VMM.		
DWord	**Bit**	**Description**
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**Function Dependency Link** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Same value as the Physical function number indicating no Dependency
	15:0	**Number of Virtual Functions** Default Value: 0000000000000000b Access: R/W _Custom_GTIReset: BUS System SW shall set this field to control the number of VFs that are visible. This field must be programmed before setting VF Enable. Changing this field when VF Enable is set will produced undefined behavior as per the SR-IOV specification. HW will ignore the new value programmed.

OAC Aggregate Perf Counter A0

OAC_OAPERF_A0 - OAC Aggregate Perf Counter A0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15000h-15003h
Name:	Aggregate Perf Counter A0
ShortName:	OAC_OAPERF_A0_CCS0_OA

This register reflects the count value of the OA Performance counter A0.
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads. Value: 0x00000000 — **[Default]** Value: [0x00000001-0xFFFFFFFF]

OAC Aggregate Perf Counter A0 Upper DWord

OAC_OAPERF_A0_UPPER - OAC Aggregate Perf Counter A0 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15004h-15007h
Name:	Aggregate Perf Counter A0 Upper DWord
ShortName:	OAC_OAPERF_A0_UPPER_CCS0_OA

This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A4

OAC_OAPERF_A4 - OAC Aggregate Perf Counter A4	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15008h-1500Bh
Name:	Aggregate Perf Counter A4
ShortName:	OAC_OAPERF_A4_CCS0_OA

This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A4 Upper DWord

OAC_OAPERF_A4_UPPER - OAC Aggregate Perf Counter A4 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1500Ch-1500Fh
Name:	Aggregate Perf Counter A4 Upper DWord
ShortName:	OAC_OAPERF_A4_UPPER_CCS0_OA

This register enables the current live value of performance counter A4 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A7

OAC_OAPERF_A7 - OAC Aggregate Perf Counter A7	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15010h-15013h
Name:	Aggregate Perf Counter A7
ShortName:	OAC_OAPERF_A7_CCS0_OA

This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A7 Upper DWord

OAC_OAPERF_A7_UPPER - OAC Aggregate Perf Counter A7 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15014h-15017h
Name:	Aggregate Perf Counter A7 Upper DWord
ShortName:	OAC_OAPERF_A7_UPPER_CCS0_OA

This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A8

OAC_OAPERF_A8 - OAC Aggregate Perf Counter A8

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15018h-1501Bh
Name:	Aggregate Perf Counter A8
ShortName:	OAC_OAPERF_A8_CCS0_OA

This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A8 Upper DWord

OAC_OAPERF_A8_UPPER - OAC Aggregate Perf Counter A8 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1501Ch-1501Fh
Name:	Aggregate Perf Counter A8 Upper DWord
ShortName:	OAC_OAPERF_A8_UPPER_CCS0_OA

This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A9

OAC_OAPERF_A9 - OAC Aggregate Perf Counter A9	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15020h-15023h
Name:	Aggregate Perf Counter A9
ShortName:	OAC_OAPERF_A9_CCS0_OA

This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A9 Upper DWord

OAC_OAPERF_A9_UPPER - OAC Aggregate Perf Counter A9 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15024h-15027h
Name:	Aggregate Perf Counter A9 Upper DWord
ShortName:	OAC_OAPERF_A9_UPPER_CCS0_OA

This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A10

OAC_OAPERF_A10 - OAC Aggregate Perf Counter A10

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15028h-1502Bh
Name:	Aggregate Perf Counter A10
ShortName:	OAC_OAPERF_A10_CCS0_OA

This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A10 Upper DWord

OAC_OAPERF_A10_UPPER - OAC Aggregate Perf Counter A10 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1502Ch-1502Fh
Name:	Aggregate Perf Counter A10 Upper DWord
ShortName:	OAC_OAPERF_A10_UPPER_CCS0_OA

This register enables the current live value of performance counter A10 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A11

OAC_OAPERF_A11 - OAC Aggregate Perf Counter A11	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15030h-15033h
Name:	Aggregate Perf Counter A11
ShortName:	OAC_OAPERF_A11_CCS0_OA

This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A11 Upper DWord

OAC_OAPERF_A11_UPPER - OAC Aggregate Perf Counter A11 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15034h-15037h
Name:	Aggregate Perf Counter A11 Upper DWord
ShortName:	OAC_OAPERF_A11_UPPER_CCS0_OA

This register enables the current live value of performance counter A11 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A12

OAC_OAPERF_A12 - OAC Aggregate Perf Counter A12

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15038h-1503Bh
Name:	Aggregate Perf Counter A12
ShortName:	OAC_OAPERF_A12_CCS0_OA

This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A12 Upper DWord

OAC_OAPERF_A12_UPPER - OAC Aggregate Perf Counter A12 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1503Ch-1503Fh
Name:	Aggregate Perf Counter A12 Upper DWord
ShortName:	OAC_OAPERF_A12_UPPER_CCS0_OA

This register enables the current live value of performance counter A12 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A13

OAC_OAPERF_A13 - OAC Aggregate Perf Counter A13	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15040h-15043h
Name:	Aggregate Perf Counter A13
ShortName:	OAC_OAPERF_A13_CCS0_OA

This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A13 Upper DWord

OAC_OAPERF_A13_UPPER - OAC Aggregate Perf Counter A13 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15044h-15047h
Name:	Aggregate Perf Counter A13 Upper DWord
ShortName:	OAC_OAPERF_A13_UPPER_CCS0_OA

This register enables the current live value of performance counter A13 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A14

OAC_OAPERF_A14 - OAC Aggregate Perf Counter A14

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15048h-1504Bh
Name:	Aggregate Perf Counter A14
ShortName:	OAC_OAPERF_A14_CCS0_OA

This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A14 Upper DWord

OAC_OAPERF_A14_UPPER - OAC Aggregate Perf Counter A14 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1504Ch-1504Fh
Name:	Aggregate Perf Counter A14 Upper DWord
ShortName:	OAC_OAPERF_A14_UPPER_CCS0_OA

This register enables the current live value of performance counter A14 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A15

OAC_OAPERF_A15 - OAC Aggregate Perf Counter A15	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15050h-15053h
Name:	Aggregate Perf Counter A15
ShortName:	OAC_OAPERF_A15_CCS0_OA

This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A15 Upper DWord

OAC_OAPERF_A15_UPPER - OAC Aggregate Perf Counter A15 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15054h-15057h
Name:	Aggregate Perf Counter A15 Upper DWord
ShortName:	OAC_OAPERF_A15_UPPER_CCS0_OA

This register enables the current live value of performance counter A15 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A16

OAC_OAPERF_A16 - OAC Aggregate Perf Counter A16	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15058h-1505Bh
Name:	Aggregate Perf Counter A16
ShortName:	OAC_OAPERF_A16_CCS0_OA

This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A16 Upper DWord

OAC_OAPERF_A16_UPPER - OAC Aggregate Perf Counter A16 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1505Ch-1505Fh
Name:	Aggregate Perf Counter A16 Upper DWord
ShortName:	OAC_OAPERF_A16_UPPER_CCS0_OA

This register enables the current live value of performance counter A16 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A17

OAC_OAPERF_A17 - OAC Aggregate Perf Counter A17

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15060h-15063h
Name:	Aggregate Perf Counter A17
ShortName:	OAC_OAPERF_A17_CCS0_OA

This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A17 Upper DWord

OAC_OAPERF_A17_UPPER - OAC Aggregate Perf Counter A17 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15064h-15067h
Name:	Aggregate Perf Counter A17 Upper DWord
ShortName:	OAC_OAPERF_A17_UPPER_CCS0_OA

This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A18

OAC_OAPERF_A18 - OAC Aggregate Perf Counter A18

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15068h-1506Bh
Name:	Aggregate Perf Counter A18
ShortName:	OAC_OAPERF_A18_CCS0_OA

This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A18 Upper DWord

OAC_OAPERF_A18_UPPER - OAC Aggregate Perf Counter A18 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1506Ch-1506Fh
Name:	Aggregate Perf Counter A18 Upper DWord
ShortName:	OAC_OAPERF_A18_UPPER_CCS0_OA

This register enables the current live value of performance counter A18 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A19

OAC_OAPERF_A19 - OAC Aggregate Perf Counter A19	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15070h-15073h
Name:	Aggregate Perf Counter A19
ShortName:	OAC_OAPERF_A19_CCS0_OA

This register reflects the count value of the OA Performance counter A19. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A19 Upper DWord

OAC_OAPERF_A19_UPPER - OAC Aggregate Perf Counter A19 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15074h-15077h
Name:	Aggregate Perf Counter A19 Upper DWord
ShortName:	OAC_OAPERF_A19_UPPER_CCS0_OA

This register enables the current live value of performance counter A19 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A20

OAC_OAPERF_A20 - OAC Aggregate Perf Counter A20	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15078h-1507Bh
Name:	Aggregate Perf Counter A20
ShortName:	OAC_OAPERF_A20_CCS0_OA

This register reflects the count value of the OA Performance counter A20. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A20 Upper DWord

OAC_OAPERF_A20_UPPER - OAC Aggregate Perf Counter A20 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1507Ch-1507Fh
Name:	Aggregate Perf Counter A20 Upper DWord
ShortName:	OAC_OAPERF_A20_UPPER_CCS0_OA

This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A28

OAC_OAPERF_A28 - OAC Aggregate Perf Counter A28	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15080h-15083h
Name:	Aggregate Perf Counter A28
ShortName:	OAC_OAPERF_A28_CCS0_OA

This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A28 Upper DWord

OAC_OAPERF_A28_UPPER - OAC Aggregate Perf Counter A28 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15084h-15087h
Name:	Aggregate Perf Counter A28 Upper DWord
ShortName:	OAC_OAPERF_A28_UPPER_CCS0_OA

This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A29

OAC_OAPERF_A29 - OAC Aggregate Perf Counter A29

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15088h-1508Bh
Name:	Aggregate Perf Counter A29
ShortName:	OAC_OAPERF_A29_CCS0_OA

This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A29 Upper DWord

OAC_OAPERF_A29_UPPER - OAC Aggregate Perf Counter A29 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1508Ch-1508Fh
Name:	Aggregate Perf Counter A29 Upper DWord
ShortName:	OAC_OAPERF_A29_UPPER_CCS0_OA

This register enables the current live value of performance counter A29 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A30

OAC_OAPERF_A30 - OAC Aggregate Perf Counter A30	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15090h-15093h
Name:	Aggregate Perf Counter A30
ShortName:	OAC_OAPERF_A30_CCS0_OA

This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h"
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A30 Upper DWord

OAC_OAPERF_A30_UPPER - OAC Aggregate Perf Counter A30 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15094h-15097h
Name:	Aggregate Perf Counter A30 Upper DWord
ShortName:	OAC_OAPERF_A30_UPPER_CCS0_OA

This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A31

OAC_OAPERF_A31 - OAC Aggregate Perf Counter A31

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15098h-1509Bh
Name:	Aggregate Perf Counter A31
ShortName:	OAC_OAPERF_A31_CCS0_OA

This register reflects the count value of the OA Performance counter A31

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A31 Upper DWord

OAC_OAPERF_A31_UPPER - OAC Aggregate Perf Counter A31 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1509Ch-1509Fh
Name:	Aggregate Perf Counter A31 Upper DWord
ShortName:	OAC_OAPERF_A31_UPPER_CCS0_OA

This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A32

OAC_OAPERF_A32 - OAC Aggregate Perf Counter A32	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150A0h-150A3h
Name:	Aggregate Perf Counter A32
ShortName:	OAC_OAPERF_A32_CCS0_OA

This register reflects the count value of the OA Performance counter A32
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OACAggregatePerfCounterA32UpperDWord

OAC_OAPERF_A32_UPPER - OACAggregatePerfCounterA32UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150A4h-150A7h
Name:	Aggregate Perf Counter A32 Upper DWord
ShortName:	OAC_OAPERF_A32_UPPER_CCS0_OA

This register enables the current live value of performance counter A32 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A34

OAC_OAPERF_A34 - OAC Aggregate Perf Counter A34

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150B0h-150B3h
Name:	Aggregate Perf Counter A34
ShortName:	OAC_OAPERF_A34_CCS0_OA

This register reflects the count value of the OA Performance counter A34

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OACAggregatePerfCounterA34UpperDWord

OAC_OAPERF_A34_UPPER - OACAggregatePerfCounterA34UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150B4h-150B7h
Name:	Aggregate Perf Counter A34 Upper DWord
ShortName:	OAC_OAPERF_A34_UPPER_CCS0_OA

This register enables the current live value of performance counter A34 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this upper register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Aggregate Perf Counter A35

OAC_OAPERF_A35 - OAC Aggregate Perf Counter A35

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150B8h-150BBh
Name:	Aggregate Perf Counter A35
ShortName:	OAC_OAPERF_A35_CCS0_OA

This register reflects the count value of the OA Performance counter A35
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OACAggregatePerfCounterA35UpperDWord

OAC_OAPERF_A35_UPPER - OACAggregatePerfCounterA35UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150BCh-150BFh
Name:	Aggregate Perf Counter A35 Upper DWord
ShortName:	OAC_OAPERF_A35_UPPER_CCS0_OA

This register enables the current live value of performance counter A35 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this upper register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Boolean_Counter_B0

OAC_OAPERF_B0 - OAC Boolean_Counter_B0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150D4h-150D7h
Name:	Boolean Counter B0
ShortName:	OAC_OAPERF_B0_CCS0_OA

This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Boolean_Counter_B1

OAC_OAPERF_B1 - OAC Boolean_Counter_B1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150D8h-150DBh
Name:	Boolean Counter B1
ShortName:	OAC_OAPERF_B1_CCS0_OA

This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Boolean_Counter_B2

OAC_OAPERF_B2 - OAC Boolean_Counter_B2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150DCh-150DFh
Name:	Boolean Counter B2
ShortName:	OAC_OAPERF_B2_CCS0_OA

This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Boolean_Counter_B3

OAC_OAPERF_B3 - OAC Boolean_Counter_B3

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150E0h-150E3h
Name:	Boolean Counter B3
ShortName:	OAC_OAPERF_B3_CCS0_OA

This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Boolean_Counter_B4

OAC_OAPERF_B4 - OAC Boolean_Counter_B4

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150E4h-150E7h
Name:	Boolean Counter B4
ShortName:	OAC_OAPERF_B4_CCS0_OA

This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Boolean_Counter_B5

OAC_OAPERF_B5 - OAC Boolean_Counter_B5

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150E8h-150EBh
Name:	Boolean Counter B5
ShortName:	OAC_OAPERF_B5_CCS0_OA

This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Boolean_Counter_B6

OAC_OAPERF_B6 - OAC Boolean_Counter_B6

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150ECh-150EFh
Name:	Boolean Counter B6
ShortName:	OAC_OAPERF_B6_CCS0_OA

This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Boolean_Counter_B7

OAC_OAPERF_B7 - OAC Boolean_Counter_B7	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	150F0h-150F3h
Name:	Boolean Counter B7
ShortName:	OAC_OAPERF_B7_CCS0_OA

This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC GPU Ticks Counter

OAC_GPU_TICKS - OAC GPU Ticks Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15120h-15123h
Name:	GPU Ticks Counter
ShortName:	OAC_GPU_TICKS_CCS0_OA

Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC GPU Ticks Counter Upper DWord

OAC_GPU_TICKS_UPPER - OAC GPU Ticks Counter Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15124h-15127h
Name:	GPU Ticks Counter Upper DWord
ShortName:	OAC_GPU_TICKS_UPPER_CCS0_OA

Reading this register returns the live value of the Upper DWord of GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAC Observation Architecture Control

OAC_OACONTROL - OAC Observation Architecture Control

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	15114h-15117h
Name:	Control Register
ShortName:	OAC_OACONTROL_CCS0_OA

This register controls OAC functionality, report format, and context filtering. If OAC is enabled then it should be enabled in CS as well

DWord	Bit	Description
0	31:4	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	3:1	**Counter Select** Access: R/W _Custom_GTIReset: DEV This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.
	0	**Performance Counter Enable** Access: R/W Format: Enable _Custom_GTIReset: DEV Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear. **Programming Notes** "OAC Context Enable" mode bit in RenderEngne CTX_SR_CTL register must be set when "Programmer Counter Enable" is set.

OAC Observation Architecture Status Register

OAC_OASTATUS - OAC Observation Architecture Status Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1511Ch-1511Fh
Name:	Status Register
ShortName:	OAC_OASTATUS_CCS0_OA

This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits. Status bits are active high flags (0=false, 1=true)

DWord	Bit	Description
0	31:22	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	21	**Start Trigger Flag 1** Access: R/W _Custom_GTIReset: DEV Value / Name: 0 **[Default]**; 1 **Programming Notes**: This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.
	20	**Start Trigger Flag 2** Access: R/W _Custom_GTIReset: DEV Value / Name: 0 **[Default]**; 1 **Programming Notes**: This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.

OAC_OASTATUS - OAC Observation Architecture Status Register

	19	**Report Trigger Flag 1** Access: R/W _Custom_GTIReset: DEV **Value** / **Name** 0 **[Default]** 1 **Programming Notes** This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.
	18	**Report Trigger Flag 2** Access: R/W _Custom_GTIReset: DEV **Value** / **Name** 0 **[Default]** 1 **Programming Notes** This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.
	17:6	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	5:2	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OAC_OASTATUS - OAC Observation Architecture Status Register

	1	**Accumulator Overflow** Access: R/W _Custom_GTIReset: DEV This field indicates that the one or more event accumulator inside the slice-OAunit has overflowed. Once set, this bit will remain set, until SW resets it by either soft reset or writing a 0 to it. **Value** / **Name** / **Description** 0 / **[Default]** / No overflow has occurred. 1 / / Overflow has occurred.
	0	**Counter Overflow** Access: R/W _Custom_GTIReset: DEV This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 0 to it. **Value** / **Name** / **Description** 0 / **[Default]** / Counter Overflow not occurred 1 / / Counter Overflow occurred

OAG Aggregate Perf Counter A0

OAG_OAPERF_A0 - OAG Aggregate Perf Counter A0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D980h

This register reflects the count value of the OA Performance counter A0.
More details about the precise event counted by this register are located **here**.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads. Value: 0x00000000 **[Default]** Value: [0x00000001-0xFFFFFFFF]

OAG Aggregate Perf Counter A0 Upper DWord

OAG_OAPERF_A0_UPPER - OAG Aggregate Perf Counter A0 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D984h

This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A1

OAG_OAPERF_A1 - OAG Aggregate Perf Counter A1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D988h	
This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A1 Upper DWord

OAG_OAPERF_A1_UPPER - OAG Aggregate Perf Counter A1 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D98Ch

This register enables the current live value of performance counter A1 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A2

OAG_OAPERF_A2 - OAG Aggregate Perf Counter A2		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D990h	
This register reflects the count value of the OA Performance counter A2. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A2 Upper DWord

OAG_OAPERF_A2_UPPER - OAG Aggregate Perf Counter A2 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D994h

This register enables the current live value of performance counter A2 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A3

OAG_OAPERF_A3 - OAG Aggregate Perf Counter A3		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D998h	
This register reflects the count value of the OA Performance counter A3. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A3 Upper DWord

OAG_OAPERF_A3_UPPER - OAG Aggregate Perf Counter A3 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D99Ch

This register enables the current live value of performance counter A3 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A4

OAG_OAPERF_A4 - OAG Aggregate Perf Counter A4		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9A0h	
This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A4 Lower DWord Free

OAG_OAPERF_A4_LOWER_FREE - OAG Aggregate Perf Counter A4 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAD4h

This register counts the same event as counter A4 however is not affected by context ID or other conditions that prevent A4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A4 Upper DWord

OAG_OAPERF_A4_UPPER - OAG Aggregate Perf Counter A4 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9A4h

This register enables the current live value of performance counter A4 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A5

OAG_OAPERF_A5 - OAG Aggregate Perf Counter A5		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9A8h	
This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A5 Upper DWord

OAG_OAPERF_A5_UPPER - OAG Aggregate Perf Counter A5 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9ACh

This register enables the current live value of performance counter A5 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A6

OAG_OAPERF_A6 - OAG Aggregate Perf Counter A6		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9B0h	
This register reflects the count value of the OA Performance counter A6. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A6 Lower DWord Free

OAG_OAPERF_A6_LOWER_FREE - OAG Aggregate Perf Counter A6 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DADCh

This register counts the same event as counter A6 however is not affected by context ID or other conditions that prevent A6 from incrementing. his counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A6 Upper DWord

OAG_OAPERF_A6_UPPER - OAG Aggregate Perf Counter A6 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9B4h

This register enables the current live value of performance counter A6 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A7

OAG_OAPERF_A7 - OAG Aggregate Perf Counter A7		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9B8h	
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A7 Upper DWord

OAG_OAPERF_A7_UPPER - OAG Aggregate Perf Counter A7 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9BCh

This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A8

OAG_OAPERF_A8 - OAG Aggregate Perf Counter A8		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9C0h	
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A8 Upper DWord

OAG_OAPERF_A8_UPPER - OAG Aggregate Perf Counter A8 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9C4h

This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A9

OAG_OAPERF_A9 - OAG Aggregate Perf Counter A9		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9C8h	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A9 Upper DWord

OAG_OAPERF_A9_UPPER - OAG Aggregate Perf Counter A9 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9CCh

This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A10

OAG_OAPERF_A10 - OAG Aggregate Perf Counter A10		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9D0h	
This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A10 Upper DWord

OAG_OAPERF_A10_UPPER - OAG Aggregate Perf Counter A10 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9D4h

This register enables the current live value of performance counter A10 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A11

OAG_OAPERF_A11 - OAG Aggregate Perf Counter A11		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9D8h	
This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A11 Upper DWord

OAG_OAPERF_A11_UPPER - OAG Aggregate Perf Counter A11 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9DCh

This register enables the current live value of performance counter A11 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A12

OAG_OAPERF_A12 - OAG Aggregate Perf Counter A12		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9E0h	
This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A12 Upper DWord

OAG_OAPERF_A12_UPPER - OAG Aggregate Perf Counter A12 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9E4h

This register enables the current live value of performance counter A12 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A13

OAG_OAPERF_A13 - OAG Aggregate Perf Counter A13		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9E8h	
This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A13 Upper DWord

OAG_OAPERF_A13_UPPER - OAG Aggregate Perf Counter A13 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9ECh

This register enables the current live value of performance counter A13 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A14

OAG_OAPERF_A14 - OAG Aggregate Perf Counter A14		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9F0h	
This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A14 Upper DWord

OAG_OAPERF_A14_UPPER - OAG Aggregate Perf Counter A14 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9F4h

This register enables the current live value of performance counter A14 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A15

OAG_OAPERF_A15 - OAG Aggregate Perf Counter A15		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0D9F8h	
This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A15 Upper DWord

OAG_OAPERF_A15_UPPER - OAG Aggregate Perf Counter A15 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D9FCh

This register enables the current live value of performance counter A15 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A16

OAG_OAPERF_A16 - OAG Aggregate Perf Counter A16		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA00h	
This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A16 Upper DWord

OAG_OAPERF_A16_UPPER - OAG Aggregate Perf Counter A16 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA04h

This register enables the current live value of performance counter A16 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A17

OAG_OAPERF_A17 - OAG Aggregate Perf Counter A17		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA08h	
This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A17 Upper DWord

OAG_OAPERF_A17_UPPER - OAG Aggregate Perf Counter A17 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA0Ch

This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A18

OAG_OAPERF_A18 - OAG Aggregate Perf Counter A18		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA10h	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A18 Upper DWord

OAG_OAPERF_A18_UPPER - OAG Aggregate Perf Counter A18 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA14h

This register enables the current live value of performance counter A18 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A19

OAG_OAPERF_A19 - OAG Aggregate Perf Counter A19		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA18h	
This register reflects the count value of the OA Performance counter A19. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A19 Lower DWord Free

OAG_OAPERF_A19_LOWER_FREE - OAG Aggregate Perf Counter A19 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAE4h

This register counts the same event as counter A19 however is not affected by context ID or other conditions that prevent A19 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A19 Upper DWord

OAG_OAPERF_A19_UPPER - OAG Aggregate Perf Counter A19 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA1Ch

This register enables the current live value of performance counter A19 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A20

OAG_OAPERF_A20 - OAG Aggregate Perf Counter A20		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA20h	
This register reflects the count value of the OA Performance counter A20. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A20 Lower DWord Free

OAG_OAPERF_A20_LOWER_FREE - OAG Aggregate Perf Counter A20 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAECh

This register counts the same event as counter A20 however is not affected by context ID or other conditions that prevent A20 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A20 Upper DWord

OAG_OAPERF_A20_UPPER - OAG Aggregate Perf Counter A20 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA24h

This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A21

OAG_OAPERF_A21 - OAG Aggregate Perf Counter A21		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA28h	
This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A21 Upper DWord

OAG_OAPERF_A21_UPPER - OAG Aggregate Perf Counter A21 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA2Ch

This register enables the current live value of performance counter A21 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A22

OAG_OAPERF_A22 - OAG Aggregate Perf Counter A22		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA30h	
This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A22 Upper DWord

OAG_OAPERF_A22_UPPER - OAG Aggregate Perf Counter A22 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA34h

This register enables the current live value of performance counter A22 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A23

OAG_OAPERF_A23 - OAG Aggregate Perf Counter A23		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA38h	
This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A23 Upper DWord

OAG_OAPERF_A23_UPPER - OAG Aggregate Perf Counter A23 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA3Ch

This register enables the current live value of performance counter A23 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A24

OAG_OAPERF_A24 - OAG Aggregate Perf Counter A24		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA40h	
This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A24 Upper DWord

OAG_OAPERF_A24_UPPER - OAG Aggregate Perf Counter A24 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA44h

This register enables the current live value of performance counter A24 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A25

OAG_OAPERF_A25 - OAG Aggregate Perf Counter A25		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA48h	
This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A25 Upper DWord

OAG_OAPERF_A25_UPPER - OAG Aggregate Perf Counter A25 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA4Ch

This register enables the current live value of performance counter A25 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A26

OAG_OAPERF_A26 - OAG Aggregate Perf Counter A26		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA50h	
This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A26 Upper DWord

OAG_OAPERF_A26_UPPER - OAG Aggregate Perf Counter A26 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA54h

This register enables the current live value of performance counter A26 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A27

OAG_OAPERF_A27 - OAG Aggregate Perf Counter A27		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA58h	
This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A27 Upper DWord

OAG_OAPERF_A27_UPPER - OAG Aggregate Perf Counter A27 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA5Ch

This register enables the current live value of performance counter A27 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A28

OAG_OAPERF_A28 - OAG Aggregate Perf Counter A28		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA60h	
This register reflects the count value of the OA Performance counter A28. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A28 Upper DWord

OAG_OAPERF_A28_UPPER - OAG Aggregate Perf Counter A28 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA64h

This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A29

OAG_OAPERF_A29 - OAG Aggregate Perf Counter A29		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA68h	
This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A29 Upper DWord

OAG_OAPERF_A29_UPPER - OAG Aggregate Perf Counter A29 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA6Ch

This register enables the current live value of performance counter A29 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A30

OAG_OAPERF_A30 - OAG Aggregate Perf Counter A30		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA70h	
This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A30 Upper DWord

OAG_OAPERF_A30_UPPER - OAG Aggregate Perf Counter A30 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA74h

This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A31

OAG_OAPERF_A31 - OAG Aggregate Perf Counter A31		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA78h	
This register reflects the count value of the OA Performance counter A31		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A31 Upper DWord

OAG_OAPERF_A31_UPPER - OAG Aggregate Perf Counter A31 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA7Ch

This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A32

OAG_OAPERF_A32 - OAG Aggregate Perf Counter A32		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA80h	
This register reflects the count value of the OA Performance counter A32.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A32 Upper DWord

OAG_OAPERF_A32_UPPER - OAG Aggregate Perf Counter A32 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA84h

This register enables the current live value of performance counter A32 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAGAggregatePerfCounterA33

OAG_OAPERF_A33 - OAGAggregatePerfCounterA33		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DA88h	
This register reflects the count value of the OA Performance counter A33.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAGAggregatePerfCounterA33UpperDWord

OAG_OAPERF_A33_UPPER - OAGAggregatePerfCounterA33UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA8Ch

This register enables the current live value of performance counter A33 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAGAggregatePerfCounterA34

OAG_OAPERF_A34 - OAGAggregatePerfCounterA34		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DB60h	
This register reflects the count value of the OA Performance counter A34		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAGAggregatePerfCounterA34UpperDWord

OAG_OAPERF_A34_UPPER - OAGAggregatePerfCounterA34UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB64h

This register enables the current live value of performance counter A34 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAGAggregatePerfCounterA35

OAG_OAPERF_A35 - OAGAggregatePerfCounterA35		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DB68h	
This register reflects the count value of the OA Performance counter A35.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAGAggregatePerfCounterA35UpperDWord

OAG_OAPERF_A35_UPPER - OAGAggregatePerfCounterA35UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB6Ch

This register enables the current live value of performance counter A35 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OAG Aggregate Perf Counter A36

OAG_OAPERF_A36 - OAG Aggregate Perf Counter A36		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DB20h	
This register reflects the count value of the OA Performance counter A36.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter A37

OAG_OAPERF_A37 - OAG Aggregate Perf Counter A37		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DB28h	
This register reflects the count value of the OA Performance counter A37.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM0 Lower DWord Free

OAG_OAPERF_SPM0_LOWER_FREE - OAG Aggregate Perf Counter SPM0 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB30h

This register counts the same event as counter SPM0 however is not affected by context ID or other conditions that prevent SPM0 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO,so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM0 Upper DWord Free

OAG_OAPERF_SPM0_UPPER_FREE - OAG Aggregate Perf Counter SPM0 Upper DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB34h

This register counts the same event as counter SPM0 however is not affected by context ID or other conditions that prevent SPM0 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM1 Lower DWord Free

OAG_OAPERF_SPM1_LOWER_FREE - OAG Aggregate Perf Counter SPM1 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB38h

This register counts the same event as counter SPM1 however is not affected by context ID or other conditions that prevent SPM1 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM1 Upper DWord Free

OAG_OAPERF_SPM1_UPPER_FREE - OAG Aggregate Perf Counter SPM1 Upper DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB3Ch

This register counts the same event as counter SPM1 however is not affected by context ID or other conditions that prevent SPM1 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.; Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM2 Lower DWord Free

OAG_OAPERF_SPM2_LOWER_FREE - OAG Aggregate Perf Counter SPM2 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB40h

This register counts the same event as counter SPM2 however is not affected by context ID or other conditions that prevent SPM2 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM2 Upper DWord Free

OAG_OAPERF_SPM2_UPPER_FREE - OAG Aggregate Perf Counter SPM2 Upper DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB44h

This register counts the same event as counter SPM2 however is not affected by context ID or other conditions that prevent SPM2 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.; Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM3 Lower DWord Free

OAG_OAPERF_SPM3_LOWER_FREE - OAG Aggregate Perf Counter SPM3 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB48h

This register counts the same event as counter SPM3 however is not affected by context ID or other conditions that prevent SPM3 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM3 Upper DWord Free

OAG_OAPERF_SPM3_UPPER_FREE - OAG Aggregate Perf Counter SPM3 Upper DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB4Ch

This register counts the same event as counter SPM3 however is not affected by context ID or other conditions that prevent SPM3 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.; Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM4 Lower DWord Free

OAG_OAPERF_SPM4_LOWER_FREE - OAG Aggregate Perf Counter SPM4 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB50h

This register counts the same event as counter SPM4 however is not affected by context ID or other conditions that prevent SPM4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO,so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM4 Upper DWord Free

OAG_OAPERF_SPM4_UPPER_FREE - OAG Aggregate Perf Counter SPM4 Upper DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB54h

This register counts the same event as counter SPM4 however is not affected by context ID or other conditions that prevent SPM4 from incrementing. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.; Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM5 Lower DWord Free

OAG_OAPERF_SPM5_LOWER_FREE - OAG Aggregate Perf Counter SPM5 Lower DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB58h

Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted used this register. This counter is free running, always enabled and counts irrespective of OA enable configuration.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Aggregate Perf Counter SPM5 Upper DWord Free

OAG_OAPERF_SPM5_UPPER_FREE - OAG Aggregate Perf Counter SPM5 Upper DWord Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB5Ch

Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is counted using this register. This counter is free running, always enabled and counts irrespective of OA enable configuration.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Any Media Fixed Function 0 Wake Count Free

OAG_ANY_MEDIA_FF0_WAKE_COUNT_FREE - OAG Any Media Fixed Function 0 Wake Count Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBA8h

This register counts the number of media fixed function wake events for Media FF0. This counter is free running, always enabled and counts irrespective of OA being enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Any Media Fixed Function 1 Wake Count Free

OAG_ANY_MEDIA_FF1_WAKE_COUNT_FREE - OAG Any Media Fixed Function 1 Wake Count Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBB8h

This register counts the number of media fixed function wake events. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Any Media Fixed Function Busy Free

OAG_ANY_MEDIA_FF_BUSY_FREE - OAG Any Media Fixed Function Busy Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBA0h

This register counts the time that any media fixed function is busy. This counter is free running, always enabled and counts irrespective of OA being enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG BLT Busy Free

OAG_BLT_BUSY_FREE - OAG BLT Busy Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBBCh

This register counts the time that BLT engine is busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG BLT Wake Count Free

OAG_BLT_WAKE_COUNT_FREE - OAG BLT Wake Count Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBC0h

This register counts the number of times that BLT wakes up. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Boolean Counter B0

OAG_OAPERF_B0 - OAG Boolean Counter B0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA94h

This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Boolean Counter B1

OAG_OAPERF_B1 - OAG Boolean Counter B1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA98h

This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Boolean Counter B2

OAG_OAPERF_B2 - OAG Boolean Counter B2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DA9Ch

This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Boolean Counter B3

OAG_OAPERF_B3 - OAG Boolean Counter B3	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAA0h

This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Boolean Counter B4

OAG_OAPERF_B4 - OAG Boolean Counter B4	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAA4h

This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Boolean Counter B5

OAG_OAPERF_B5 - OAG Boolean Counter B5			
Register Space:	MMIO: 0/2/0		
Access:	R/W		
Size (in bits):	32		
Address:	0DAA8h		
This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.			
DWord	**Bit**	**Description**	
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.	

OAG Boolean Counter B6

OAG_OAPERF_B6 - OAG Boolean Counter B6	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAACh

This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Boolean Counter B7

OAG_OAPERF_B7 - OAG Boolean Counter B7

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAB0h

This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Context Control

OAG_OAGLBCTXCTRL - OAG Context Control

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02B28h

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: PBC _Custom_GTIReset: DEV
	7:2	**Timer Period** Default Value: 00b Access: R/W Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: Strobe Period = MinimumTimeStampPeriod * 2 **(TimerPeriod + 1)** The exponent is defined by this field. **Programming Notes** **Note:** The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full Strobe Period elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.
	1	**Timer Enable** Access: R/W This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. **Value** / **Name** / **Description** 0 / Disable **[Default]** / Counter does not get written out on regular interval 1 / Enable / Counter gets written out on regular intervals, defined by the Timer Period

OAG_OAGLBCTXCTRL - OAG Context Control

		Programming Notes When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts.
	0	**Counter Stop-Resume Mechanism** Access: R/W Counter stop-resume mechanism

Value	Name	Description
1	Resume	Resume counting for all counters

OAG Customizable Event Creation 0-0

OAG_CEC00 - OAG Customizable Event Creation 0-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D940h

Description
This register is used to define custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b / Reserved /

OAG_CEC00 - OAG Customizable Event Creation 0-0

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 1-0

OAG_CEC10 - OAG Customizable Event Creation 1-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D948h

Description
This register is used to define custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b – Reserved –

OAG_CEC10 - OAG Customizable Event Creation 1-0

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 1-1

OAG_CEC11 - OAG Customizable Event Creation 1-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D94Ch

Description
This register configures the input conditioning portion of CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. Value / Name / Description 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. Value / Name / Description 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OAG Customizable Event Creation 2-0

OAG_CEC20 - OAG Customizable Event Creation 2-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D950h

Description
This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b – Reserved –

OAG_CEC20 - OAG Customizable Event Creation 2-0

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 2-1

OAG_CEC21 - OAG Customizable Event Creation 2-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D954h

Description
This register configures the input conditioning portion of CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAG Customizable Event Creation 3-0

OAG_CEC30 - OAG Customizable Event Creation 3-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D958h

Description
This register is used to define custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b – Reserved –

OAG_CEC30 - OAG Customizable Event Creation 3-0

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 3-1

OAG_CEC31 - OAG Customizable Event Creation 3-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D95Ch

Description
This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAG Customizable Event Creation 4-0

OAG_CEC40 - OAG Customizable Event Creation 4-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D960h

Description
This register is used to define custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b – Reserved –

OAG_CEC40 - OAG Customizable Event Creation 4-0

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 5-0

OAG_CEC50 - OAG Customizable Event Creation 5-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D968h

Description
This register is used to define custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b – Reserved –

OAG_CEC50 - OAG Customizable Event Creation 5-0

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 5-1

OAG_CEC51 - OAG Customizable Event Creation 5-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D96Ch

Description
This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAG Customizable Event Creation 6-0

OAG_CEC60 - OAG Customizable Event Creation 6-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D970h

Description
This register is used to define custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b – Reserved –

OAG_CEC60 - OAG Customizable Event Creation 6-0

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 6-1

OAG_CEC61 - OAG Customizable Event Creation 6-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D974h

Description
This register configures the input conditioning portion of CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAG Customizable Event Creation 7-0

OAG_CEC70 - OAG Customizable Event Creation 7-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D978h

Description
This register is used to define custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b – Reserved –

OAG_CEC70 - OAG Customizable Event Creation 7-0

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Customizable Event Creation 7-1

OAG_CEC71 - OAG Customizable Event Creation 7-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D97Ch

Description
This register configures the input conditioning portion of CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.
This register can be used to customize counters for events from both unslice and slice units.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAG GPU Ticks Counter

OAG_GPU_TICKS - OAG GPU Ticks Counter		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DB70h	
Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG GPU Ticks Counter Upper DWord

OAG_GPU_TICKS_UPPER - OAG GPU Ticks Counter Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB74h

Reading this register returns the live value of the Upper DWord of GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG GTI Busy Free

OAG_GTI_BUSY_FREE - OAG GTI Busy Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBCCh

This register counts the time that any engine residing in GTI(currently WG, BLT, or GuC) is busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG GTI Wake Count Free

OAG_GTI_WAKE_COUNT_FREE - OAG GTI Wake Count Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBD0h

This register counts the number of times that GTI wakes up due to one of the engines resident in GTI (currently WG, BLT, and GuC) becoming busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG GuC Busy Free

OAG_GUC_BUSY_FREE - OAG GuC Busy Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBC4h

This register counts the time that GuC is busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG GuC Wake Count Free

OAG_GUC_WAKE_COUNT_FREE - OAG GuC Wake Count Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBC8h

This register counts the number of times that GuC wakes up. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Interrupt Mask Register

OAG_OA_IMR - OAG Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB14h

The OAIMR register is used by software to control whether OA generates an interrupt or not.

DWord	Bit	Description
0	31:29	**Reserved** Default Value: 7h Access: R/W Format: PBC _Custom_GTIReset: DEV
	28	**Mask Bit** Access: R/W _Custom_GTIReset: DEV 0h – Not Masked – May generate an interrupt 1h – Masked **[Default]** – Will not generate an interrupt
	27:0	**Reserved** Default Value: FFFFFFFh Access: R/W Format: PBC _Custom_GTIReset: DEV

OAG L3Node Customizable Event Creation 0-0

OAG_LCEC0_0 - OAG L3Node Customizable Event Creation 0-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD00h

This register is used to define the slice custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_LCEC0_0 - OAG L3Node Customizable Event Creation 0-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG L3Node Customizable Event Creation 1-0

OAG_LCEC1_0 - OAG L3Node Customizable Event Creation 1-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD08h

This register is used to define slice custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_LCEC1_0 - OAG L3Node Customizable Event Creation 1-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG L3Node Customizable Event Creation 1-1

OAG_LCEC1_1 - OAG L3Node Customizable Event Creation 1-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD0Ch

This register configures the input conditioning portion of slice CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. **Value** / **Name** / **Description** 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. **Value** / **Name** / **Description** 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OAG L3Node Customizable Event Creation 2-0

OAG_LCEC2_0 - OAG L3Node Customizable Event Creation 2-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD10h

This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_LCEC2_0 - OAG L3Node Customizable Event Creation 2-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG L3Node Customizable Event Creation 2-1

OAG_LCEC2_1 - OAG L3Node Customizable Event Creation 2-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD14h

This register configures the input conditioning portion of slice CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. **Value** / **Name** / **Description** 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. **Value** / **Name** / **Description** 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OAG L3Node Customizable Event Creation 3-0

OAG_LCEC3_0 - OAG L3Node Customizable Event Creation 3-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD18h

This register is used to define slice custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_LCEC3_0 - OAG L3Node Customizable Event Creation 3-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG L3Node Customizable Event Creation 3-1

OAG_LCEC3_1 - OAG L3Node Customizable Event Creation 3-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD1Ch

This register configures the input conditioning portion of Slice CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAG L3Node Customizable Event Creation 4-0

OAG_LCEC4_0 - OAG L3Node Customizable Event Creation 4-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD20h

This register is used to define slice custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). 01b – Prev Event – Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b – Reserved –
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_LCEC4_0 - OAG L3Node Customizable Event Creation 4-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG L3Node Customizable Event Creation 5-0

OAG_LCEC5_0 - OAG L3Node Customizable Event Creation 5-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD28h

This register is used to define slice custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_LCEC5_0 - OAG L3Node Customizable Event Creation 5-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG L3Node Customizable Event Creation 5-1

OAG_LCEC5_1 - OAG L3Node Customizable Event Creation 5-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD2Ch

This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.

Value	Name	Description
0b	Live	Input bit is not delayed by 1 clock before event calculation
1b	Delayed	Input bit is delayed by 1 clock before event calculation

DWord	Bit	Description
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.

Value	Name	Description
0b	Unmasked	Input bit is considered in event calculation
1b	Masked	Input bit is ignored in event calculation

OAG L3Node Customizable Event Creation 6-0

OAG_LCEC6_0 - OAG L3Node Customizable Event Creation 6-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD30h

This register is used to define slice custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_LCEC6_0 - OAG L3Node Customizable Event Creation 6-0

	2:0	**Compare Function** Access: R/W Format: U3 _Custom_GTIReset: DEV This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG L3Node Customizable Event Creation 6-1

OAG_LCEC6_1 - OAG L3Node Customizable Event Creation 6-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD34h

This register configures the input conditioning portion of slice CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:16</td><td>Considerations
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Live</td><td>Input bit is not delayed by 1 clock before event calculation</td></tr>
<tr><td>1b</td><td>Delayed</td><td>Input bit is delayed by 1 clock before event calculation</td></tr>
</table></td></tr>
<tr><td></td><td>15:0</td><td>Mask
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Unmasked</td><td>Input bit is considered in event calculation</td></tr>
<tr><td>1b</td><td>Masked</td><td>Input bit is ignored in event calculation</td></tr>
</table></td></tr>
</table>

OAG L3Node Customizable Event Creation 7-0

OAG_LCEC7_0 - OAG L3Node Customizable Event Creation 7-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD38h

This register is used to define slice custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_LCEC7_0 - OAG L3Node Customizable Event Creation 7-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG L3Node Customizable Event Creation 7-1

OAG_LCEC7_1 - OAG L3Node Customizable Event Creation 7-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DD3Ch

This register configures the input conditioning portion of slice CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:16</td><td>Considerations
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Live</td><td>Input bit is not delayed by 1 clock before event calculation</td></tr>
<tr><td>1b</td><td>Delayed</td><td>Input bit is delayed by 1 clock before event calculation</td></tr>
</table></td></tr>
<tr><td></td><td>15:0</td><td>Mask
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Unmasked</td><td>Input bit is considered in event calculation</td></tr>
<tr><td>1b</td><td>Masked</td><td>Input bit is ignored in event calculation</td></tr>
</table></td></tr>
</table>

OAG MCPG0 Hysteresis Time Free

OAG_MCPG0_HYSTERESIS_TIME_FREE - OAG MCPG0 Hysteresis Time Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBA4h

This register counts the time that MCPG hysteresis time is accumulating for media slice 0. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Media Sampler Really Busy Free

OAG_MEDIA_SAMPLER_REALLY_BUSY_FREE - OAG Media Sampler Really Busy Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBACh

This register counts the time that media sampler is really busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Media Sampler Wake Count Free

OAG_MEDIA_SAMPLER_WAKE_COUNT_FREE - OAG Media Sampler Wake Count Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBB0h

This register counts the number of times that media sampler wakes up. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG MMIO Trigger

OAG_MMIO_TRG - OAG MMIO Trigger		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DB1Ch	
Writing in this register triggers a report in OAG. The reports are stored in the OA Buffer space.		
DWord	**Bit**	**Description**
0	31:0	**Unique ID** Access: R/W Format: U32 _Custom_GTIReset: DEV This field is inserted as such into the Context ID field of the report generated due to the write to this register. Report gets triggered irrespective of the value written into this register. By uniquely maintaining this value for every trigger, user can uniquely identify various reports.

OAG Observation Architecture Buffer

OAG_OABUFFER - OAG Observation Architecture Buffer

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB08h

This register is used to program the OA unit.

Programming Notes

This MMIO must be set before the OATAILPTR register and set after the OAHEADPTR register. This is to enable proper functionality of the overflow bit.

DWord	Bit	Description
0	31:6	**Report Buffer Offset** Access: R/W _Custom_GTIReset: DEV This field specifies 64B aligned GFX MEM address where the chap counter values are reported.
	5:3	**Inter Trigger Report Buffer Size** Access: R/W _Custom_GTIReset: DEV **Description** This field indicates the size of report buffer for time/event-based report trigger mechanisms.

Value	Name	Description
0h	128 KB or 1MB **[Default]**	All context considered.
1h	256 KB or 2MB	
2h	512 KB or 4MB	
3h	1 MB or 8MB	
4h	2 MB or 16MB	
5h	4 MB or 32MB	
6h	8 MB or 64MB	
7h	16 MB or 128MB	

OAG_OABUFFER - OAG Observation Architecture Buffer

2 **OA Report Trigger Select**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
0		Level Report trigger
1		Edge Report trigger

1 **Disable Overrun Mode**

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

This field defines the mode of reporting for internal trigger/timer based reporting. When this bit is set, overrun does not lose reports but stops reporting. Based on the head and tail pointer, when HW detects room for the report, it would resume reporting to the buffer. This mode would not set the over-run bit in the register. When this mode bit is reset, buffer overrun can happen and lose the reports while setting the buffer over-run bit.

Value	Name	Description
0h	Disable **[Default]**	Counter gets written out on regular intervals, defined by the Timer Period
1h	Enable	Counter does not get written out on regular interval

0 **Memory Select PPGTT/GGTT Access**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0h	PPGTT
1h	GGTT **[Default]**

Programming Notes
When each context has its own Per Process GTT, this field should be always set to GGTT.

OAG Observation Architecture Control

OAG_OACONTROL - OAG Observation Architecture Control

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAF4h

This register controls global OA functionality, report format, interrupt steering and context filtering.

DWord	Bit	Description
0	31:18	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	17:16	**CCS Select for Perf Mon** Access: R/W _Custom_GTIReset: DEV This field selects CCS to be performance monitored (through OAC). 00b: CCS0 **[Default]** 01b: CCS1 10b: CCS2 11b: CCS3 **Programming Notes** CCS0-CCS3 can be selected through CCS Select for Perf Mon value of 00b-11b. CCS Context and/or Workload serialization is recommended for Profiling using this programmable field. s/r of counters to have no obvious meaning in non-serialized usages with ccs hw context switches as there is only one copy of counters.
	15:8	**Reserved** Access: R/W
	7	**Reserved** Access: R/W

OAG_OACONTROL - OAG Observation Architecture Control

6	**OA Context control select**

Access:	R/W
_Custom_GTIReset:	DEV

Description
This field is obsolete Bit field to indicate which context control inputs are to be chosen in the OACS

Value	Name	Description
0	OAG RCS Select **[Default]**	Select the OA context control from RCS (Default)
1	Global	Select the Global OA context control

5	**Interrupt Steering Bit**

Access:	R/W
_Custom_GTIReset:	DEV

When set, OACS unit sends interrupt messages to the SHIM of the GUC through message channel. When reset, OACS unit sends the interrupt message to Display Engine as config writes on GAM interface.

4:2	**Counter Select**

Access:	R/W
_Custom_GTIReset:	DEV

This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.

1	**Reserved**

Access:	RO
Format:	MBZ

0	**Performance Counter Enable**

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear.

Programming Notes
When this bit is set, OABUFFER, OAHEADPTR and OATAILPTR must be programmed correctly to ensure report triggers due to Context Switch and GO transition happen correctly.

OAG Observation Architecture Report Trigger 2

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D924h

This register controls some of the Boolean logic defining Boolean/threshold report trigger 0. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are ORed to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	**Report Trigger Enable** Access: R/W Format: Enable _Custom_GTIReset: DEV Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.
	30:24	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

	23	**Threshold Enable** Access: R/W Format: Enable _Custom_GTIReset: DEV Enable the threshold compare logic within the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	22	**Invert D Enable 0** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the D stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	21	**Invert C Enable 1** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	20	**Invert C Enable 0** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	19	**Invert B Enable 3** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

	18	**Invert B Enable 2** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	14	**Invert A Enable 14** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

	12	**Invert A Enable 12** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	11	**Invert A Enable 11** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	10	**Invert A Enable 10** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	9	**Invert A Enable 9** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	8	**Invert A Enable 8** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

	7	**Invert A Enable 7** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	6	**Invert A Enable 6** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG2 - OAG Observation Architecture Report Trigger 2

	2	**Invert A Enable 2** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAG Observation Architecture Report Trigger 6

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D934h

This register controls some of the Boolean logic defining Boolean/threshold report trigger 1. Note that Boolean report triggers 0 and 1 are logically OR'd together without buffering, this implies that only one performance counter report will be generated for clocks where both Boolean report triggers evaluate true. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are OR'd to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	**Report Trigger Enable** Access: R/W _Custom_GTIReset: DEV Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.
	30:24	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6

	23	**Threshold Enable** Access: R/W _Custom_GTIReset: DEV Enable the threshold compare logic within the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	22	**Invert D Enable 0** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the D stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	21	**Invert C Enable 1** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	20	**Invert C Enable 0** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	19	**Invert B Enable 3** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	18	**Invert B Enable 2** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6

	16	**Invert B Enable 0** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	14	**Invert A Enable 14** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	12	**Invert A Enable 12** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	11	**Invert A Enable 11** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	10	**Invert A Enable 10** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6

	9	**Invert A Enable 9** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	8	**Invert A Enable 8** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	7	**Invert A Enable 7** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	6	**Invert A Enable 6** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAG_OAREPORTTRIG6 - OAG Observation Architecture Report Trigger 6

	2	**Invert A Enable 2** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAG Observation Architecture Report Trigger Counter

OAG_OARPTTRIG_COUNTER - OAG Observation Architecture Report Trigger Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB10h

This register provides status of report trigger threshold count 1 and 2. This register is for HW internal purpose and power context save/restored. This register must not be programmed by SW.

DWord	Bit	Description
0	31:16	**Report Trig Threshold Count 1 Status** Access: R/W _Custom_GTIReset: DEV **Programming Notes** This field is for HW internal use to context save/restore rpt trigger threshold count 1. It always indicates current value of HW's internal report trigger count. SW should not program these bits.
	15:0	**Report Trig Threshold count 2 status** Access: R/W _Custom_GTIReset: DEV **Programming Notes** This field is for HW internal use to context save/restore rpt trigger threshold count 2. It always indicates current value of HW's internal report trigger count. SW should not program these bits.

OAG Observation Architecture Start Trigger 5

OAG_OASTARTTRIG5 - OAG Observation Architecture Start Trigger 5

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0D910h

This register provides the threshold value optionally used to define the start trigger for B7-B4 counters. Note that the value in this register must match the value in OASTARTTRIG1 to have B7-B0 start at the same time. The bit definition in this register refers to the stages in the start trigger block diagram in the Performance Counter Reporting section.

DWord	Bit	Description
0	31:16	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	15:0	**Threshold Value** Access: R/W Format: U16 _Custom_GTIReset: DEV **Programming Notes** Threshold value for the compare logic within the start trigger logic for B7-B4 counters.

OAG Observation Architecture Start Trigger Counter

OAG_OASTARTTRIG_COUNTER - OAG Observation Architecture Start Trigger Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB0Ch

This register provides status of start trigger threshold count 1 and 2. This register is for HW internal purpose.

DWord	Bit	Description
0	31:16	**Start Trig Threshold Count 1 Status** Access: R/W _Custom_GTIReset: DEV **Programming Notes** This field is for HW internal use to context save/restore start trigger threshold count 1. It always indicates current value of HW's internal start trigger count. SW should not program these bits.
	15:0	**Start Trig Threshold count 2 status** Access: R/W _Custom_GTIReset: DEV **Programming Notes** : This field is for HW internal use to context save/restore start trigger threshold count 2. It always indicates current value of HW's internal start trigger count. SW should not program these bits.

OAG Observation Architecture Status Register

OAG_OASTATUS - OAG Observation Architecture Status Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DAFCh

This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits. Status bits are active high flags (0=false, 1=true)

DWord	Bit	Description
0	31:22	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	21	**Start Trigger Flag 1** Access: R/W _Custom_GTIReset: DEV Value / Name: 0 **[Default]**; 1 **Programming Notes**: This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.
	20	**Start Trigger Flag 2** Access: R/W _Custom_GTIReset: DEV Value / Name: 0 **[Default]**; 1 **Programming Notes**: This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.

OAG_OASTATUS - OAG Observation Architecture Status Register

19 **Report Trigger Flag 1**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0	**[Default]**
1	

Programming Notes
This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.

18 **Report Trigger Flag 2**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0	**[Default]**
1	

Programming Notes
This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.

17 **Tail Pointer Wrap Flag**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Value	Name
0	
1	**[Default]**

Programming Notes
This bit is for HW internal use to context save /restore Tail Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Tail Pointer Wrap Mask bit is set.

OAG_OASTATUS - OAG Observation Architecture Status Register

16 **Head Pointer Wrap Flag**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Value	Name
0	
1	**[Default]**

Programming Notes
This bit is for HW internal use to context save /restore Head Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Head Pointer Wrap Mask bit is set.

15:7 **Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

6 **MMIO Trigger Queue Full**

Access:	R/W
Format:	Boolean
_Custom_GTIReset:	DEV

This bit is set if MMIO Trigger FIFO in HW becomes full. This bit can be reset by SW by either soft reset or writing a 0 to it.

Value	Name	Description
0h	**[Default]**	MMIO Trigger Queue is not full
1h		MMIO Trigger Queue is full

5 **Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

4 **Accumulator Overflow**

Access:	R/W
_Custom_GTIReset:	DEV

This field indicates that the one or more event accumulator inside the slice-OAunit has overflowed. Once set, this bit will remain set, until SW resets it by either soft reset or writing a 0 to it.

Value	Name	Description
0	**[Default]**	No overflow has occurred.
1		Overflow has occurred.

OAG_OASTATUS - OAG Observation Architecture Status Register

3 **Overrun Status**

Access:	R/W
_Custom_GTIReset:	DEV

This field indicates the status of overrun. This bit is read only and writing to this bit will have no effect. This bit will reflect the status of overrun irrespective of Overrun Mode enabled or disabled.

Value	Name	Description
0	**[Default]**	No overrun has occurred
1		Overrun has occurred

2 **Counter Overflow**

Access:	R/W
_Custom_GTIReset:	DEV

This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 0 to it.

Value	Name	Description
0	**[Default]**	Counter Overflow Not Occurred
1		Counter Overflow Occurred

1 **Buffer Overflow**

Access:	R/W
_Custom_GTIReset:	DEV

This bit is set when the Tail-pointer - Head pointer > max internal trigger buffer size

Value	Name	Description
0h	**[Default]**	Buffer Overflow Not Occurred
1		Buffer Overflow Occurred

0 **Report Lost Error**

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

This bit is set if the Report Trigger due to "Internal Report Trigger-1", "Internal Report Trigger-2" or "Timer Triggered" or "MMIO Trigger" to write out the counter values is dropped, while there is an ongoing report in progress. The report request is ignored and the counter continue to count. This bit will be set along with this MMIO Trigger Queue Full, in case of dropped request for MMIO trigger.

Value	Name	Description
0	**[Default]**	Report Lost Error Not Occurred
1		Report Lost Error Occurred

Programming Notes
This bit can be reset by SW by either soft reset or writing a 0 to it.

OAG Observation Architecture Tail Pointer

OAG_OATAILPTR - OAG Observation Architecture Tail Pointer

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB04h

This register allows software to program tail pointer and also indicates current tail pointer value.

DWord	Bit	Description
0	31:6	**Tail Pointer** Access: R/W _Custom_GTIReset: DEV Virtual address of the internal trigger based buffer that is updated for every 64B cacheline write to memory when reporting via internal report trigger. This pointer will not be updated for MI_REPORT_PERF_COUNT command based writes. **Programming Notes** Before enabling internally triggered performance counter reporting, SW must ensure that this address matches the Report Buffer Offset programmed in OABUFFER register (i.e. tail pointer must start at the beginning of the report buffer). SW must ensure that Tail pointer and the Head Pointer match before enabling internally triggered performance counter reporting.
	5:0	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OAG RC0 Any Engine Busy Free

OAG_RC0_ANY_ENGINE_BUSY_FREE - OAG RC0 Any Engine Busy Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB80h

This register counts the time that any engine is truly busy (not simply powered up). This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO,so the value returned from this register may be different on back-to-back reads. Unit in GPMusec. Refer to **Timestamp Bases** for details.

OAG RC0 Clocks Free

OAG_RC0_CLOCKS_FREE - OAG RC0 Clocks Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB90h

This register counts the clocks that GFX has been in RC0 in increments of 64 GFX clocks. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read.Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO,so the value returned from this register may be different on back-to-back reads.

OAG RC0 Hysteresis Free

OAG_RC0_HYSTERISIS_FREE - OAG RC0 Hysteresis Free	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	0DB84h

This register counts the time that any engine is truly busy (not simply powered up). This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: RO _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG RC0 Wake Count Free

OAG_RC0_WAKE_COUNT_FREE - OAG RC0 Wake Count Free		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	0DB88h	
This counter is free running, always enabled and counting irrespective of OA enabled or disabled.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: RO _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG RC6 Entry Count Free

OAG_RC6_ENTRY_COUNT_FREE - OAG RC6 Entry Count Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB9Ch

This register counts number rc6 entries. This counter is free running, always enabled and counting irrespective of OA enabled or disabled. This is an RPM mirrored register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG RC6 Pre Engine Wake Overhead Free

OAG_RC6_PRE_ENGINE_WAKE_OVERHEAD_FREE - OAG RC6 Pre Engine Wake Overhead Free	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	0DB8Ch

This register counts the time between boot complete and Go=1. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: RO _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG RCPG Hysteresis Time Free

OAG_RCPG_HYSTERESIS_TIME_FREE - OAG RCPG Hysteresis Time Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBE0h

This register counts the time RCPG hysteresis count is accumulating. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Render Busy Free

OAG_RENDER_BUSY_FREE - OAG Render Busy Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBDCh

This register counts the time that any render engine is busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Render Wake Count Free

OAG_RENDER_WAKE_COUNT_FREE - OAG Render Wake Count Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBE4h

This register counts the number of render wakes that have occurred. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Slice Customizable Event Creation 0-0

OAG_SCEC0_0 - OAG Slice Customizable Event Creation 0-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC00h

This register is used to define the slice custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_SCEC0_0 - OAG Slice Customizable Event Creation 0-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 1-0

OAG_SCEC1_0 - OAG Slice Customizable Event Creation 1-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC08h

This register is used to define slice custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_SCEC1_0 - OAG Slice Customizable Event Creation 1-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 1-1

OAG_SCEC1_1 - OAG Slice Customizable Event Creation 1-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC0Ch

This register configures the input conditioning portion of slice CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAG Slice Customizable Event Creation 2-0

OAG_SCEC2_0 - OAG Slice Customizable Event Creation 2-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC10h

This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_SCEC2_0 - OAG Slice Customizable Event Creation 2-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 2-1

OAG_SCEC2_1 - OAG Slice Customizable Event Creation 2-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC14h

This register configures the input conditioning portion of slice CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td rowspan="2">0</td><td>31:16</td><td>Considerations
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Live</td><td>Input bit is not delayed by 1 clock before event calculation</td></tr>
<tr><td>1b</td><td>Delayed</td><td>Input bit is delayed by 1 clock before event calculation</td></tr>
</table></td></tr>
<tr><td>15:0</td><td>Mask
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Unmasked</td><td>Input bit is considered in event calculation</td></tr>
<tr><td>1b</td><td>Masked</td><td>Input bit is ignored in event calculation</td></tr>
</table></td></tr>
</table>

OAG Slice Customizable Event Creation 3-0

OAG_SCEC3_0 - OAG Slice Customizable Event Creation 3-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC18h

This register is used to define slice custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_SCEC3_0 - OAG Slice Customizable Event Creation 3-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 3-1

OAG_SCEC3_1 - OAG Slice Customizable Event Creation 3-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC1Ch

This register configures the input conditioning portion of Slice CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. **Value / Name / Description** 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. **Value / Name / Description** 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OAG Slice Customizable Event Creation 4-0

OAG_SCEC4_0 - OAG Slice Customizable Event Creation 4-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC20h

This register is used to define slice custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_SCEC4_0 - OAG Slice Customizable Event Creation 4-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 5-0

OAG_SCEC5_0 - OAG Slice Customizable Event Creation 5-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC28h

This register is used to define slice custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_SCEC5_0 - OAG Slice Customizable Event Creation 5-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 5-1

OAG_SCEC5_1 - OAG Slice Customizable Event Creation 5-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC2Ch

This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. **Value / Name / Description** 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. **Value / Name / Description** 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OAG Slice Customizable Event Creation 6-0

OAG_SCEC6_0 - OAG Slice Customizable Event Creation 6-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC30h

This register is used to define slice custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_SCEC6_0 - OAG Slice Customizable Event Creation 6-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 6-1

OAG_SCEC6_1 - OAG Slice Customizable Event Creation 6-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC34h

This register configures the input conditioning portion of slice CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:16</td><td>Considerations
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Live</td><td>Input bit is not delayed by 1 clock before event calculation</td></tr>
<tr><td>1b</td><td>Delayed</td><td>Input bit is delayed by 1 clock before event calculation</td></tr>
</table></td></tr>
<tr><td></td><td>15:0</td><td>Mask
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Unmasked</td><td>Input bit is considered in event calculation</td></tr>
<tr><td>1b</td><td>Masked</td><td>Input bit is ignored in event calculation</td></tr>
</table></td></tr>
</table>

OAG Slice Customizable Event Creation 7-0

OAG_SCEC7_0 - OAG Slice Customizable Event Creation 7-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC38h

This register is used to define slice custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. **Value** / **Name** / **Description** 0b / Pass-through / Input bit is passed through to comparator as is 1b / Negated / Input bit is negated before passing to comparator
	20:19	**Source Select** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section). **Value** / **Name** / **Description** 01b / Prev Event / Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block 11b / Reserved /
	18:3	**Compare Value** Access: R/W Format: U16 _Custom_GTIReset: DEV The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

OAG_SCEC7_0 - OAG Slice Customizable Event Creation 7-0

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAG Slice Customizable Event Creation 7-1

OAG_SCEC7_1 - OAG Slice Customizable Event Creation 7-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DC3Ch

This register configures the input conditioning portion of slice CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. **Value / Name / Description** 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. **Value / Name / Description** 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OAG SQ Full Occupancy count Free

OAG_SQ_FULL_OCCUPANCY_COUNT_FREE - OAG SQ Full Occupancy count Free	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB98h

This register counts the number of GFX clocks that SQ was full. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG SQ Memory Bound Stall count Free

OAG_SQ_MBSTALL_COUNT_FREE - OAG SQ Memory Bound Stall count Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB94h

This register counts the number of GFX clocks that SQ read has been stalled. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Unslice Busy Free

OAG_UNSLICE_BUSY_FREE - OAG Unslice Busy Free

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DBD4h

This register counts the number of times that unslice wakes up due to any unslice engine (currently WG, BLT, GuC, and media fixed functions) becoming busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAG Unslice Wake Count Free

OAG_UNSLICE_WAKE_COUNT_FREE - OAG Unslice Wake Count Free		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0DBD8h	
This register counts the number of times that unslice wakes up due to any unslice engine (currently WG, BLT, GuC, and media fixed functions)becoming busy. This counter is free running, always enabled and counting irrespective of OA enabled or disabled.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Aggregate Perf Counter A36

OAM_OAPERF_A36 - OAM Aggregate Perf Counter A36

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	130C4h-130C7h
Name:	Aggregate Perf Counter 36
ShortName:	AGG_PERF_COUNTER_A36_MEDIA_SLICE_0_OA
Address:	132C4h-132C7h
Name:	Aggregate Perf Counter 36
ShortName:	AGG_PERF_COUNTER_A36_MEDIA_SLICE_1_OA
Address:	136C4h-136C7h
Name:	Aggregate Perf Counter 36
ShortName:	AGG_PERF_COUNTER_A36_MEDIA_SLICE_3_OA

This register reflects the count value of the OA Performance counter A36.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Aggregate Perf Counter A37

OAM_OAPERF_A37 - OAM Aggregate Perf Counter A37	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	130CCh-130CFh
Name:	Aggregate Perf Counter 37
ShortName:	AGG_PERF_COUNTER_A37_MEDIA_SLICE_0_OA
Address:	132CCh-132CFh
Name:	Aggregate Perf Counter 37
ShortName:	AGG_PERF_COUNTER_A37_MEDIA_SLICE_1_OA
Address:	134CCh-134CFh
Name:	Aggregate Perf Counter 37
ShortName:	AGG_PERF_COUNTER_A37_MEDIA_SLICE_2_OA
Address:	136CCh-136CFh
Name:	Aggregate Perf Counter 37
ShortName:	AGG_PERF_COUNTER_A37_MEDIA_SLICE_3_OA

This register reflects the count value of the OA Performance counter A37.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Boolean_Counter_B0

OAM_OAPERF_B0 - OAM Boolean_Counter_B0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13084h-13087h
Name:	Boolean Counter B0
ShortName:	BOOLEAN_COUNTER_B0_MEDIA_SLICE_0_OA
Address:	13284h-13287h
Name:	Boolean Counter B0
ShortName:	BOOLEAN_COUNTER_B0_MEDIA_SLICE_1_OA
Address:	13484h-13487h
Name:	Boolean Counter B0
ShortName:	BOOLEAN_COUNTER_B0_MEDIA_SLICE_2_OA
Address:	13684h-13687h
Name:	Boolean Counter B0
ShortName:	BOOLEAN_COUNTER_B0_MEDIA_SLICE_3_OA

This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Boolean_Counter_B1

OAM_OAPERF_B1 - OAM Boolean_Counter_B1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13088h-1308Bh
Name:	Boolean Counter B1
ShortName:	BOOLEAN_COUNTER_B1_MEDIA_SLICE_0_OA
Address:	13288h-1328Bh
Name:	Boolean Counter B1
ShortName:	BOOLEAN_COUNTER_B1_MEDIA_SLICE_1_OA
Address:	13488h-1348Bh
Name:	Boolean Counter B1
ShortName:	BOOLEAN_COUNTER_B1_MEDIA_SLICE_2_OA
Address:	13688h-1368Bh
Name:	Boolean Counter B1
ShortName:	BOOLEAN_COUNTER_B1_MEDIA_SLICE_3_OA

This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Boolean_Counter_B2

OAM_OAPERF_B2 - OAM Boolean_Counter_B2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1308Ch-1308Fh
Name:	Boolean Counter B2
ShortName:	BOOLEAN_COUNTER_B2_MEDIA_SLICE_0_OA
Address:	1328Ch-1328Fh
Name:	Boolean Counter B2
ShortName:	BOOLEAN_COUNTER_B2_MEDIA_SLICE_1_OA
Address:	1348Ch-1348Fh
Name:	Boolean Counter B2
ShortName:	BOOLEAN_COUNTER_B2_MEDIA_SLICE_2_OA
Address:	1368Ch-1368Fh
Name:	Boolean Counter B2
ShortName:	BOOLEAN_COUNTER_B2_MEDIA_SLICE_3_OA

This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Boolean_Counter_B3

OAM_OAPERF_B3 - OAM Boolean_Counter_B3	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13090h-13093h
Name:	Boolean Counter B3
ShortName:	BOOLEAN_COUNTER_B3_MEDIA_SLICE_0_OA
Address:	13290h-13293h
Name:	Boolean Counter B3
ShortName:	BOOLEAN_COUNTER_B3_MEDIA_SLICE_1_OA
Address:	13490h-13493h
Name:	Boolean Counter B3
ShortName:	BOOLEAN_COUNTER_B3_MEDIA_SLICE_2_OA
Address:	13690h-13693h
Name:	Boolean Counter B3
ShortName:	BOOLEAN_COUNTER_B3_MEDIA_SLICE_3_OA

This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Boolean_Counter_B4

OAM_OAPERF_B4 - OAM Boolean_Counter_B4	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13094h-13097h
Name:	Boolean Counter B4
ShortName:	BOOLEAN_COUNTER_B4_MEDIA_SLICE_0_OA
Address:	13294h-13297h
Name:	Boolean Counter B4
ShortName:	BOOLEAN_COUNTER_B4_MEDIA_SLICE_1_OA
Address:	13494h-13497h
Name:	Boolean Counter B4
ShortName:	BOOLEAN_COUNTER_B4_MEDIA_SLICE_2_OA
Address:	13694h-13697h
Name:	Boolean Counter B4
ShortName:	BOOLEAN_COUNTER_B4_MEDIA_SLICE_3_OA

This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Boolean_Counter_B5

OAM_OAPERF_B5 - OAM Boolean_Counter_B5	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13098h-1309Bh
Name:	Boolean Counter B5
ShortName:	BOOLEAN_COUNTER_B5_MEDIA_SLICE_0_OA
Address:	13298h-1329Bh
Name:	Boolean Counter B5
ShortName:	BOOLEAN_COUNTER_B5_MEDIA_SLICE_1_OA
Address:	13498h-1349Bh
Name:	Boolean Counter B5
ShortName:	BOOLEAN_COUNTER_B5_MEDIA_SLICE_2_OA
Address:	13698h-1369Bh
Name:	Boolean Counter B5
ShortName:	BOOLEAN_COUNTER_B5_MEDIA_SLICE_3_OA

This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Boolean_Counter_B6

OAM_OAPERF_B6 - OAM Boolean_Counter_B6	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1309Ch-1309Fh
Name:	Boolean Counter B6
ShortName:	BOOLEAN_COUNTER_B6_MEDIA_SLICE_0_OA
Address:	1329Ch-1329Fh
Name:	Boolean Counter B6
ShortName:	BOOLEAN_COUNTER_B6_MEDIA_SLICE_1_OA
Address:	1349Ch-1349Fh
Name:	Boolean Counter B6
ShortName:	BOOLEAN_COUNTER_B6_MEDIA_SLICE_2_OA
Address:	1369Ch-1369Fh
Name:	Boolean Counter B6
ShortName:	BOOLEAN_COUNTER_B6_MEDIA_SLICE_3_OA

This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Boolean_Counter_B7

OAM_OAPERF_B7 - OAM Boolean_Counter_B7	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	130A0h-130A3h
Name:	Boolean Counter B7
ShortName:	BOOLEAN_COUNTER_B7_MEDIA_SLICE_0_OA
Address:	132A0h-132A3h
Name:	Boolean Counter B7
ShortName:	BOOLEAN_COUNTER_B7_MEDIA_SLICE_1_OA
Address:	134A0h-134A3h
Name:	Boolean Counter B7
ShortName:	BOOLEAN_COUNTER_B7_MEDIA_SLICE_2_OA
Address:	136A0h-136A3h
Name:	Boolean Counter B7
ShortName:	BOOLEAN_COUNTER_B7_MEDIA_SLICE_3_OA

This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Context Control

OAM_OACTXCTRL - OAM Context Control

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	131BCh-131BFh
Name:	OAM Context Control
ShortName:	OAM_CONTEXT_CONTROL_MEDIA_SLICE_0_OA
Address:	133BCh-133BFh
Name:	OAM Context Control
ShortName:	OAM_CONTEXT_CONTROL_MEDIA_SLICE_1_OA
Address:	135BCh-135BFh
Name:	OAM Context Control
ShortName:	OAM_CONTEXT_CONTROL_MEDIA_SLICE_2_OA
Address:	137BCh-137BFh
Name:	OAM Context Control
ShortName:	OAM_CONTEXT_CONTROL_MEDIA_SLICE_3_OA

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: PBC _Custom_GTIReset: DEV
	7:2	**Timer Period** Default Value: 00b Access: R/W Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: StrobePeriod = MinimumTimeStampPeriod * 2 **(TimerPeriod + 1)** The exponent is defined by this field. **Programming Notes** **Note:** The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.

OAM_OACTXCTRL - OAM Context Control

1 **Timer Enable**

Access:	R/W

This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.

Value	Name	Description
0	Disable **[Default]**	Counter does not get written out on regular interval
1	Enable	Counter gets written out on regular intervals, defined by the Timer Period

Programming Notes
When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts.

0 **Counter Stop-Resume Mechanism**

Access:	R/W

Counter stop-resume mechanism

Value	Name	Description
1	Resume	Resume counting for all counters

OAM GPU Ticks Counter

OAM_GPU_TICKS - OAM GPU Ticks Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	130E0h-130E3h
Name:	GPU Ticks Counter
ShortName:	GPU_TICKS_COUNTER_MEDIA_SLICE_0_OA
Address:	132E0h-132E3h
Name:	GPU Ticks Counter
ShortName:	GPU_TICKS_COUNTER_MEDIA_SLICE_1_OA
Address:	134E0h-134E3h
Name:	GPU Ticks Counter
ShortName:	GPU_TICKS_COUNTER_MEDIA_SLICE_2_OA
Address:	136E0h-136E3h
Name:	GPU Ticks Counter
ShortName:	GPU_TICKS_COUNTER_MEDIA_SLICE_3_OA

Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM GPU Ticks Counter Upper DWord

OAM_GPU_TICKS_UPPER - OAM GPU Ticks Counter Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	130E4h-130E7h
Name:	GPU Ticks Counter Upper DWord
ShortName:	GPU_TICKS_COUNTER_UPPER_MEDIA_SLICE_0_OA

Address:	132E4h-132E7h
Name:	GPU Ticks Counter Upper DWord
ShortName:	GPU_TICKS_COUNTER_UPPER_MEDIA_SLICE_1_OA

Address:	134E4h-134E7h
Name:	GPU Ticks Counter Upper DWord
ShortName:	GPU_TICKS_COUNTER_UPPER_MEDIA_SLICE_2_OA

Address:	136E4h-136E7h
Name:	GPU Ticks Counter Upper DWord
ShortName:	GPU_TICKS_COUNTER_UPPER_MEDIA_SLICE_3_OA

Reading this register returns the live value of the Upper DWord of GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAM Interrupt Mask Register

OAM_OA_IMR - OAM Interrupt Mask Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	131B4h-131B7h
Name:	OAM Interrupt Mask
ShortName:	OAM_INTERRUPT_MASK_MEDIA_SLICE_0_OA
Address:	133B4h-133B7h
Name:	OAM Interrupt Mask
ShortName:	OAM_INTERRUPT_MASK_MEDIA_SLICE_1_OA
Address:	135B4h-135B7h
Name:	OAM Interrupt Mask
ShortName:	OAM_INTERRUPT_MASK_MEDIA_SLICE_2_OA
Address:	137B4h-137B7h
Name:	OAM Interrupt Mask
ShortName:	OAM_INTERRUPT_MASK_MEDIA_SLICE_3_OA

The OAIMR register is used by software to control whether OA generates an interrupt or not.

DWord	Bit	Description
0	31:29	**Reserved** Default Value: 7h Access: R/W Format: PBC _Custom_GTIReset: DEV
	28	**Mask Bit** Access: R/W _Custom_GTIReset: DEV 0h – Not Masked – May generate an interrupt 1h – Masked **[Default]** – Will not generate an interrupt
	27:0	**Reserved** Default Value: FFFFFFFh Access: R/W Format: PBC _Custom_GTIReset: DEV

OAM MMIO Trigger

OAM_MMIO_TRG - OAM MMIO Trigger	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	131D0h-131D3h
Name:	OAM MMIO Trigger
ShortName:	OAM_MMIO_TRG_MEDIA_SLICE_0_OA
Address:	133D0h-133D3h
Name:	OAM MMIO Trigger
ShortName:	OAM_MMIO_TRG_MEDIA_SLICE_1_OA
Address:	135D0h-135D3h
Name:	OAM MMIO Trigger
ShortName:	OAM_MMIO_TRG_MEDIA_SLICE_2_OA
Address:	137D0h-137D3h
Name:	OAM MMIO Trigger
ShortName:	OAM_MMIO_TRG_MEDIA_SLICE_3_OA

Writing in this register triggers a report in OAM. The reports are stored in the OA Buffer space.

DWord	Bit	Description
0	31:0	**Unique ID** Access: R/W Format: U32 _Custom_GTIReset: DEV This field is inserted as such into the Context ID field of the report generated due to the write to this register. Report gets triggered irrespective of the value written into this register. By uniquely maintaining this value for every trigger, user can uniquely identify various reports.

OAM Observation Architecture Buffer

OAM_OABUFFER - OAM Observation Architecture Buffer

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	131A8h-131ABh
Name:	OAM Buffer
ShortName:	OAM_BUFFER_MEDIA_SLICE_0_OA
Address:	133A8h-133ABh
Name:	OAM Buffer
ShortName:	OAM_BUFFER_MEDIA_SLICE_1_OA
Address:	135A8h-135ABh
Name:	OAM Buffer
ShortName:	OAM_BUFFER_MEDIA_SLICE_2_OA
Address:	137A8h-137ABh
Name:	OAM Buffer
ShortName:	OAM_BUFFER_MEDIA_SLICE_3_OA

This register is used to program the OA unit.

Programming Notes

This MMIO must be set before the OATAILPTR register and set after the OAHEADPTR register. This is to enable proper functionality of the overflow bit.

DWord	Bit	Description
0	31:6	**Report Buffer Offset** Access: R/W _Custom_GTIReset: DEV This field specifies 64B aligned GFX MEM address where the chap counter values are reported.
	5:3	**Inter Trigger Report Buffer Size** Access: R/W _Custom_GTIReset: DEV **Description** This field indicates the size of report buffer for time/event-based report trigger mechanisms. This field is programmed in terms of multiple of 128KB. Value / Name / Description 0h / 128 KB or 1MB **[Default]** / All context considered.

1h	256 KB or 2MB	
2h	512 KB or 4MB	
3h	1 MB or 8MB	
4h	2 MB or 16MB	
5h	4 MB or 32MB	
6h	8 MB or 64MB	
7h	16 MB or 128MB	

2 **OA Report Trigger Select**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
0		Level Report trigger
1		Edge Report trigger

1 **Disable Overrun Mode**

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

This field defines the mode of reporting for internal trigger/timer based reporting. When this bit is set, overrun does not lose reports but stops reporting. Based on the head and tail pointer, when HW detects room for the report, it would resume reporting to the buffer. This mode would not set the over-run bit in the register. When this mode bit is reset, buffer overrun can happen and lose the reports while setting the buffer over-run bit.

Value	Name	Description
0h	Disable **[Default]**	Counter gets written out on regular intervals, defined by the Timer Period
1h	Enable	Counter does not get written out on regular interval

0 **Memory Select PPGTT/GGTT Access**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0h	PPGTT
1h	GGTT **[Default]**

Programming Notes
When each context has its own Per Process GTT, this field should be always set to GGTT.

OAM Observation Architecture Control

OAM_OACONTROL - OAM Observation Architecture Control

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13194h-13197h
Name:	OAM Control
ShortName:	OAM_CONTROL_MEDIA_SLICE_0_OA
Address:	13394h-13397h
Name:	OAM Control
ShortName:	OAM_CONTROL_MEDIA_SLICE_1_OA
Address:	13594h-13597h
Name:	OAM Control
ShortName:	OAM_CONTROL_MEDIA_SLICE_2_OA
Address:	13794h-13797h
Name:	OAM Control
ShortName:	OAM_CONTROL_MEDIA_SLICE_3_OA

This register controls OAM functionality, report format, and context filtering. If OAM is enabled then it should be enabled in CS as well

DWord	Bit	Description
0	31:4	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	3:1	**Counter Select** Access: R/W _Custom_GTIReset: DEV This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.

OAM_OACONTROL - OAM Observation Architecture Control

	0	**Performance Counter Enable** Access: R/W Format: Enable _Custom_GTIReset: DEV Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear. **Programming Notes** "OAM Context Enable" mode bit in CTX_SR_CTL register must be set when "Programmer Counter Enable" is set. VDBOX0 fuse of respective media slice should be enabled for corresponding OAM functionality to be available.

OAM Observation Architecture Head Pointer

OAM_OAHEADPTR - OAM Observation Architecture Head Pointer

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	131A0h-131A3h
Name:	OAM Head Pointer
ShortName:	OAM_HEAD_POINTER_MEDIA_SLICE_0_OA
Address:	133A0h-133A3h
Name:	OAM Head Pointer
ShortName:	OAM_HEAD_POINTER_MEDIA_SLICE_1_OA
Address:	135A0h-135A3h
Name:	OAM Head Pointer
ShortName:	OAM_HEAD_POINTER_MEDIA_SLICE_2_OA
Address:	137A0h-137A3h
Name:	OAM Head Pointer
ShortName:	OAM_HEAD_POINTER_MEDIA_SLICE_3_OA

This register allows SW to program head pointer.

DWord	Bit	Description
0	31:6	**Head Pointer** Access: R/W _Custom_GTIReset: DEV Virtual address of the internal trigger based buffer that is updated by software after consuming reports from the report buffer. This pointer must be updated by SW only when using time or event-based report triggering. **Programming Notes** SW must ensure that Head Pointer and the Tail Pointer match before enabling internally triggered performance counter reporting.
	5:0	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OAM Observation Architecture Report Trigger 2

OAM_OAREPORTTRIG2 - OAM Observation Architecture Report Trigger 2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	13024h-13027h
Name:	Report Trigger 2
ShortName:	REPORT_TRIGGER_2_MEDIA_SLICE_0_OA

Address:	13224h-13227h
Name:	Report Trigger 2
ShortName:	REPORT_TRIGGER_2_MEDIA_SLICE_1_OA

Address:	13424h-13427h
Name:	Report Trigger 2
ShortName:	REPORT_TRIGGER_2_MEDIA_SLICE_2_OA

Address:	13624h-13627h
Name:	Report Trigger 2
ShortName:	REPORT_TRIGGER_2_MEDIA_SLICE_3_OA

This register controls some of the Boolean logic defining Boolean/threshold report trigger 0. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are OR'd to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	**Report Trigger Enable** Access: R/W Format: Enable _Custom_GTIReset: DEV Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.

OAM_OAREPORTTRIG2 - OAM Observation Architecture Report Trigger 2

	When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.
30:24	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
23	**Threshold Enable** Access: R/W Format: Enable _Custom_GTIReset: DEV Enable the threshold compare logic within the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
22	**Invert D Enable 0** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the D stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
21	**Invert C Enable 1** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
20	**Invert C Enable 0** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the C stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
19	**Invert B Enable 3** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAM_OAREPORTTRIG2 - OAM Observation Architecture Report Trigger 2

	18	**Invert B Enable 2** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	17	**Invert B Enable 1** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	14	**Invert A Enable 14** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAM_OAREPORTTRIG2 - OAM Observation Architecture Report Trigger 2

12	**Invert A Enable 12** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
11	**Invert A Enable 11** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
10	**Invert A Enable 10** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
9	**Invert A Enable 9** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
8	**Invert A Enable 8** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
7	**Invert A Enable 7** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAM_OAREPORTTRIG2 - OAM Observation Architecture Report Trigger 2

	6	**Invert A Enable 6** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	3	**Invert A Enable 3** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	2	**Invert A Enable 2** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAM_OAREPORTTRIG2 - OAM Observation Architecture Report Trigger 2

	0	**Invert A Enable 0** Access: R/W Format: Enable _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 0 logic (see block diagram in the Performance Counter Reporting section).

OAM Observation Architecture Report Trigger 6

OAM_OAREPORTTRIG6 - OAM Observation Architecture Report Trigger 6

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	13034h-13037h
Name:	Report Trigger 6
ShortName:	REPORT_TRIGGER_6_MEDIA_SLICE_0_OA

Address:	13234h-13237h
Name:	Report Trigger 6
ShortName:	REPORT_TRIGGER_6_MEDIA_SLICE_1_OA

Address:	13434h-13437h
Name:	Report Trigger 6
ShortName:	REPORT_TRIGGER_6_MEDIA_SLICE_2_OA

Address:	13634h-13637h
Name:	Report Trigger 6
ShortName:	REPORT_TRIGGER_6_MEDIA_SLICE_3_OA

This register controls some of the Boolean logic defining Boolean/threshold report trigger 1. Note that Boolean report triggers 0 and 1 are logically OR'd together without buffering, this implies that only one performance counter report will be generated for clocks where both Boolean report triggers evaluate true. The bit definitions in this register refer to the stages in the report trigger block diagram in the Performance Counter Reporting section.

Report triggers generated from OAREPORTTRIG 1-4 and OAREPORTTRIG 5-8 are OR'd to form a new report trigger. Report trigger behavior can be derived by programming these two sets of OA REPORT registers with the same value. Users should be aware that while programming Timer based and Threshold Counter based triggers simultaneously for internal reporting, they should be programmed such way that they are not consecutively triggered. If programmed simultaneously, RTL pulse detection logic will have problem when these triggers occur in consecutive clock cycles.

DWord	Bit	Description
0	31	**Report Trigger Enable** Access: R/W _Custom_GTIReset: DEV Enable Boolean/threshold report trigger 0. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.

OAM_OAREPORTTRIG6 - OAM Observation Architecture Report Trigger 6

	When "Specific Context Enable" bit set to '1' in OACONTROL register, Boolean/Threshold report trigger function gets enabled only for the selected context.When "Specific Context Enable" bit set to '0' in OACONTROL register, Boolean/Threshold report trigger function gets enabled for all contexts.
30:24	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
23	**Threshold Enable** Access: R/W _Custom_GTIReset: DEV Enable the threshold compare logic within the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
22	**Invert D Enable 0** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the D stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
21	**Invert C Enable 1** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
20	**Invert C Enable 0** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the C stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
19	**Invert B Enable 3** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
18	**Invert B Enable 2** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAM_OAREPORTTRIG6 - OAM Observation Architecture Report Trigger 6

	17	**Invert B Enable 1** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	16	**Invert B Enable 0** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the B stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	15	**Invert A Enable 15** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	14	**Invert A Enable 14** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	13	**Invert A Enable 13** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	12	**Invert A Enable 12** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	11	**Invert A Enable 11** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAM_OAREPORTTRIG6 - OAM Observation Architecture Report Trigger 6

	10	**Invert A Enable 10** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	9	**Invert A Enable 9** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	8	**Invert A Enable 8** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	7	**Invert A Enable 7** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	6	**Invert A Enable 6** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	5	**Invert A Enable 5** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	4	**Invert A Enable 4** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAM_OAREPORTTRIG6 - OAM Observation Architecture Report Trigger 6

	3	**Invert A Enable 3** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	2	**Invert A Enable 2** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	1	**Invert A Enable 1** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).
	0	**Invert A Enable 0** Access: R/W _Custom_GTIReset: DEV Invert the specified signal at the A stage of the Boolean/threshold report trigger 1 logic (see block diagram in the Performance Counter Reporting section).

OAM Observation Architecture Report Trigger Counter

OAM_OARPTTRIG_COUNTER - OAM Observation Architecture Report Trigger Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	131B0h-131B3h
Name:	Report Trigger Counter
ShortName:	REPORT_TRIGGER_COUNTER_MEDIA_SLICE_0_OA
Address:	133B0h-133B3h
Name:	Report Trigger Counter
ShortName:	REPORT_TRIGGER_COUNTER_MEDIA_SLICE_1_OA
Address:	135B0h-135B3h
Name:	Report Trigger Counter
ShortName:	REPORT_TRIGGER_COUNTER_MEDIA_SLICE_2_OA
Address:	137B0h-137B3h
Name:	Report Trigger Counter
ShortName:	REPORT_TRIGGER_COUNTER_MEDIA_SLICE_3_OA

This register provides status of report trigger threshold count 1 and 2. This register is for HW internal purpose and power context save/restored. This register must not be programmed by SW.

DWord	Bit	Description
0	31:16	**Report Trig Threshold Count 1 Status** Access: R/W _Custom_GTIReset: DEV **Programming Notes** This field is for HW internal use to context save/restore rpt trigger threshold count 1. It always indicates current value of HW's internal report trigger count. SW should not program these bits.
	15:0	**Report Trig Threshold count 2 status** Access: R/W _Custom_GTIReset: DEV **Programming Notes** This field is for HW internal use to context save/restore rpt trigger threshold count 2. It always indicates current value of HW's internal report trigger count. SW should not program these bits.

OAM Observation Architecture Start Trigger 5

OAM_OASTARTTRIG5 - OAM Observation Architecture Start Trigger 5

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	13010h-13013h
Name:	Start Trigger 5
ShortName:	START_TRIGGER_5_MEDIA_SLICE_0_OA

Address:	13210h-13213h
Name:	Start Trigger 5
ShortName:	START_TRIGGER_5_MEDIA_SLICE_1_OA

Address:	13410h-13413h
Name:	Start Trigger 5
ShortName:	START_TRIGGER_5_MEDIA_SLICE_2_OA

Address:	13610h-13613h
Name:	Start Trigger 5
ShortName:	START_TRIGGER_5_MEDIA_SLICE_3_OA

This register provides the threshold value optionally used to define the start trigger for B7-B4 counters. Note that the value in this register must match the value in OASTARTTRIG1 to have B7-B0 start at the same time. The bit definition in this register refers to the stages in the start trigger block diagram in the Performance Counter Reporting section.

DWord	Bit	Description
0	31:16	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	15:0	**Threshold Value** Access: R/W Format: U16 _Custom_GTIReset: DEV **Programming Notes** Threshold value for the compare logic within the start trigger logic for B7-B4 counters.

OAM Observation Architecture Start Trigger Counter

OAM_OASTARTTRIG_COUNTER - OAM Observation Architecture Start Trigger Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	131ACh-131AFh
Name:	Start Trigger Counter
ShortName:	START_TRIGGER_COUNTER_MEDIA_SLICE_0_OA
Address:	133ACh-133AFh
Name:	Start Trigger Counter
ShortName:	START_TRIGGER_COUNTER_MEDIA_SLICE_1_OA
Address:	135ACh-135AFh
Name:	Start Trigger Counter
ShortName:	START_TRIGGER_COUNTER_MEDIA_SLICE_2_OA
Address:	137ACh-137AFh
Name:	Start Trigger Counter
ShortName:	START_TRIGGER_COUNTER_MEDIA_SLICE_3_OA

This register provides status of start trigger threshold count 1 and 2. This register is for HW internal purpose.

DWord	Bit	Description
0	31:16	**Start Trig Threshold Count 1 Status** Access: R/W _Custom_GTIReset: DEV **Programming Notes** This field is for HW internal use to context save/restore start trigger threshold count 1. It always indicates current value of HW's internal start trigger count. SW should not program these bits.
	15:0	**Start Trig Threshold count 2 status** Access: R/W _Custom_GTIReset: DEV **Programming Notes** : This field is for HW internal use to context save/restore start trigger threshold count 2. It always indicates current value of HW's internal start trigger count. SW should not program these bits.

OAM Observation Architecture Status Register

OAM_OASTATUS - OAM Observation Architecture Status Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1319Ch-1319Fh
Name:	OAM Status
ShortName:	OAM_STATUS_MEDIA_SLICE_0_OA
Address:	1339Ch-1339Fh
Name:	OAM Status
ShortName:	OAM_STATUS_MEDIA_SLICE_1_OA
Address:	1359Ch-1359Fh
Name:	OAM Status
ShortName:	OAM_STATUS_MEDIA_SLICE_2_OA
Address:	1379Ch-1379Fh
Name:	OAM Status
ShortName:	OAM_STATUS_MEDIA_SLICE_3_OA

This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits. Status bits are active high flags (0=false, 1=true)

DWord	Bit	Description
0	31:22	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	21	**Start Trigger Flag 1** Access: R/W _Custom_GTIReset: DEV Value / Name: 0 **[Default]** 1 **Programming Notes** This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.

OAM_OASTATUS - OAM Observation Architecture Status Register

20 **Start Trigger Flag 2**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0	**[Default]**
1	

Programming Notes
This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.

19 **Report Trigger Flag 1**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0	**[Default]**
1	

Programming Notes
This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.

18 **Report Trigger Flag 2**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0	**[Default]**
1	

Programming Notes
This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.

OAM_OASTATUS - OAM Observation Architecture Status Register

17 **Tail Pointer Wrap Flag**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Value	Name
0	
1	**[Default]**

Programming Notes
This bit is for HW internal use to context save /restore Tail Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Tail Pointer Wrap Mask bit is set.

16 **Head Pointer Wrap Flag**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Value	Name
0	
1	**[Default]**

Programming Notes
This bit is for HW internal use to context save /restore Head Pointer Wrap Flag. SW should not program this bit. This bit gets programmed only when Head Pointer Wrap Mask bit is set.

15:7 **Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

6 **MMIO Trigger Queue Full**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

This bit is set if MMIO Trigger FIFO in HW becomes full. This bit can be reset by SW by either soft reset or writing a 0to it.

Value	Name	Description
0h	**[Default]**	MMIO Trigger Queue is not full
1h		MMIO Trigger Queue is full

5 **Reserved**

OAM_OASTATUS - OAM Observation Architecture Status Register

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

4 **Accumulator Overflow**

Access:	R/W
_Custom_GTIReset:	DEV

This field indicates that the one or more event accumulator inside the slice-OAunit has overflowed. Once set, this bit will remain set, until SW resets it by either soft reset or writing a 0 to it.

Value	Name	Description
0	**[Default]**	No overflow has occurred.
1		Overflow has occurred.

3 **Overrun Status**

Access:	R/W
_Custom_GTIReset:	DEV

This field indicates the status of overrun. This bit is read only and writing to this bit will have no effect. This bit will reflect the status of overrun irrespective of Overun Mode enabled or disabled.

Value	Name	Description
0	**[Default]**	No overrun has occurred
1		Overrun has occurred

2 **Counter Overflow**

Access:	R/W
_Custom_GTIReset:	DEV

This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 0 to it.

Value	Name	Description
0	**[Default]**	Counter Overflow Not Occurred
1		Counter Overflow Occurred

1 **Buffer Overflow**

Access:	R/W
_Custom_GTIReset:	DEV

This bit is set when the Tail-pointer - Head pointer > max internal trigger buffer size

Value	Name	Description
0h	**[Default]**	Buffer Overflow Not Occurred
1		Buffer Overflow Occurred

OAM_OASTATUS - OAM Observation Architecture Status Register

0 **Report Lost Error**

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

This bit is set if the Report Trigger due to "Internal Report Trigger-1", "Internal Report Trigger-2" or "Timer Triggered" or "MMIO Trigger" to write out the counter values is dropped, while there is an ongoing report in progress. The report request is ignored and the counter continue to count. This bit will be set along with this MMIO Trigger Queue Full, in case of dropped request for MMIO trigger.

Value	Name	Description
0	**[Default]**	Report Lost Error Not Occurred
1		Report Lost Error Occurred

Programming Notes
This bit can be reset by SW by either soft reset or writing a 0 to it.

OAM Observation Architecture Tail Pointer

OAM_OATAILPTR - OAM Observation Architecture Tail Pointer

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	131A4h-131A7h
Name:	OAM Tail Pointer
ShortName:	OAM_TAIL_POINTER_MEDIA_SLICE_0_OA
Address:	133A4h-133A7h
Name:	OAM Tail Pointer
ShortName:	OAM_TAIL_POINTER_MEDIA_SLICE_1_OA
Address:	135A4h-135A7h
Name:	OAM Tail Pointer
ShortName:	OAM_TAIL_POINTER_MEDIA_SLICE_2_OA
Address:	137A4h-137A7h
Name:	OAM Tail Pointer
ShortName:	OAM_TAIL_POINTER_MEDIA_SLICE_3_OA

This register allows software to program tail pointer and also indicates current tail pointer value.

DWord	Bit	Description
0	31:6	**Tail Pointer** Access: R/W _Custom_GTIReset: DEV Virtual address of the internal trigger based buffer that is updated for every 64B cacheline write to memory when reporting via internal report trigger. This pointer will not be updated for MI_REPORT_PERF_COUNT command based writes. **Programming Notes** Before enabling internally triggered performance counter reporting, SW must ensure that this address matches the Report Buffer Offset programmed in OABUFFER register (i.e. tail pointer must start at the beginning of the report buffer). SW must ensure that Tail pointer and the Head Pointer match before enabling internally triggered performance counter reporting.
	5:0	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OAM Slice Customizable Event Creation 0-0

OAM_SCEC00 - OAM Slice Customizable Event Creation 0-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13040h-13043h
Name:	Customizable Event Creation 0-0
ShortName:	CEC_00_MEDIA_SLICE_0_OA
Address:	13240h-13243h
Name:	Customizable Event Creation 0-0
ShortName:	CEC_00_MEDIA_SLICE_1_OA
Address:	13440h-13443h
Name:	Customizable Event Creation 0-0
ShortName:	CEC_00_MEDIA_SLICE_2_OA
Address:	13640h-13643h
Name:	Customizable Event Creation 0-0
ShortName:	CEC_00_MEDIA_SLICE_3_OA

This register is used to define the slice custom counter event 0, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator

OAM_SCEC00 - OAM Slice Customizable Event Creation 0-0

20:19 **Source Select**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block
11b	Reserved	

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC0 comparator when comparing the compare value to the value active on the CEC0 conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAM Slice Customizable Event Creation 1-0

OAM_SCEC10 - OAM Slice Customizable Event Creation 1-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13048h-1304Bh
Name:	Customizable Event Creation 1-0
ShortName:	CEC_10_MEDIA_SLICE_0_OA
Address:	13248h-1324Bh
Name:	Customizable Event Creation 1-0
ShortName:	CEC_10_MEDIA_SLICE_1_OA
Address:	13448h-1344Bh
Name:	Customizable Event Creation 1-0
ShortName:	CEC_10_MEDIA_SLICE_2_OA
Address:	13648h-1364Bh
Name:	Customizable Event Creation 1-0
ShortName:	CEC_10_MEDIA_SLICE_3_OA

This register is used to define slice custom counter event 1, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.

Value	Name	Description
0b	Pass-through	Input bit is passed through to comparator as is
1b	Negated	Input bit is negated before passing to comparator

OAM_SCEC10 - OAM Slice Customizable Event Creation 1-0

20:19 **Source Select**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAM Slice Customizable Event Creation 1-1

OAM_SCEC11 - OAM Slice Customizable Event Creation 1-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1304Ch-1304Fh
Name:	Customizable Event Creation 1-1
ShortName:	CEC_11_MEDIA_SLICE_0_OA
Address:	1324Ch-1324Fh
Name:	Customizable Event Creation 1-1
ShortName:	CEC_11_MEDIA_SLICE_1_OA
Address:	1344Ch-1344Fh
Name:	Customizable Event Creation 1-1
ShortName:	CEC_11_MEDIA_SLICE_2_OA
Address:	1364Ch-1364Fh
Name:	Customizable Event Creation 1-1
ShortName:	CEC_11_MEDIA_SLICE_3_OA

This register configures the input conditioning portion of slice CEC (custom event creation) block 1, bit definitions in this register refer to the CEC block diagram.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAM Slice Customizable Event Creation 2-0

OAM_SCEC20 - OAM Slice Customizable Event Creation 2-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13050h-13053h
Name:	Customizable Event Creation 2-0
ShortName:	CEC_20_MEDIA_SLICE_0_OA
Address:	13250h-13253h
Name:	Customizable Event Creation 2-0
ShortName:	CEC_20_MEDIA_SLICE_1_OA
Address:	13450h-13453h
Name:	Customizable Event Creation 2-0
ShortName:	CEC_20_MEDIA_SLICE_2_OA
Address:	13650h-13653h
Name:	Customizable Event Creation 2-0
ShortName:	CEC_20_MEDIA_SLICE_3_OA

This register is used to define custom counter event 2, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator

OAM_SCEC20 - OAM Slice Customizable Event Creation 2-0

20:19 **Source Select**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAM Slice Customizable Event Creation 2-1

OAM_SCEC21 - OAM Slice Customizable Event Creation 2-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13054h-13057h
Name:	Customizable Event Creation 2-1
ShortName:	CEC_21_MEDIA_SLICE_0_OA
Address:	13254h-13257h
Name:	Customizable Event Creation 2-1
ShortName:	CEC_21_MEDIA_SLICE_1_OA
Address:	13454h-13457h
Name:	Customizable Event Creation 2-1
ShortName:	CEC_21_MEDIA_SLICE_2_OA
Address:	13654h-13657h
Name:	Customizable Event Creation 2-1
ShortName:	CEC_21_MEDIA_SLICE_3_OA

This register configures the input conditioning portion of slice CEC (custom event creation) block 2, bit definitions in this register refer to the CEC block diagram.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:16</td><td>Considerations
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Live</td><td>Input bit is not delayed by 1 clock before event calculation</td></tr>
<tr><td>1b</td><td>Delayed</td><td>Input bit is delayed by 1 clock before event calculation</td></tr>
</table></td></tr>
<tr><td></td><td>15:0</td><td>Mask
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Unmasked</td><td>Input bit is considered in event calculation</td></tr>
<tr><td>1b</td><td>Masked</td><td>Input bit is ignored in event calculation</td></tr>
</table></td></tr>
</table>

OAM Slice Customizable Event Creation 3-0

OAM_SCEC30 - OAM Slice Customizable Event Creation 3-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13058h-1305Bh
Name:	Customizable Event Creation 3-0
ShortName:	CEC_30_MEDIA_SLICE_0_OA
Address:	13258h-1325Bh
Name:	Customizable Event Creation 3-0
ShortName:	CEC_30_MEDIA_SLICE_1_OA
Address:	13458h-1345Bh
Name:	Customizable Event Creation 3-0
ShortName:	CEC_30_MEDIA_SLICE_2_OA
Address:	13658h-1365Bh
Name:	Customizable Event Creation 3-0
ShortName:	CEC_30_MEDIA_SLICE_3_OA

This register is used to define slice custom counter event 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator

OAM_SCEC30 - OAM Slice Customizable Event Creation 3-0

20:19 **Source Select**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAM Slice Customizable Event Creation 3-1

OAM_SCEC31 - OAM Slice Customizable Event Creation 3-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1305Ch-1305Fh
Name:	Customizable Event Creation 3-1
ShortName:	CEC_31_MEDIA_SLICE_0_OA
Address:	1325Ch-1325Fh
Name:	Customizable Event Creation 3-1
ShortName:	CEC_31_MEDIA_SLICE_1_OA
Address:	1345Ch-1345Fh
Name:	Customizable Event Creation 3-1
ShortName:	CEC_31_MEDIA_SLICE_2_OA
Address:	1365Ch-1365Fh
Name:	Customizable Event Creation 3-1
ShortName:	CEC_31_MEDIA_SLICE_3_OA

This register configures the input conditioning portion of Slice CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. **Value** / **Name** / **Description** 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. **Value** / **Name** / **Description** 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OAM Slice Customizable Event Creation 4-0

OAM_SCEC40 - OAM Slice Customizable Event Creation 4-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13060h-13063h
Name:	Customizable Event Creation 4-0
ShortName:	CEC_40_MEDIA_SLICE_0_OA
Address:	13260h-13263h
Name:	Customizable Event Creation 4-0
ShortName:	CEC_40_MEDIA_SLICE_1_OA
Address:	13460h-13463h
Name:	Customizable Event Creation 4-0
ShortName:	CEC_40_MEDIA_SLICE_2_OA
Address:	13660h-13663h
Name:	Customizable Event Creation 4-0
ShortName:	CEC_40_MEDIA_SLICE_3_OA

This register is used to define slice custom counter event 4, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator

OAM_SCEC40 - OAM Slice Customizable Event Creation 4-0

20:19 **Source Select**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the last CEC block as the input bus to CEC0 block
11b	Reserved	

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAM Slice Customizable Event Creation 5-0

OAM_SCEC50 - OAM Slice Customizable Event Creation 5-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13068h-1306Bh
Name:	Customizable Event Creation 5-0
ShortName:	CEC_50_MEDIA_SLICE_0_OA
Address:	13268h-1326Bh
Name:	Customizable Event Creation 5-0
ShortName:	CEC_50_MEDIA_SLICE_1_OA
Address:	13468h-1346Bh
Name:	Customizable Event Creation 5-0
ShortName:	CEC_50_MEDIA_SLICE_2_OA
Address:	13668h-1366Bh
Name:	Customizable Event Creation 5-0
ShortName:	CEC_50_MEDIA_SLICE_3_OA

This register is used to define slice custom counter event 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator

OAM_SCEC50 - OAM Slice Customizable Event Creation 5-0

20:19 **Source Select**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAM Slice Customizable Event Creation 5-1

OAM_SCEC51 - OAM Slice Customizable Event Creation 5-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1306Ch-1306Fh
Name:	Customizable Event Creation 5-1
ShortName:	CEC_51_MEDIA_SLICE_0_OA
Address:	1326Ch-1326Fh
Name:	Customizable Event Creation 5-1
ShortName:	CEC_51_MEDIA_SLICE_1_OA
Address:	1346Ch-1346Fh
Name:	Customizable Event Creation 5-1
ShortName:	CEC_51_MEDIA_SLICE_2_OA

This register configures the input conditioning portion of CEC (custom event creation) block 5, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. 0b – Live – Input bit is not delayed by 1 clock before event calculation 1b – Delayed – Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. 0b – Unmasked – Input bit is considered in event calculation 1b – Masked – Input bit is ignored in event calculation

OAM Slice Customizable Event Creation 6-0

OAM_SCEC60 - OAM Slice Customizable Event Creation 6-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13070h-13073h
Name:	Customizable Event Creation 6-0
ShortName:	CEC_60_MEDIA_SLICE_0_OA
Address:	13270h-13273h
Name:	Customizable Event Creation 6-0
ShortName:	CEC_60_MEDIA_SLICE_1_OA
Address:	13470h-13473h
Name:	Customizable Event Creation 6-0
ShortName:	CEC_60_MEDIA_SLICE_2_OA
Address:	13670h-13673h
Name:	Customizable Event Creation 6-0
ShortName:	CEC_60_MEDIA_SLICE_3_OA

This register is used to define slice custom counter event 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:21	**Negate** Access: R/W Format: U11 _Custom_GTIReset: DEV The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus. 0b – Pass-through – Input bit is passed through to comparator as is 1b – Negated – Input bit is negated before passing to comparator

OAM_SCEC60 - OAM Slice Customizable Event Creation 6-0

20:19 **Source Select**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator (see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAM Slice Customizable Event Creation 6-1

OAM_SCEC61 - OAM Slice Customizable Event Creation 6-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13074h-13077h
Name:	Customizable Event Creation 6-1
ShortName:	CEC_61_MEDIA_SLICE_0_OA
Address:	13274h-13277h
Name:	Customizable Event Creation 6-1
ShortName:	CEC_61_MEDIA_SLICE_1_OA
Address:	13474h-13477h
Name:	Customizable Event Creation 6-1
ShortName:	CEC_61_MEDIA_SLICE_2_OA
Address:	13674h-13677h
Name:	Customizable Event Creation 6-1
ShortName:	CEC_61_MEDIA_SLICE_3_OA

This register configures the input conditioning portion of slice CEC (custom event creation) block 6, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. **Value** / **Name** / **Description** 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. **Value** / **Name** / **Description** 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OAM Slice Customizable Event Creation 7-0

OAM_SCEC70 - OAM Slice Customizable Event Creation 7-0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	13078h-1307Bh
Name:	Customizable Event Creation 7-0
ShortName:	CEC_70_MEDIA_SLICE_0_OA
Address:	13278h-1327Bh
Name:	Customizable Event Creation 7-0
ShortName:	CEC_70_MEDIA_SLICE_1_OA
Address:	13478h-1347Bh
Name:	Customizable Event Creation 7-0
ShortName:	CEC_70_MEDIA_SLICE_2_OA
Address:	13678h-1367Bh
Name:	Customizable Event Creation 7-0
ShortName:	CEC_70_MEDIA_SLICE_3_OA

This register is used to define slice custom counter event 7, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:21</td><td>Negate
<table>
<tr><td>Access:</td><td>R/W</td></tr>
<tr><td>Format:</td><td>U11</td></tr>
<tr><td>_Custom_GTIReset:</td><td>DEV</td></tr>
</table>
The 11-bit array defined in this field allows input bus bits [10:0] to be individually negated in order to facilitate more complicated custom event creation (e.g. A & (!B | !C)). Note that LSB of this field affects bit 0 of the selected input bus.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th></tr>
<tr><td>0b</td><td>Pass-through</td><td>Input bit is passed through to comparator as is</td></tr>
<tr><td>1b</td><td>Negated</td><td>Input bit is negated before passing to comparator</td></tr>
</table>
</td></tr>
</table>

OAM_SCEC70 - OAM Slice Customizable Event Creation 7-0

20:19 **Source Select**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the input signals to the Boolean event definition logic (see block diagram in the Custom Event Counters section).

Value	Name	Description
01b	Prev Event	Selects the conditioned/flopped input from the previous CEC block as the input bus to this CEC block
11b	Reserved	

18:3 **Compare Value**

Access:	R/W
Format:	U16
_Custom_GTIReset:	DEV

The value in this field is compared the 16-bit conditioned input bus that are fed into the comparator(see block diagram in the Custom Event Counters section). The type of comparison that is done is controlled by the Compare Function. When the compare function is true, then the signal for the custom event is asserted. This signal in turn can be counted by the B0 performance counter or fed into other CEC blocks.

2:0 **Compare Function**

Access:	R/W
Format:	U3
_Custom_GTIReset:	DEV

This field selects the function used by the CEC comparator when comparing the compare value to the value active on the CEC conditioned input bus (see block diagram in the Custom Event Counters section).

Value	Name	Description
000b	Any Are Equal	Compare and assert output if any are equal (Can be used as OR function)
001b	Greater Than	Compare and assert output if greater than
010b	Equal	Compare and assert output if equal to (Can also be used as AND function)
011b	Greater Than or Equal	Compare and assert output if greater than or equal
100b	Less Than	Compare and assert output if less than
101b	Not Equal	Compare and assert output if not equal
110b	Less Than or Equal	Compare and assert output if less than or equal
111b	Reserved	

OAM Slice Customizable Event Creation 7-1

OAM_SCEC71 - OAM Slice Customizable Event Creation 7-1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1307Ch-1307Fh
Name:	Customizable Event Creation 7-1
ShortName:	CEC_71_MEDIA_SLICE_0_OA
Address:	1327Ch-1327Fh
Name:	Customizable Event Creation 7-1
ShortName:	CEC_71_MEDIA_SLICE_1_OA
Address:	1347Ch-1347Fh
Name:	Customizable Event Creation 7-1
ShortName:	CEC_71_MEDIA_SLICE_2_OA
Address:	1367Ch-1367Fh
Name:	Customizable Event Creation 7-1
ShortName:	CEC_71_MEDIA_SLICE_3_OA

This register configures the input conditioning portion of slice CEC (custom event creation) block 3, bit definitions in this register refer to the CEC block diagram in the Custom Event Counters section.

DWord	Bit	Description
0	31:16	**Considerations** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual bits of the bus selected as the input to CEC block to be delayed by 1 clock relative to the non-delayed bits in the bus (see block diagram in the Custom Event Counters section). See CEC0-1 register definition for an example use case. **Value** / **Name** / **Description** 0b / Live / Input bit is not delayed by 1 clock before event calculation 1b / Delayed / Input bit is delayed by 1 clock before event calculation
	15:0	**Mask** Access: R/W _Custom_GTIReset: DEV This 16-bit field allows individual input bits to be ignored in custom event calculation. See block diagram in the Custom Event Counters section for more details on where this field is used. **Value** / **Name** / **Description** 0b / Unmasked / Input bit is considered in event calculation 1b / Masked / Input bit is ignored in event calculation

OA Programmable Event Source Select Register

OAG_OA_PESS - OA Programmable Event Source Select Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02B2Ch

The OA_PESS register is used by software to control programmable event P15 to P0 source selection generated from 'unslice' or 'aggregated P events generated from slice'. Bit[0] indicates selection for P0, bit[1] for P1 and so on.

DWord	Bit	Description
0	31:16	**Reserved** Default Value: 0000h Access: R/W Format: PBC _Custom_GTIReset: DEV
	15:0	**P event source select** Access: R/W _Custom_GTIReset: DEV Value / Name / Description: 0h — P event generated from unslice **[Default]** — Bit wise select for P[15:0] events generated from boolean logic present in unslice 1h — P event generated from slice — Bit wise select for P[15:0] events generated from boolean logic present in slice in an aggregated manner

OAR Aggregate Perf Counter A0

OAR_OAPERF_A0 - OAR Aggregate Perf Counter A0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02800h

This register reflects the count value of the OA Performance counter A0.
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads. Value: 0x00000000 — **[Default]** Value: [0x00000001-0xFFFFFFFF]

OAR Aggregate Perf Counter A0 Upper DWord

OAR_OAPERF_A0_UPPER - OAR Aggregate Perf Counter A0 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02804h

This register enables the current live value of performance counter A0 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A1

OAR_OAPERF_A1 - OAR Aggregate Perf Counter A1		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02808h	
This register reflects the count value of the OA Performance counter A1. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A1 Upper DWord

OAR_OAPERF_A1_UPPER - OAR Aggregate Perf Counter A1 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0280Ch

This register enables the current live value of performance counter A1 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A2

OAR_OAPERF_A2 - OAR Aggregate Perf Counter A2		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02810h	
This register reflects the count value of the OA Performance counter A2. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A2 Upper DWord

OAR_OAPERF_A2_UPPER - OAR Aggregate Perf Counter A2 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02814h

This register enables the current live value of performance counter A2 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A3

OAR_OAPERF_A3 - OAR Aggregate Perf Counter A3		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02818h	
This register reflects the count value of the OA Performance counter A3. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A3 Upper DWord

OAR_OAPERF_A3_UPPER - OAR Aggregate Perf Counter A3 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0281Ch

This register enables the current live value of performance counter A3 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A4

OAR_OAPERF_A4 - OAR Aggregate Perf Counter A4		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02820h	
This register reflects the count value of the OA Performance counter A4. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A4 Upper DWord

OAR_OAPERF_A4_UPPER - OAR Aggregate Perf Counter A4 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02824h

This register enables the current live value of performance counter A4 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A5

OAR_OAPERF_A5 - OAR Aggregate Perf Counter A5		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02828h	
This register reflects the count value of the OA Performance counter A5. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A5 Upper DWord

OAR_OAPERF_A5_UPPER - OAR Aggregate Perf Counter A5 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0282Ch

This register enables the current live value of performance counter A5 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A6

OAR_OAPERF_A6 - OAR Aggregate Perf Counter A6		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02830h	
This register reflects the count value of the OA Performance counter A6. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A6 Upper DWord

OAR_OAPERF_A6_UPPER - OAR Aggregate Perf Counter A6 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02834h

This register enables the current live value of performance counter A6 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A7

OAR_OAPERF_A7 - OAR Aggregate Perf Counter A7		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02838h	
This register reflects the count value of the OA Performance counter A7. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A7 Upper DWord

OAR_OAPERF_A7_UPPER - OAR Aggregate Perf Counter A7 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0283Ch

This register enables the current live value of performance counter A7 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A8

OAR_OAPERF_A8 - OAR Aggregate Perf Counter A8		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02840h	
This register reflects the count value of the OA Performance counter A8. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A8 Upper DWord

OAR_OAPERF_A8_UPPER - OAR Aggregate Perf Counter A8 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02844h

This register enables the current live value of performance counter A8 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A9

OAR_OAPERF_A9 - OAR Aggregate Perf Counter A9		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02848h	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A9 Upper DWord

OAR_OAPERF_A9_UPPER - OAR Aggregate Perf Counter A9 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0284Ch

This register enables the current live value of performance counter A9 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A10

OAR_OAPERF_A10 - OAR Aggregate Perf Counter A10		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02850h	
This register reflects the count value of the OA Performance counter A10. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A10 Upper DWord

OAR_OAPERF_A10_UPPER - OAR Aggregate Perf Counter A10 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02854h

This register enables the current live value of performance counter A10 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A11

OAR_OAPERF_A11 - OAR Aggregate Perf Counter A11		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02858h	
This register reflects the count value of the OA Performance counter A11. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A11 Upper DWord

OAR_OAPERF_A11_UPPER - OAR Aggregate Perf Counter A11 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0285Ch

This register enables the current live value of performance counter A11 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A12

OAR_OAPERF_A12 - OAR Aggregate Perf Counter A12		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02860h	
This register reflects the count value of the OA Performance counter A12. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A12 Upper DWord

OAR_OAPERF_A12_UPPER - OAR Aggregate Perf Counter A12 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02864h

This register enables the current live value of performance counter A12 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A13

OAR_OAPERF_A13 - OAR Aggregate Perf Counter A13		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02868h	
This register reflects the count value of the OA Performance counter A13. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A13 Upper DWord

OAR_OAPERF_A13_UPPER - OAR Aggregate Perf Counter A13 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0286Ch

This register enables the current live value of performance counter A13 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A14

OAR_OAPERF_A14 - OAR Aggregate Perf Counter A14		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02870h	
This register reflects the count value of the OA Performance counter A14. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A14 Upper DWord

OAR_OAPERF_A14_UPPER - OAR Aggregate Perf Counter A14 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02874h

This register enables the current live value of performance counter A14 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A15

OAR_OAPERF_A15 - OAR Aggregate Perf Counter A15		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02878h	
This register reflects the count value of the OA Performance counter A15. DefaultValue="00000000h"		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A15 Upper DWord

OAR_OAPERF_A15_UPPER - OAR Aggregate Perf Counter A15 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0287Ch

This register enables the current live value of performance counter A15 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A16

OAR_OAPERF_A16 - OAR Aggregate Perf Counter A16		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02880h	
This register reflects the count value of the OA Performance counter A16. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A16 Upper DWord

OAR_OAPERF_A16_UPPER - OAR Aggregate Perf Counter A16 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02884h

This register enables the current live value of performance counter A16 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A17

OAR_OAPERF_A17 - OAR Aggregate Perf Counter A17		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02888h	
This register reflects the count value of the OA Performance counter A17. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A17 Upper DWord

OAR_OAPERF_A17_UPPER - OAR Aggregate Perf Counter A17 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0288Ch

This register enables the current live value of performance counter A17 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A18

OAR_OAPERF_A18 - OAR Aggregate Perf Counter A18		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02890h	
This register reflects the count value of the OA Performance counter A9. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A18 Upper DWord

OAR_OAPERF_A18_UPPER - OAR Aggregate Perf Counter A18 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02894h

This register enables the current live value of performance counter A18 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A19

OAR_OAPERF_A19 - OAR Aggregate Perf Counter A19		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02898h	
This register reflects the count value of the OA Performance counter A19. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A19 Upper DWord

OAR_OAPERF_A19_UPPER - OAR Aggregate Perf Counter A19 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0289Ch

This register enables the current live value of performance counter A19 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A20

OAR_OAPERF_A20 - OAR Aggregate Perf Counter A20		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028A0h	
This register reflects the count value of the OA Performance counter A20. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A20 Upper DWord

OAR_OAPERF_A20_UPPER - OAR Aggregate Perf Counter A20 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028A4h

This register enables the current live value of performance counter A20 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A21

OAR_OAPERF_A21 - OAR Aggregate Perf Counter A21		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028A8h	
This register reflects the count value of the OA Performance counter A21. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A21 Upper DWord

OAR_OAPERF_A21_UPPER - OAR Aggregate Perf Counter A21 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028ACh

This register enables the current live value of performance counter A21 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A22

OAR_OAPERF_A22 - OAR Aggregate Perf Counter A22		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028B0h	
This register reflects the count value of the OA Performance counter A22. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A22 Upper DWord

OAR_OAPERF_A22_UPPER - OAR Aggregate Perf Counter A22 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028B4h

This register enables the current live value of performance counter A22 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A23

OAR_OAPERF_A23 - OAR Aggregate Perf Counter A23		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028B8h	
This register reflects the count value of the OA Performance counter A23. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A23 Upper DWord

OAR_OAPERF_A23_UPPER - OAR Aggregate Perf Counter A23 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028BCh

This register enables the current live value of performance counter A23 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A24

OAR_OAPERF_A24 - OAR Aggregate Perf Counter A24		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028C0h	
This register reflects the count value of the OA Performance counter A24. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A24 Upper DWord

OAR_OAPERF_A24_UPPER - OAR Aggregate Perf Counter A24 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028C4h

This register enables the current live value of performance counter A24 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A25

OAR_OAPERF_A25 - OAR Aggregate Perf Counter A25		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028C8h	
This register reflects the count value of the OA Performance counter A25. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A25 Upper DWord

OAR_OAPERF_A25_UPPER - OAR Aggregate Perf Counter A25 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028CCh

This register enables the current live value of performance counter A25 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A26

OAR_OAPERF_A26 - OAR Aggregate Perf Counter A26		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028D0h	
This register reflects the count value of the OA Performance counter A26. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A26 Upper DWord

OAR_OAPERF_A26_UPPER - OAR Aggregate Perf Counter A26 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028D4h

This register enables the current live value of performance counter A26 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A27

OAR_OAPERF_A27 - OAR Aggregate Perf Counter A27		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028D8h	
This register reflects the count value of the OA Performance counter A27. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A27 Upper DWord

OAR_OAPERF_A27_UPPER - OAR Aggregate Perf Counter A27 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028DCh

This register enables the current live value of performance counter A27 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A28

OAR_OAPERF_A28 - OAR Aggregate Perf Counter A28		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028E0h	
This register reflects the count value of the OA Performance counter A28. Default Value="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A28 Upper DWord

OAR_OAPERF_A28_UPPER - OAR Aggregate Perf Counter A28 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028E4h

This register enables the current live value of performance counter A28 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A29

OAR_OAPERF_A29 - OAR Aggregate Perf Counter A29		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028E8h	
This register reflects the count value of the OA Performance counter A29. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A29 Upper DWord

OAR_OAPERF_A29_UPPER - OAR Aggregate Perf Counter A29 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028ECh

This register enables the current live value of performance counter A29 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A30

OAR_OAPERF_A30 - OAR Aggregate Perf Counter A30		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	028F0h	
This register reflects the count value of the OA Performance counter A30. DefaultValue="00000000h".		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A30 Upper DWord

OAR_OAPERF_A30_UPPER - OAR Aggregate Perf Counter A30 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028F4h

This register enables the current live value of performance counter A30 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A31

OAR_OAPERF_A31 - OAR Aggregate Perf Counter A31

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028F8h

This register reflects the count value of the OA Performance counter A31

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A31 Upper DWord

OAR_OAPERF_A31_UPPER - OAR Aggregate Perf Counter A31 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	028FCh

This register enables the current live value of performance counter A31 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A32

OAR_OAPERF_A32 - OAR Aggregate Perf Counter A32		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02900h	
This register reflects the count value of the OA Performance counter A32.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Aggregate Perf Counter A32 Upper DWord

OAR_OAPERF_A32_UPPER - OAR Aggregate Perf Counter A32 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02904h

This register enables the current live value of performance counter A32 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OARAggregatePerfCounterA33

OAR_OAPERF_A33 - OARAggregatePerfCounterA33		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	02908h	
This register reflects the count value of the OA Performance counter A33		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OARAggregatePerfCounterA33UpperDWord

OAR_OAPERF_A33_UPPER - OARAggregatePerfCounterA33UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0290Ch

This register enables the current live value of performance counter A33 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OARAggregatePerfCounterA34

OAR_OAPERF_A34 - OARAggregatePerfCounterA34		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	029B0h	
This register reflects the count value of the OA Performance Aggregating counter A34		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OARAggregatePerfCounterA34UpperDWord

OAR_OAPERF_A34_UPPER - OARAggregatePerfCounterA34UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	029B4h

This register enables the current live value of performance counter A34 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this upper register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads

OARAggregatePerfCounterA35UpperDWord

OAR_OAPERF_A35_UPPER - OARAggregatePerfCounterA35UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	029BCh

This register enables the current live value of performance counter A35 to be read. Please refer to the detailed description of the aggregating performance counters in the Aggregating Counters section for more details on what event is reported via this upper register.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Boolean_Counter_B0

OAR_OAPERF_B0 - OAR Boolean_Counter_B0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02920h

This register enables the current live value of performance counter B0 to be read. Since what conditions cause B0 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Boolean_Counter_B1

OAR_OAPERF_B1 - OAR Boolean_Counter_B1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02924h

This register enables the current live value of performance counter B1 to be read. Since what conditions cause B1 to increment are defined by the programming of CEC1-0/CEC1-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Boolean_Counter_B2

OAR_OAPERF_B2 - OAR Boolean_Counter_B2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02928h

This register enables the current live value of performance counter B2 to be read. Since what conditions cause B2 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Boolean_Counter_B3

OAR_OAPERF_B3 - OAR Boolean_Counter_B3

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0292Ch

This register enables the current live value of performance counter B3 to be read. Since what conditions cause B3 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Boolean_Counter_B4

OAR_OAPERF_B4 - OAR Boolean_Counter_B4	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02930h

This register enables the current live value of performance counter B4 to be read. Since what conditions cause B4 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Boolean_Counter_B5

OAR_OAPERF_B5 - OAR Boolean_Counter_B5

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02934h

This register enables the current live value of performance counter B5 to be read. Since what conditions cause B5 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Boolean_Counter_B6

OAR_OAPERF_B6 - OAR Boolean_Counter_B6	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02938h

This register enables the current live value of performance counter B6 to be read. Since what conditions cause B6 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Boolean_Counter_B7

OAR_OAPERF_B7 - OAR Boolean_Counter_B7

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0293Ch

This register enables the current live value of performance counter B7 to be read. Since what conditions cause B7 to increment are defined by the programming of CEC0-0/CEC0-1, please refer to the description of these registers and the values they hold to determine what event is reported via this register.

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR GPU Ticks Counter

OAR_GPU_TICKS - OAR GPU Ticks Counter		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	029C0h	
Reading this register returns the live value of the GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.		
DWord	**Bit**	**Description**
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR GPU Ticks Counter Upper DWord

OAR_GPU_TICKS_UPPER - OAR GPU Ticks Counter Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	029C4h

Reading this register returns the live value of the Upper DWord of GPU ticks counter that is sampled and included in the performance counter report header. It increments every GFX clock and hence the number of increments per second changes with GFX frequency.

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the GPU tick counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

OAR Observation Architecture Control

OAR_OACONTROL - OAR Observation Architecture Control

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02960h
Name:	OAR Observation Architecture Control
ShortName:	OAR_OACONTROL

This register controls OAR functionality, report format, and context filtering. If OAR is enabled then it should be enabled in CS as well

DWord	Bit	Description
0	31:4	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	3:1	**Counter Select** Access: R/W _Custom_GTIReset: DEV This field selects which performance counter report format to use, please refer to Performance Counter Report Formats section for more details on the structure of the format.
	0	**Performance Counter Enable** Access: R/W Format: Enable _Custom_GTIReset: DEV Global performance counter enable. If clear, no counting will occur. MI_REPORT_PERF_COUNT is undefined when clear. **Programming Notes** "OAR Context Enable" mode bit in RenderEngne CTX_SR_CTL register must be set when "Programmer Counter Enable" is set. OAC and OAR concurrent enabling is not supported (OAG is recommended instead).

OAR Observation Architecture Status Register

OAR_OASTATUS - OAR Observation Architecture Status Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	02968h
Name:	OAR Observation Architecture Status Register
ShortName:	OAR_OASTATUS

This register provides status of report buffer and overflow conditions as well as status of some flags which hardware needs for internal purpose. Software should not program these status bits. Status bits are active high flags (0=false, 1=true)

DWord	Bit	Description
0	31:22	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	21	**Start Trigger Flag 1** Access: R/W _Custom_GTIReset: DEV Value / Name: 0 **[Default]**; 1 **Programming Notes**: This bit is for HW internal use to context save /restore Start Trigger 1 occurrence On RC6 entry. Software should not program this bit.
	20	**Start Trigger Flag 2** Access: R/W _Custom_GTIReset: DEV Value / Name: 0 **[Default]**; 1 **Programming Notes**: This bit is for HW internal use to context save /restore Start Trigger 2 occurrence On RC6 entry. Software should not program this bit.

OAR_OASTATUS - OAR Observation Architecture Status Register

	19	**Report Trigger Flag 1** Access: R/W _Custom_GTIReset: DEV **Value** / **Name** 0 **[Default]** 1 **Programming Notes** This bit is for HW internal use to context save /restore Report Trigger 1 occurrence On RC6 entry. Software should not program this bit.
	18	**Report Trigger Flag 2** Access: R/W _Custom_GTIReset: DEV **Value** / **Name** 0 **[Default]** 1 **Programming Notes** This bit is for HW internal use to context save /restore Report Trigger 2 occurrence On RC6 entry. Software should not program this bit.
	17:6	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	5:2	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OAR_OASTATUS - OAR Observation Architecture Status Register

	1	**Accumulator Overflow** Access: R/W _Custom_GTIReset: DEV This field indicates that the one or more event accumulator inside the slice-OAunit has overflowed. Once set, this bit will remain set, until SW resets it by either soft reset or writing a 0 to it. **Value** / **Name** / **Description** 0 / **[Default]** / No overflow has occurred. 1 / / Overflow has occurred.
	0	**Counter Overflow** Access: R/W _Custom_GTIReset: DEV This bit is set if any of the counters overflows. This bit can be reset by SW by either soft reset or writing a 0 to it. **Value** / **Name** / **Description** 0 / **[Default]** / Counter Overflow not occurred 1 / / Counter Overflow occurred

Observation Architecture Control per Context

OACTXCONTROL - Observation Architecture Control per Context

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	02360h-02363h
Name:	OACTXCONTROL
ShortName:	OACTXCONTROL_RCSUNIT_BE_COMPUTE

Address:	1A360h-1A363h
Name:	OACTXCONTROL
ShortName:	OACTXCONTROL_CCSUNIT_BE_COMPUTE0

Address:	1C360h-1C363h
Name:	OACTXCONTROL
ShortName:	OACTXCONTROL_CCSUNIT_BE_COMPUTE1

Address:	1E360h-1E363h
Name:	OACTXCONTROL
ShortName:	OACTXCONTROL_CCSUNIT_BE_COMPUTE2

Address:	26360h-26363h
Name:	OACTXCONTROL
ShortName:	OACTXCONTROL_CCSUNIT_BE_COMPUTE3

This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.

DWord	Bit	Description
0	31	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	30:8	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OACTXCONTROL - Observation Architecture Control per Context

7:2 **Timer Period**

Access:	R/W
_Custom_GTIReset:	DEV

Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows:StrobePeriod = MinimumTimeStampPeriod * 2 **(TimerPeriod + 1)**The exponent is defined by this field.

Note: The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.

1 **Timer Enable**

Access:	R/W
_Custom_GTIReset:	DEV

This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report.

When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report trigger function gets enabled only for the selected context. When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts.

Value	Name	Description
0h	Disable **[Default]**	Counter does not get written out on regular interval
1h	Enable	Counter gets written out on regular intervals, defined by the Timer Period

0 **Counter Stop-Resume Mechanism**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
1h		resume counting for all counters

Observation Architecture Head Pointer

OAG_OAHEADPTR - Observation Architecture Head Pointer

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB00h

This register allows SW to program head pointer.

DWord	Bit	Description
0	31:6	**Head Pointer** Access: R/W _Custom_GTIReset: DEV Virtual address of the internal trigger based buffer that is updated by software after consuming reports from the report buffer. This pointer must be updated by SW only when using time or event-based report triggering. **Programming Notes** SW must ensure that Head Pointer and the Tail Pointer match before enabling internally triggered performance counter reporting.
	5:0	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

OUTPUT_CSC_COEFF

OUTPUT_CSC_COEFF

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed

Address:	49050h-49067h
Name:	Pipe Output CSC Coefficients
ShortName:	OUTPUT_CSC_COEFF_A
Reset:	soft

Address:	49150h-49167h
Name:	Pipe Output CSC Coefficients
ShortName:	OUTPUT_CSC_COEFF_B
Reset:	soft

Address:	49250h-49267h
Name:	Pipe Output CSC Coefficients
ShortName:	OUTPUT_CSC_COEFF_C
Reset:	soft

Address:	49350h-49367h
Name:	Pipe Output CSC Coefficients
ShortName:	OUTPUT_CSC_COEFF_D
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
1	31:16	**BY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

OUTPUT_CSC_COEFF		
2	31:16	**RU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
3	31:16	**BU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ
4	31:16	**RV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
5	31:16	**BV** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ

OUTPUT_CSC_POSTOFF

OUTPUT_CSC_POSTOFF

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed

Address:	49074h-4907Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_A
Reset:	soft

Address:	49174h-4917Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_B
Reset:	soft

Address:	49274h-4927Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_C
Reset:	soft

Address:	49374h-4937Fh
Name:	Pipe Output CSC Post-Offsets
ShortName:	OUTPUT_CSC_POSTOFF_D
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit pipe output color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ

OUTPUT_CSC_POSTOFF		
	12:0	**PostCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC Low Offset** Access: Double Buffered This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

OUTPUT_CSC_PREOFF

OUTPUT_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to CSC_MODE
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed

Address:	49068h-49073h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_A
Reset:	soft

Address:	49168h-49173h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_B
Reset:	soft

Address:	49268h-49273h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_C
Reset:	soft

Address:	49368h-49373h
Name:	Pipe Output CSC Pre-Offsets
ShortName:	OUTPUT_CSC_PREOFF_D
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter pipe output color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ

OUTPUT_CSC_PREOFF		
	12:0	**PreCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
2	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Low Offset** Access: Double Buffered This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

Outstanding Page Request Allocation

OPRA_0_2_0_PCI - Outstanding Page Request Allocation		
Register Space:	PCI: 0/2/0	
Size (in bits):	32	
Address:	0030Ch	
DWord	**Bit**	**Description**
0	31:0	**Outstanding Page Req Alloc** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.

Outstanding Page Request Capacity

OPRC_0_2_0_PCI - Outstanding Page Request Capacity

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00308h

DWord	Bit	Description
0	31:0	**Outstanding Page Req Cap** Access: RO _Custom_GTIReset: BUS This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Value: 00000000000000001000000000000000b — Name: 32k **[Default]**

PAGE_FAULT_MODE

PAGE_FAULT_MODE - PAGE_FAULT_MODE

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0E454h
Name:	PAGE_FAULT_MODE
ShortName:	PAGE_FAULT_MODE

This register is written as part of Context Submission to TDL. The data written is the lower 32 bits of the Context Descriptor Format structure.

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:6	**FAULT_MODE** Access: WO **Fault Model:** Applicable only in advanced context Value / Name / Description: 00b / Fault and Hang **[Default]** / In Legacy Context mode, this is the only valid encoding. 01b / Fault and Halt / Restriction : Only valid in Advanced Context mode. 010b / Fault and Stream / Restriction : Only valid in Advanced Context mode. Others / Reserved /
	5:0	**Reserved** Access: RO Format: MBZ

Page Directory Pointer Descriptor - PDP0/PML4/PASID

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02270h-02277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_RCSUNIT_CTX
Address:	22270h-22277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_BCSUNIT_CTX
Address:	1C0270h-1C0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT0_CTX
Address:	1C4270h-1C4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT1_CTX
Address:	1C8270h-1C8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT0_CTX
Address:	1D0270h-1D0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT2_CTX
Address:	1D4270h-1D4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT3_CTX
Address:	1D8270h-1D8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT1_CTX
Address:	1E0270h-1E0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT4_CTX
Address:	1E4270h-1E4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT5_CTX

PDP0 - Page Directory Pointer Descriptor - PDP0/PML4/PASID

Address:	1E8270h-1E8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT2_CTX
Address:	1F0270h-1F0277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT6_CTX
Address:	1F4270h-1F4277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VCSUNIT7_CTX
Address:	1F8270h-1F8277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_VECSUNIT3_CTX
Address:	1A270h-1A277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_CCSUNIT0_CTX
Address:	1C270h-1C277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_CCSUNIT1_CTX
Address:	1E270h-1E277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_CCSUNIT2_CTX
Address:	26270h-26277h
Name:	Page Directory Pointer Descriptor - PDP0/PML4/PASID
ShortName:	PDP0_CCSUNIT3_CTX

PDP0/PML4/PASID: This register can contain three values which depend on the element descriptor definition. **PASID[19:0]:** Populated in the first 20bits of the register and selected when Advanced Context flag is set in the element descriptor in execlist mode of submission. This is not valid in ring buffer mode of scheduling.**PML4[38:12]:** Pointer to base address of PML4 and selected when Legacy Context flag is set and 64b address support is selected.**PDP0[38:12]:** Pointer to one of the four page directory pointer (lowest) and defines the first 0-1GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

Programming Notes
Execlist Based Scheduling: SW should update PDP0/12/3 registers in context image with proper values before submitting the context to HW in execlist mode of scheduling. HW restores these registers as part of context restore to set the PPGTT access accordingly. PPGTT is always enabled in advanced context mode of execlist based scheduling and can be disabled only in legacy context mode. Privilege Access Bit in Element Descriptor controls the PPGTT enabling in legacy context mode.
Ring Buffer Based Scheduling: A write via MMIO to PDP0_DESCRIPROR (lower Dword) triggers the Page Directory Restore in HW when PPGTT is enabled. SW should ensure PDP1/2/3 registers are programmed appropriately prior to programming PDP0. PDP0_DESCRIPTOR lower dword should be programmed at the end. Per-Process GTT Enable Bit in GFX_MODE register controls the PPGTT enabling and disabling. Programming Per-Process GTT Enable Bit in GFX_MODE register doesn't enable/disable the PPGTT translation of memory access immediately; the change comes in to affect only when the Page Directory registers are programmed. Programming Per-Process GTT Enable Bit in GFX_MODE register bit must be followed by programming Page Directory Registers in order to enable or disable the PPGTT translation of memory access. PDP* DESCRIPTOR registers must always be programmed through MI_LOAD_REGISTER_IMMEDIATE command in ring buffer with PDP0_DESCRIPRTOR lower dword written at the end. PDP0/12/3 registers are context save restored. PDP descriptors are context save restored per render context in RCS and must be programmed following MI_SET_CONTEXT command, in case of PDP descriptors programmed without context set (MI_SET_CONTEXT) will get lost on C6 entry/exit. PDP descriptors are context save restored in VCS, BCS and VECS engines and must be programmed following setup of CCID register, in case of PDP descriptors programmed without CCID set will get lost on C6 entry/exit. PDP descriptor registers should be programmed after ensuring the pipe is completely flushed and TLB's invalidated.

DWord	Bit	Description
0	63	**PD Load Busy** Access: RO This read-only field gets set when PDP0 is written to indicating Page Directory Restore activity is in progress and will get reset once the activity is completed.
	62:0	**PDP0 Descriptor** Access: R/W

Page Directory Pointer Descriptor - PDP1

PDP1 - Page Directory Pointer Descriptor - PDP1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02278h-0227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_RCSUNIT_CTX
Address:	22278h-2227Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_BCSUNIT_CTX
Address:	1C0278h-1C027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT0_CTX
Address:	1C4278h-1C427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT1_CTX
Address:	1C8278h-1C827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT0_CTX
Address:	1D0278h-1D027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT2_CTX
Address:	1D4278h-1D427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT3_CTX
Address:	1D8278h-1D827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT1_CTX
Address:	1E0278h-1E027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT4_CTX
Address:	1E4278h-1E427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT5_CTX

PDP1 - Page Directory Pointer Descriptor - PDP1

Address:	1E8278h-1E827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT2_CTX

Address:	1F0278h-1F027Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT6_CTX

Address:	1F4278h-1F427Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VCSUNIT7_CTX

Address:	1F8278h-1F827Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_VECSUNIT3_CTX

Address:	1A278h-1A27Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_CCSUNIT0_CTX

Address:	1C278h-1C27Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_CCSUNIT1_CTX

Address:	1E278h-1E27Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_CCSUNIT2_CTX

Address:	26278h-2627Fh
Name:	Page Directory Pointer Descriptor - PDP1
ShortName:	PDP1_CCSUNIT3_CTX

PDP1[38:12]: Pointer to one of the four page directory pointer (lowest+1) and defines the first 1-2GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported.*Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP1 Descriptor** Access: R/W

Page Directory Pointer Descriptor - PDP2

PDP2 - Page Directory Pointer Descriptor - PDP2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02280h-02287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_RCSUNIT_CTX
Address:	22280h-22287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_BCSUNIT_CTX
Address:	1C0280h-1C0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT0_CTX
Address:	1C4280h-1C4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT1_CTX
Address:	1C8280h-1C8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT0_CTX
Address:	1D0280h-1D0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT2_CTX
Address:	1D4280h-1D4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT3_CTX
Address:	1D8280h-1D8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT1_CTX
Address:	1E0280h-1E0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT4_CTX
Address:	1E4280h-1E4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT5_CTX

PDP2 - Page Directory Pointer Descriptor - PDP2

Address:	1E8280h-1E8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT2_CTX

Address:	1F0280h-1F0287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT6_CTX

Address:	1F4280h-1F4287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VCSUNIT7_CTX

Address:	1F8280h-1F8287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_VECSUNIT3_CTX

Address:	1A280h-1A287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_CCSUNIT0_CTX

Address:	1C280h-1C287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_CCSUNIT1_CTX

Address:	1E280h-1E287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_CCSUNIT2_CTX

Address:	26280h-26287h
Name:	Page Directory Pointer Descriptor - PDP2
ShortName:	PDP2_CCSUNIT3_CTX

PDP2[38:12]: Pointer to one of the four page directory pointer (lowest+2) and defines the first 2-3GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP2 Descriptor** Access: R/W

Page Directory Pointer Descriptor - PDP3

PDP3 - Page Directory Pointer Descriptor - PDP3	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02288h-0228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_RCSUNIT_CTX
Address:	22288h-2228Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_BCSUNIT_CTX
Address:	1C0288h-1C028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT0_CTX
Address:	1C4288h-1C428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT1_CTX
Address:	1C8288h-1C828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT0_CTX
Address:	1D0288h-1D028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT2_CTX
Address:	1D4288h-1D428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT3_CTX
Address:	1D8288h-1D828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT1_CTX
Address:	1E0288h-1E028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT4_CTX
Address:	1E4288h-1E428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT5_CTX

PDP3 - Page Directory Pointer Descriptor - PDP3

Address:	1E8288h-1E828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT2_CTX

Address:	1F0288h-1F028Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT6_CTX

Address:	1F4288h-1F428Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VCSUNIT7_CTX

Address:	1F8288h-1F828Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_VECSUNIT3_CTX

Address:	1A288h-1A28Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_CCSUNIT0_CTX

Address:	1C288h-1C28Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_CCSUNIT1_CTX

Address:	1E288h-1E28Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_CCSUNIT2_CTX

Address:	26288h-2628Fh
Name:	Page Directory Pointer Descriptor - PDP3
ShortName:	PDP3_CCSUNIT3_CTX

PDP3[38:12]: Pointer to one of the four page directory pointer (lowest+3) and defines the first 3-4GB of memory mapping. This is valid when Legacy Context Flag is set and 64bit virtual addressing is not supported. *Note: This is a guest physical address.*

DWord	Bit	Description
0	63:0	**PDP3 Descriptor** Access: R/W

Page Req Queue Tail Shadow Register DW0

PRQTP_DW0 - Page Req Queue Tail Shadow Register DW0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00EC4h-00EC7h	
DWord	**Bit**	**Description**
0	31:0	**TailPtr** Access: R/W Shadow register for Page Req Queue Tail register DW0. Usage: GAM will provide the data which is readable via address F0C8.

Page Req Queue Tail Shadow Register DW1

PRQTP_DW1 - Page Req Queue Tail Shadow Register DW1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00EC8h-00ECBh	
DWord	**Bit**	**Description**
0	31:0	**TailPtr** Access: R/W Shadow register for Page Req Queue Tail register DW1. Usage: GAM will provide the data which is readable via address F0CC.

Page Request Control

PR_CTRL_0_2_0_PCI - Page Request Control		
Register Space:	PCI: 0/2/0	
Size (in bits):	16	
Address:	00304h	

DWord	Bit	Description
0	15:2	**Reserved** Access: RO Format: MBZ
	1	**Reset** Default Value: 0b Access: RO _Custom_GTIReset: BUS When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit Counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value when the PRE field is set. Processor graphics does not use this field, and hardwires it as read-only (0).
	0	**Page-Request Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page responses is not yet received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.

Page Request Extended Capability Header

PR_EXTCAP_0_2_0_PCI - Page Request Extended Capability Header

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00300h

Page Request Extended Capability reports support for Page Request Services for this function.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Access: RO Variant _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list. A value of 000h (Default) indicates the end of the PCI-Express Extended Capability linked list. Value: 000000000000b — Name: **[Default]**
	19:16	**Version** Default Value: 0001b Access: RO _Custom_GTIReset: BUS Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0013h Page Request Services Capability Access: RO _Custom_GTIReset: BUS Indicates the type of Extended Capability.

Page Request Queue Address Register 0

PAGEREQ_QADDR_0 - Page Request Queue Address Register 0	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0F0D0h

Register to configure the base address and size of the page request queue.

DWord	Bit	Description
0	31:12	**Page Request Queue Base Register** Default Value: 00000h Access: R/W This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.
	11:3	**Reserved** Access: RO Format: MBZ
	2:0	**Queue Size** Default Value: 000b Access: R/W This field specifies the size of the page request queue. A value of X in this field indicates a page request queue of (2X) 4KB pages. The number of entries in the invalidation queue is 2(X+8).

Page Request Queue Address Register 1

PAGEREQ_QADDR_1 - Page Request Queue Address Register 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	0F0D4h	
Register to configure the base address and size of the page request queue.		
DWord	**Bit**	**Description**
0	31:0	**Page Request Queue Base Register** Default Value: 00000000h Access: R/W This field points to the base of 4KB aligned invalidation request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.

Page Request Queue Head Register 0

PAGEREQ_QHEAD_0 - Page Request Queue Head Register 0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	0F0C0h	
Register indicating the page request queue head.		

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:4	**Queue Head** Default Value: 000000000000000b Access: R/W Specifies the offset (128-bit aligned) to the page request queue for the command that is processed next by software. GFX implementation: GFX has to read the content of the Head pointer as tail pointer gets close to it to prevent overflows in page request queue.
	3:0	**Reserved** Access: RO Format: MBZ

Page Request Queue Head Register 1

PAGEREQ_QHEAD_1 - Page Request Queue Head Register 1	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	0F0C4h

Register indicating the page request queue head.

DWord	Bit	Description
0	31:0	**Page Request Queue Head Register 1 Reserved** Default Value: 00000000h Access: RO Bit[63:32]: Reserved.

Page Request Queue Tail Register 0

PAGEREQ_QTAIL_0 - Page Request Queue Tail Register 0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	0F0C8h	
Register indicating the page request queue tail.		
DWord	**Bit**	**Description**
0	31:1	**Queue Tail** Default Value: 00000000000000000000000000000000b Access: R/W Bit[31:19]: Reserved. Bit[18:4]: Specifies the offset (128-bit aligned) to the page request queue for the request that is written next by hardware. GFX Implementation: GT manages the tail pointer value as part of page requests. The value can be acquired as part of the RC6 exit. Bit[3:1]: Reserved.
	0	**Valid Bit** Default Value: 0b Access: R/W This bit can only be cleared by SW, which also clears the other fields.

Page Request Queue Tail Register 1

PAGEREQ_QTAIL_1 - Page Request Queue Tail Register 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	0F0CCh	
Register indicating the page request queue tail.		
DWord	**Bit**	**Description**
0	31:0	**Page Request Queue Tail Register 1 Reserved** Default Value: 00000000h Access: RO Bit[63:32]: Reserved.

Page Request Status

PR_STATUS_0_2_0_PCI - Page Request Status

Register Space: PCI: 0/2/0
Size (in bits): 16

Address: 00306h

DWord	Bit	Description
0	15	**PRG Response PASID Required** Default Value: 1b Access: RO _Custom_GTIReset: BUS If set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding page requests had a PASID TLP Prefix. If Clear, the function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is Rsvd if the Function does not support the PASID TLP Prefix.
	14:9	**Reserved** Access: RO Format: MBZ
	8	**Stopped** Default Value: 1b Access: RO _Custom_GTIReset: BUS When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests.
	7:2	**Reserved** Access: RO Format: MBZ
	1	**Unexpected Page Request Group Index** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: BUS When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.

PR_STATUS_0_2_0_PCI - Page Request Status

	0	**Response Failure** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: BUS When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host (any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field.

PAK_NUM_OF_SLICES

PAK_NUM_OF_SLICES - PAK_NUM_OF_SLICES		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	12954h	
ShortName:	PAK_NUM_OF_SLICES1	
Address:	1C954h	
ShortName:	PAK_NUM_OF_SLICES2	

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Number of slices in a frame.** Access: RO This field indicates number of slices in the current frame. This register is updated at the end of each slice.

PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	128E8h

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21	**Incorrect IntraMBFlag in I-slice(AVCf)** Access: RO
	20	**Out of Range Symbol Code(AVC/mpeg2)** Access: RO
	19	**Incorrect MBType(AVC/mpeg2** Access: RO
	18	**Motion Vectors are not inside the frame boundary(mpeg2)** Access: RO
	17	**Scale code is zero(mpeg2)** Access: RO
	16	**Incorrect DCTtype for given motionType(mpeg2)** Access: RO
	15:8	**MB Y-position** Access: RO This field indicates Macro Block(MB) Y- position where an error occurred while encoding.
	7:0	**MB X-position** Access: RO This field indicates Macro Block(MB) X- position where an error occurred while encoding.

PAK_Stream-Out Report (Warnings)

PAK_WARN - PAK_Stream-Out Report (Warnings)		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128E4h	

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21	**Skip Run Greater Than 8192 (AVC)** Access: RO
	20	**Incorrect SkipMB (AVC and mpeg2)** Access: RO
	19	**Incorrect MV difference for dual-prime MB (mpeg2)** Access: RO
	18	**End of Slice signal missing on last MB of a Row(mpeg2)** Access: RO
	17	**Incorrect DCT type for field picture** Access: RO
	16	**MVs are not within defined range by fcode** Access: RO
	15:8	**MB Y-position** Access: RO
	7:0	**MB X-position** Access: RO

PAK Report Running Status

PAK_REPORT_STAT - PAK Report Running Status

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	128ECh

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**PAK Status** Access: RO Value / Name / Description: 0 — PAK engine is IDLE 1 — PAK engine is currently generating bit stream.

PAL_EXT_GC_MAX

PAL_EXT_GC_MAX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	96
Address:	4A420h-4A42Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_A
Reset:	soft
Address:	4AC20h-4AC2Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_B
Reset:	soft
Address:	4B420h-4B42Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_C
Reset:	soft
Address:	4BC20h-4BC2Bh
Name:	Pipe Extended Gamma Correction Max
ShortName:	PAL_EXT_GC_MAX_D
Reset:	soft

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:0	**Red Ext Max GC Point** Default Value: 1111111111111111b Access: R/W Format: U3.16 The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.
1	31:19	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">PAL_EXT_GC_MAX</th></tr>
<tr><td></td><td>18:0</td><td>Green Ext Max GC Point<table><tr><td>Default Value:</td><td>1111111111111111b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td>Format:</td><td>U3.16</td></tr></table>The extended point for green color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.</td></tr>
<tr><td rowspan="2">2</td><td>31:19</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>18:0</td><td>Blue Ext Max GC Point<table><tr><td>Default Value:</td><td>1111111111111111b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td>Format:</td><td>U3.16</td></tr></table>The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.</td></tr>
</table>

PAL_EXT2_GC_MAX

PAL_EXT2_GC_MAX	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	96
Address:	4A430h-4A43Bh
Name:	Pipe Extended Second Gamma Correction Max
ShortName:	PAL_EXT2_GC_MAX_A
Reset:	soft
Address:	4AC30h-4AC3Bh
Name:	Pipe Extended Second Gamma Correction Max
ShortName:	PAL_EXT2_GC_MAX_B
Reset:	soft
Address:	4B430h-4B43Bh
Name:	Pipe Extended Second Gamma Correction Max
ShortName:	PAL_EXT2_GC_MAX_C
Reset:	soft
Address:	4BC30h-4BC3Bh
Name:	Pipe Extended Second Gamma Correction Max
ShortName:	PAL_EXT2_GC_MAX_D
Reset:	soft

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:0	**Red Ext Max GC Point** Default Value: 1111111111111111b Access: R/W Format: U3.16 The extended point for red color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.
1	31:19	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">PAL_EXT2_GC_MAX</th></tr>
<tr><td></td><td>18:0</td><td>Green Ext Max GC Point<table><tr><td>Default Value:</td><td>1111111111111111b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td>Format:</td><td>U3.16</td></tr></table>The extended point for green color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.</td></tr>
<tr><td rowspan="2">2</td><td>31:19</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>18:0</td><td>Blue Ext Max GC Point<table><tr><td>Default Value:</td><td>1111111111111111b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td>Format:</td><td>U3.16</td></tr></table>The extended point for blue color channel gamma correction. This value is represented in a 3.16 format with 3 integer and 16 fractional bits.</td></tr>
</table>

PAL_GC_MAX

PAL_GC_MAX		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	96	
Address:	4A410h-4A41Bh	
Name:	Pipe Gamma Correction Max	
ShortName:	PAL_GC_MAX_A	
Reset:	soft	
Address:	4AC10h-4AC1Bh	
Name:	Pipe Gamma Correction Max	
ShortName:	PAL_GC_MAX_B	
Reset:	soft	
Address:	4B410h-4B41Bh	
Name:	Pipe Gamma Correction Max	
ShortName:	PAL_GC_MAX_C	
Reset:	soft	
Address:	4BC10h-4BC1Bh	
Name:	Pipe Gamma Correction Max	
ShortName:	PAL_GC_MAX_D	
Reset:	soft	
Address:	4A548h-4A553h	
Name:	Pipe CC2 Gamma Correction Max	
ShortName:	PAL_GC_MAX_CC2_A	
Reset:	soft	
Address:	4AD48h-4AD53h	
Name:	Pipe CC2 Gamma Correction Max	
ShortName:	PAL_GC_MAX_CC2_B	
Reset:	soft	

DWord	Bit	Description	
0	31:17	**Reserved**	
		Access:	RO
		Format:	MBZ

PAL_GC_MAX

	16:0	**Red Max GC Point** Default Value: 10000000000000000b Access: R/W Format: U1.16 **Description** The 513th entry for the red color channel of the 12 bit interpolated gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. The 511th entry for the red color channel of the 12 bit logarithmic gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** The value should always be programmed to be less than or equal to 1.0.
1	31:17	**Reserved** Access: RO Format: MBZ
	16:0	**Green Max GC Point** Default Value: 10000000000000000b Access: R/W Format: U1.16 **Description** The 511th entry for the green color channel of the 12 bit logarithmic gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** The value should always be programmed to be less than or equal to 1.0.
2	31:17	**Reserved** Access: RO Format: MBZ

PAL_GC_MAX

	16:0	**Blue Max GC Point** Default Value: 10000000000000000b Access: R/W Format: U1.16 **Description** The 511th entry for the blue color channel of the 12 bit logarithmic gamma correction. This value is represented in a 1.16 format with 1 integer and 16 fractional bits. **Restriction** The value should always be programmed to be less than or equal to 1.0.

PAL_LGC

PAL_LGC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A000h-4A003h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_0_A
Reset:	soft
Address:	4A004h-4A007h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_1_A
Reset:	soft
Address:	4A008h-4A00Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_2_A
Reset:	soft
Address:	4A00Ch-4A00Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_3_A
Reset:	soft
Address:	4A010h-4A013h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_4_A
Reset:	soft
Address:	4A014h-4A017h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_5_A
Reset:	soft
Address:	4A018h-4A01Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_6_A
Reset:	soft

Address:	4A01Ch-4A01Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_7_A
Reset:	soft
Address:	4A020h-4A023h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_8_A
Reset:	soft
Address:	4A024h-4A027h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_9_A
Reset:	soft
Address:	4A028h-4A02Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_10_A
Reset:	soft
Address:	4A02Ch-4A02Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_11_A
Reset:	soft
Address:	4A030h-4A033h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_12_A
Reset:	soft
Address:	4A034h-4A037h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_13_A
Reset:	soft
Address:	4A038h-4A03Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_14_A
Reset:	soft
Address:	4A03Ch-4A03Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_15_A
Reset:	soft

Address:	4A040h-4A043h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_16_A
Reset:	soft
Address:	4A044h-4A047h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_17_A
Reset:	soft
Address:	4A048h-4A04Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_18_A
Reset:	soft
Address:	4A04Ch-4A04Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_19_A
Reset:	soft
Address:	4A050h-4A053h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_20_A
Reset:	soft
Address:	4A054h-4A057h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_21_A
Reset:	soft
Address:	4A058h-4A05Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_22_A
Reset:	soft
Address:	4A05Ch-4A05Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_23_A
Reset:	soft
Address:	4A060h-4A063h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_24_A
Reset:	soft

Address:	4A064h-4A067h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_25_A
Reset:	soft
Address:	4A068h-4A06Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_26_A
Reset:	soft
Address:	4A06Ch-4A06Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_27_A
Reset:	soft
Address:	4A070h-4A073h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_28_A
Reset:	soft
Address:	4A074h-4A077h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_29_A
Reset:	soft
Address:	4A078h-4A07Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_30_A
Reset:	soft
Address:	4A07Ch-4A07Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_31_A
Reset:	soft
Address:	4A080h-4A083h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_32_A
Reset:	soft
Address:	4A084h-4A087h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_33_A
Reset:	soft

Address:	4A088h-4A08Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_34_A
Reset:	soft
Address:	4A08Ch-4A08Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_35_A
Reset:	soft
Address:	4A090h-4A093h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_36_A
Reset:	soft
Address:	4A094h-4A097h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_37_A
Reset:	soft
Address:	4A098h-4A09Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_38_A
Reset:	soft
Address:	4A09Ch-4A09Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_39_A
Reset:	soft
Address:	4A0A0h-4A0A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_40_A
Reset:	soft
Address:	4A0A4h-4A0A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_41_A
Reset:	soft
Address:	4A0A8h-4A0ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_42_A
Reset:	soft

Address:	4A0ACh-4A0AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_43_A
Reset:	soft
Address:	4A0B0h-4A0B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_44_A
Reset:	soft
Address:	4A0B4h-4A0B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_45_A
Reset:	soft
Address:	4A0B8h-4A0BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_46_A
Reset:	soft
Address:	4A0BCh-4A0BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_47_A
Reset:	soft
Address:	4A0C0h-4A0C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_48_A
Reset:	soft
Address:	4A0C4h-4A0C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_49_A
Reset:	soft
Address:	4A0C8h-4A0CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_50_A
Reset:	soft
Address:	4A0CCh-4A0CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_51_A
Reset:	soft

Address:	4A0D0h-4A0D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_52_A
Reset:	soft
Address:	4A0D4h-4A0D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_53_A
Reset:	soft
Address:	4A0D8h-4A0DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_54_A
Reset:	soft
Address:	4A0DCh-4A0DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_55_A
Reset:	soft
Address:	4A0E0h-4A0E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_56_A
Reset:	soft
Address:	4A0E4h-4A0E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_57_A
Reset:	soft
Address:	4A0E8h-4A0EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_58_A
Reset:	soft
Address:	4A0ECh-4A0EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_59_A
Reset:	soft
Address:	4A0F0h-4A0F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_60_A
Reset:	soft

Address:	4A0F4h-4A0F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_61_A
Reset:	soft
Address:	4A0F8h-4A0FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_62_A
Reset:	soft
Address:	4A0FCh-4A0FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_63_A
Reset:	soft
Address:	4A100h-4A103h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_64_A
Reset:	soft
Address:	4A104h-4A107h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_65_A
Reset:	soft
Address:	4A108h-4A10Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_66_A
Reset:	soft
Address:	4A10Ch-4A10Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_67_A
Reset:	soft
Address:	4A110h-4A113h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_68_A
Reset:	soft
Address:	4A114h-4A117h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_69_A
Reset:	soft

Address:	4A118h-4A11Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_70_A
Reset:	soft
Address:	4A11Ch-4A11Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_71_A
Reset:	soft
Address:	4A120h-4A123h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_72_A
Reset:	soft
Address:	4A124h-4A127h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_73_A
Reset:	soft
Address:	4A128h-4A12Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_74_A
Reset:	soft
Address:	4A12Ch-4A12Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_75_A
Reset:	soft
Address:	4A130h-4A133h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_76_A
Reset:	soft
Address:	4A134h-4A137h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_77_A
Reset:	soft
Address:	4A138h-4A13Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_78_A
Reset:	soft

Address:	4A13Ch-4A13Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_79_A
Reset:	soft
Address:	4A140h-4A143h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_80_A
Reset:	soft
Address:	4A144h-4A147h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_81_A
Reset:	soft
Address:	4A148h-4A14Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_82_A
Reset:	soft
Address:	4A14Ch-4A14Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_83_A
Reset:	soft
Address:	4A150h-4A153h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_84_A
Reset:	soft
Address:	4A154h-4A157h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_85_A
Reset:	soft
Address:	4A158h-4A15Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_86_A
Reset:	soft
Address:	4A15Ch-4A15Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_87_A
Reset:	soft

Address:	4A160h-4A163h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_88_A
Reset:	soft
Address:	4A164h-4A167h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_89_A
Reset:	soft
Address:	4A168h-4A16Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_90_A
Reset:	soft
Address:	4A16Ch-4A16Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_91_A
Reset:	soft
Address:	4A170h-4A173h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_92_A
Reset:	soft
Address:	4A174h-4A177h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_93_A
Reset:	soft
Address:	4A178h-4A17Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_94_A
Reset:	soft
Address:	4A17Ch-4A17Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_95_A
Reset:	soft
Address:	4A180h-4A183h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_96_A
Reset:	soft

Address:	4A184h-4A187h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_97_A
Reset:	soft
Address:	4A188h-4A18Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_98_A
Reset:	soft
Address:	4A18Ch-4A18Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_99_A
Reset:	soft
Address:	4A190h-4A193h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_100_A
Reset:	soft
Address:	4A194h-4A197h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_101_A
Reset:	soft
Address:	4A198h-4A19Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_102_A
Reset:	soft
Address:	4A19Ch-4A19Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_103_A
Reset:	soft
Address:	4A1A0h-4A1A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_104_A
Reset:	soft
Address:	4A1A4h-4A1A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_105_A
Reset:	soft

Address:	4A1A8h-4A1ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_106_A
Reset:	soft
Address:	4A1ACh-4A1AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_107_A
Reset:	soft
Address:	4A1B0h-4A1B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_108_A
Reset:	soft
Address:	4A1B4h-4A1B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_109_A
Reset:	soft
Address:	4A1B8h-4A1BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_110_A
Reset:	soft
Address:	4A1BCh-4A1BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_111_A
Reset:	soft
Address:	4A1C0h-4A1C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_112_A
Reset:	soft
Address:	4A1C4h-4A1C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_113_A
Reset:	soft
Address:	4A1C8h-4A1CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_114_A
Reset:	soft

Address:	4A1CCh-4A1CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_115_A
Reset:	soft
Address:	4A1D0h-4A1D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_116_A
Reset:	soft
Address:	4A1D4h-4A1D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_117_A
Reset:	soft
Address:	4A1D8h-4A1DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_118_A
Reset:	soft
Address:	4A1DCh-4A1DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_119_A
Reset:	soft
Address:	4A1E0h-4A1E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_120_A
Reset:	soft
Address:	4A1E4h-4A1E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_121_A
Reset:	soft
Address:	4A1E8h-4A1EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_122_A
Reset:	soft
Address:	4A1ECh-4A1EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_123_A
Reset:	soft

Address:	4A1F0h-4A1F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_124_A
Reset:	soft
Address:	4A1F4h-4A1F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_125_A
Reset:	soft
Address:	4A1F8h-4A1FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_126_A
Reset:	soft
Address:	4A1FCh-4A1FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_127_A
Reset:	soft
Address:	4A200h-4A203h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_128_A
Reset:	soft
Address:	4A204h-4A207h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_129_A
Reset:	soft
Address:	4A208h-4A20Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_130_A
Reset:	soft
Address:	4A20Ch-4A20Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_131_A
Reset:	soft
Address:	4A210h-4A213h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_132_A
Reset:	soft

Address:	4A214h-4A217h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_133_A
Reset:	soft
Address:	4A218h-4A21Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_134_A
Reset:	soft
Address:	4A21Ch-4A21Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_135_A
Reset:	soft
Address:	4A220h-4A223h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_136_A
Reset:	soft
Address:	4A224h-4A227h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_137_A
Reset:	soft
Address:	4A228h-4A22Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_138_A
Reset:	soft
Address:	4A22Ch-4A22Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_139_A
Reset:	soft
Address:	4A230h-4A233h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_140_A
Reset:	soft
Address:	4A234h-4A237h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_141_A
Reset:	soft

Address:	4A238h-4A23Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_142_A
Reset:	soft
Address:	4A23Ch-4A23Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_143_A
Reset:	soft
Address:	4A240h-4A243h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_144_A
Reset:	soft
Address:	4A244h-4A247h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_145_A
Reset:	soft
Address:	4A248h-4A24Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_146_A
Reset:	soft
Address:	4A24Ch-4A24Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_147_A
Reset:	soft
Address:	4A250h-4A253h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_148_A
Reset:	soft
Address:	4A254h-4A257h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_149_A
Reset:	soft
Address:	4A258h-4A25Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_150_A
Reset:	soft

Address:	4A25Ch-4A25Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_151_A
Reset:	soft
Address:	4A260h-4A263h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_152_A
Reset:	soft
Address:	4A264h-4A267h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_153_A
Reset:	soft
Address:	4A268h-4A26Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_154_A
Reset:	soft
Address:	4A26Ch-4A26Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_155_A
Reset:	soft
Address:	4A270h-4A273h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_156_A
Reset:	soft
Address:	4A274h-4A277h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_157_A
Reset:	soft
Address:	4A278h-4A27Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_158_A
Reset:	soft
Address:	4A27Ch-4A27Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_159_A
Reset:	soft

Address:	4A280h-4A283h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_160_A
Reset:	soft
Address:	4A284h-4A287h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_161_A
Reset:	soft
Address:	4A288h-4A28Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_162_A
Reset:	soft
Address:	4A28Ch-4A28Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_163_A
Reset:	soft
Address:	4A290h-4A293h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_164_A
Reset:	soft
Address:	4A294h-4A297h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_165_A
Reset:	soft
Address:	4A298h-4A29Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_166_A
Reset:	soft
Address:	4A29Ch-4A29Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_167_A
Reset:	soft
Address:	4A2A0h-4A2A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_168_A
Reset:	soft

Address:	4A2A4h-4A2A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_169_A
Reset:	soft
Address:	4A2A8h-4A2ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_170_A
Reset:	soft
Address:	4A2ACh-4A2AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_171_A
Reset:	soft
Address:	4A2B0h-4A2B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_172_A
Reset:	soft
Address:	4A2B4h-4A2B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_173_A
Reset:	soft
Address:	4A2B8h-4A2BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_174_A
Reset:	soft
Address:	4A2BCh-4A2BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_175_A
Reset:	soft
Address:	4A2C0h-4A2C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_176_A
Reset:	soft
Address:	4A2C4h-4A2C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_177_A
Reset:	soft

Address:	4A2C8h-4A2CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_178_A
Reset:	soft
Address:	4A2CCh-4A2CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_179_A
Reset:	soft
Address:	4A2D0h-4A2D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_180_A
Reset:	soft
Address:	4A2D4h-4A2D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_181_A
Reset:	soft
Address:	4A2D8h-4A2DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_182_A
Reset:	soft
Address:	4A2DCh-4A2DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_183_A
Reset:	soft
Address:	4A2E0h-4A2E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_184_A
Reset:	soft
Address:	4A2E4h-4A2E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_185_A
Reset:	soft
Address:	4A2E8h-4A2EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_186_A
Reset:	soft

Address:	4A2ECh-4A2EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_187_A
Reset:	soft
Address:	4A2F0h-4A2F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_188_A
Reset:	soft
Address:	4A2F4h-4A2F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_189_A
Reset:	soft
Address:	4A2F8h-4A2FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_190_A
Reset:	soft
Address:	4A2FCh-4A2FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_191_A
Reset:	soft
Address:	4A300h-4A303h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_192_A
Reset:	soft
Address:	4A304h-4A307h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_193_A
Reset:	soft
Address:	4A308h-4A30Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_194_A
Reset:	soft
Address:	4A30Ch-4A30Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_195_A
Reset:	soft

Address:	4A310h-4A313h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_196_A
Reset:	soft
Address:	4A314h-4A317h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_197_A
Reset:	soft
Address:	4A318h-4A31Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_198_A
Reset:	soft
Address:	4A31Ch-4A31Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_199_A
Reset:	soft
Address:	4A320h-4A323h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_200_A
Reset:	soft
Address:	4A324h-4A327h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_201_A
Reset:	soft
Address:	4A328h-4A32Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_202_A
Reset:	soft
Address:	4A32Ch-4A32Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_203_A
Reset:	soft
Address:	4A330h-4A333h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_204_A
Reset:	soft

Address:	4A334h-4A337h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_205_A
Reset:	soft
Address:	4A338h-4A33Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_206_A
Reset:	soft
Address:	4A33Ch-4A33Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_207_A
Reset:	soft
Address:	4A340h-4A343h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_208_A
Reset:	soft
Address:	4A344h-4A347h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_209_A
Reset:	soft
Address:	4A348h-4A34Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_210_A
Reset:	soft
Address:	4A34Ch-4A34Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_211_A
Reset:	soft
Address:	4A350h-4A353h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_212_A
Reset:	soft
Address:	4A354h-4A357h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_213_A
Reset:	soft

Address:	4A358h-4A35Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_214_A
Reset:	soft
Address:	4A35Ch-4A35Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_215_A
Reset:	soft
Address:	4A360h-4A363h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_216_A
Reset:	soft
Address:	4A364h-4A367h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_217_A
Reset:	soft
Address:	4A368h-4A36Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_218_A
Reset:	soft
Address:	4A36Ch-4A36Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_219_A
Reset:	soft
Address:	4A370h-4A373h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_220_A
Reset:	soft
Address:	4A374h-4A377h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_221_A
Reset:	soft
Address:	4A378h-4A37Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_222_A
Reset:	soft

Address:	4A37Ch-4A37Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_223_A
Reset:	soft
Address:	4A380h-4A383h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_224_A
Reset:	soft
Address:	4A384h-4A387h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_225_A
Reset:	soft
Address:	4A388h-4A38Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_226_A
Reset:	soft
Address:	4A38Ch-4A38Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_227_A
Reset:	soft
Address:	4A390h-4A393h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_228_A
Reset:	soft
Address:	4A394h-4A397h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_229_A
Reset:	soft
Address:	4A398h-4A39Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_230_A
Reset:	soft
Address:	4A39Ch-4A39Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_231_A
Reset:	soft

Address:	4A3A0h-4A3A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_232_A
Reset:	soft
Address:	4A3A4h-4A3A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_233_A
Reset:	soft
Address:	4A3A8h-4A3ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_234_A
Reset:	soft
Address:	4A3ACh-4A3AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_235_A
Reset:	soft
Address:	4A3B0h-4A3B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_236_A
Reset:	soft
Address:	4A3B4h-4A3B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_237_A
Reset:	soft
Address:	4A3B8h-4A3BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_238_A
Reset:	soft
Address:	4A3BCh-4A3BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_239_A
Reset:	soft
Address:	4A3C0h-4A3C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_240_A
Reset:	soft

Address:	4A3C4h-4A3C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_241_A
Reset:	soft
Address:	4A3C8h-4A3CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_242_A
Reset:	soft
Address:	4A3CCh-4A3CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_243_A
Reset:	soft
Address:	4A3D0h-4A3D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_244_A
Reset:	soft
Address:	4A3D4h-4A3D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_245_A
Reset:	soft
Address:	4A3D8h-4A3DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_246_A
Reset:	soft
Address:	4A3DCh-4A3DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_247_A
Reset:	soft
Address:	4A3E0h-4A3E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_248_A
Reset:	soft
Address:	4A3E4h-4A3E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_249_A
Reset:	soft

Address:	4A3E8h-4A3EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_250_A
Reset:	soft
Address:	4A3ECh-4A3EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_251_A
Reset:	soft
Address:	4A3F0h-4A3F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_252_A
Reset:	soft
Address:	4A3F4h-4A3F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_253_A
Reset:	soft
Address:	4A3F8h-4A3FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_254_A
Reset:	soft
Address:	4A3FCh-4A3FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_255_A
Reset:	soft
Address:	4A800h-4A803h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_0_B
Reset:	soft
Address:	4A804h-4A807h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_1_B
Reset:	soft
Address:	4A808h-4A80Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_2_B
Reset:	soft

Address:	4A80Ch-4A80Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_3_B
Reset:	soft
Address:	4A810h-4A813h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_4_B
Reset:	soft
Address:	4A814h-4A817h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_5_B
Reset:	soft
Address:	4A818h-4A81Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_6_B
Reset:	soft
Address:	4A81Ch-4A81Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_7_B
Reset:	soft
Address:	4A820h-4A823h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_8_B
Reset:	soft
Address:	4A824h-4A827h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_9_B
Reset:	soft
Address:	4A828h-4A82Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_10_B
Reset:	soft
Address:	4A82Ch-4A82Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_11_B
Reset:	soft

Address:	4A830h-4A833h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_12_B
Reset:	soft
Address:	4A834h-4A837h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_13_B
Reset:	soft
Address:	4A838h-4A83Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_14_B
Reset:	soft
Address:	4A83Ch-4A83Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_15_B
Reset:	soft
Address:	4A840h-4A843h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_16_B
Reset:	soft
Address:	4A844h-4A847h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_17_B
Reset:	soft
Address:	4A848h-4A84Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_18_B
Reset:	soft
Address:	4A84Ch-4A84Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_19_B
Reset:	soft
Address:	4A850h-4A853h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_20_B
Reset:	soft

Address:	4A854h-4A857h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_21_B
Reset:	soft
Address:	4A858h-4A85Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_22_B
Reset:	soft
Address:	4A85Ch-4A85Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_23_B
Reset:	soft
Address:	4A860h-4A863h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_24_B
Reset:	soft
Address:	4A864h-4A867h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_25_B
Reset:	soft
Address:	4A868h-4A86Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_26_B
Reset:	soft
Address:	4A86Ch-4A86Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_27_B
Reset:	soft
Address:	4A870h-4A873h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_28_B
Reset:	soft
Address:	4A874h-4A877h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_29_B
Reset:	soft

Address:	4A878h-4A87Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_30_B
Reset:	soft
Address:	4A87Ch-4A87Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_31_B
Reset:	soft
Address:	4A880h-4A883h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_32_B
Reset:	soft
Address:	4A884h-4A887h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_33_B
Reset:	soft
Address:	4A888h-4A88Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_34_B
Reset:	soft
Address:	4A88Ch-4A88Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_35_B
Reset:	soft
Address:	4A890h-4A893h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_36_B
Reset:	soft
Address:	4A894h-4A897h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_37_B
Reset:	soft
Address:	4A898h-4A89Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_38_B
Reset:	soft

Address:	4A89Ch-4A89Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_39_B
Reset:	soft
Address:	4A8A0h-4A8A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_40_B
Reset:	soft
Address:	4A8A4h-4A8A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_41_B
Reset:	soft
Address:	4A8A8h-4A8ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_42_B
Reset:	soft
Address:	4A8ACh-4A8AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_43_B
Reset:	soft
Address:	4A8B0h-4A8B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_44_B
Reset:	soft
Address:	4A8B4h-4A8B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_45_B
Reset:	soft
Address:	4A8B8h-4A8BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_46_B
Reset:	soft
Address:	4A8BCh-4A8BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_47_B
Reset:	soft

Address:	4A8C0h-4A8C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_48_B
Reset:	soft
Address:	4A8C4h-4A8C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_49_B
Reset:	soft
Address:	4A8C8h-4A8CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_50_B
Reset:	soft
Address:	4A8CCh-4A8CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_51_B
Reset:	soft
Address:	4A8D0h-4A8D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_52_B
Reset:	soft
Address:	4A8D4h-4A8D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_53_B
Reset:	soft
Address:	4A8D8h-4A8DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_54_B
Reset:	soft
Address:	4A8DCh-4A8DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_55_B
Reset:	soft
Address:	4A8E0h-4A8E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_56_B
Reset:	soft

Address:	4A8E4h-4A8E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_57_B
Reset:	soft
Address:	4A8E8h-4A8EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_58_B
Reset:	soft
Address:	4A8ECh-4A8EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_59_B
Reset:	soft
Address:	4A8F0h-4A8F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_60_B
Reset:	soft
Address:	4A8F4h-4A8F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_61_B
Reset:	soft
Address:	4A8F8h-4A8FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_62_B
Reset:	soft
Address:	4A8FCh-4A8FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_63_B
Reset:	soft
Address:	4A900h-4A903h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_64_B
Reset:	soft
Address:	4A904h-4A907h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_65_B
Reset:	soft

Address:	4A908h-4A90Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_66_B
Reset:	soft
Address:	4A90Ch-4A90Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_67_B
Reset:	soft
Address:	4A910h-4A913h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_68_B
Reset:	soft
Address:	4A914h-4A917h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_69_B
Reset:	soft
Address:	4A918h-4A91Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_70_B
Reset:	soft
Address:	4A91Ch-4A91Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_71_B
Reset:	soft
Address:	4A920h-4A923h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_72_B
Reset:	soft
Address:	4A924h-4A927h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_73_B
Reset:	soft
Address:	4A928h-4A92Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_74_B
Reset:	soft

Address:	4A92Ch-4A92Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_75_B
Reset:	soft
Address:	4A930h-4A933h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_76_B
Reset:	soft
Address:	4A934h-4A937h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_77_B
Reset:	soft
Address:	4A938h-4A93Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_78_B
Reset:	soft
Address:	4A93Ch-4A93Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_79_B
Reset:	soft
Address:	4A940h-4A943h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_80_B
Reset:	soft
Address:	4A944h-4A947h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_81_B
Reset:	soft
Address:	4A948h-4A94Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_82_B
Reset:	soft
Address:	4A94Ch-4A94Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_83_B
Reset:	soft

Address:	4A950h-4A953h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_84_B
Reset:	soft
Address:	4A954h-4A957h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_85_B
Reset:	soft
Address:	4A958h-4A95Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_86_B
Reset:	soft
Address:	4A95Ch-4A95Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_87_B
Reset:	soft
Address:	4A960h-4A963h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_88_B
Reset:	soft
Address:	4A964h-4A967h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_89_B
Reset:	soft
Address:	4A968h-4A96Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_90_B
Reset:	soft
Address:	4A96Ch-4A96Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_91_B
Reset:	soft
Address:	4A970h-4A973h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_92_B
Reset:	soft

Address:	4A974h-4A977h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_93_B
Reset:	soft
Address:	4A978h-4A97Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_94_B
Reset:	soft
Address:	4A97Ch-4A97Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_95_B
Reset:	soft
Address:	4A980h-4A983h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_96_B
Reset:	soft
Address:	4A984h-4A987h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_97_B
Reset:	soft
Address:	4A988h-4A98Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_98_B
Reset:	soft
Address:	4A98Ch-4A98Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_99_B
Reset:	soft
Address:	4A990h-4A993h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_100_B
Reset:	soft
Address:	4A994h-4A997h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_101_B
Reset:	soft

Address:	4A998h-4A99Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_102_B
Reset:	soft
Address:	4A99Ch-4A99Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_103_B
Reset:	soft
Address:	4A9A0h-4A9A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_104_B
Reset:	soft
Address:	4A9A4h-4A9A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_105_B
Reset:	soft
Address:	4A9A8h-4A9ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_106_B
Reset:	soft
Address:	4A9ACh-4A9AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_107_B
Reset:	soft
Address:	4A9B0h-4A9B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_108_B
Reset:	soft
Address:	4A9B4h-4A9B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_109_B
Reset:	soft
Address:	4A9B8h-4A9BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_110_B
Reset:	soft

Address:	4A9BCh-4A9BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_111_B
Reset:	soft
Address:	4A9C0h-4A9C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_112_B
Reset:	soft
Address:	4A9C4h-4A9C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_113_B
Reset:	soft
Address:	4A9C8h-4A9CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_114_B
Reset:	soft
Address:	4A9CCh-4A9CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_115_B
Reset:	soft
Address:	4A9D0h-4A9D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_116_B
Reset:	soft
Address:	4A9D4h-4A9D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_117_B
Reset:	soft
Address:	4A9D8h-4A9DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_118_B
Reset:	soft
Address:	4A9DCh-4A9DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_119_B
Reset:	soft

Address:	4A9E0h-4A9E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_120_B
Reset:	soft
Address:	4A9E4h-4A9E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_121_B
Reset:	soft
Address:	4A9E8h-4A9EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_122_B
Reset:	soft
Address:	4A9ECh-4A9EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_123_B
Reset:	soft
Address:	4A9F0h-4A9F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_124_B
Reset:	soft
Address:	4A9F4h-4A9F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_125_B
Reset:	soft
Address:	4A9F8h-4A9FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_126_B
Reset:	soft
Address:	4A9FCh-4A9FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_127_B
Reset:	soft
Address:	4AA00h-4AA03h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_128_B
Reset:	soft

Address:	4AA04h-4AA07h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_129_B
Reset:	soft
Address:	4AA08h-4AA0Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_130_B
Reset:	soft
Address:	4AA0Ch-4AA0Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_131_B
Reset:	soft
Address:	4AA10h-4AA13h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_132_B
Reset:	soft
Address:	4AA14h-4AA17h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_133_B
Reset:	soft
Address:	4AA18h-4AA1Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_134_B
Reset:	soft
Address:	4AA1Ch-4AA1Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_135_B
Reset:	soft
Address:	4AA20h-4AA23h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_136_B
Reset:	soft
Address:	4AA24h-4AA27h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_137_B
Reset:	soft

Address:	4AA28h-4AA2Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_138_B
Reset:	soft
Address:	4AA2Ch-4AA2Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_139_B
Reset:	soft
Address:	4AA30h-4AA33h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_140_B
Reset:	soft
Address:	4AA34h-4AA37h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_141_B
Reset:	soft
Address:	4AA38h-4AA3Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_142_B
Reset:	soft
Address:	4AA3Ch-4AA3Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_143_B
Reset:	soft
Address:	4AA40h-4AA43h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_144_B
Reset:	soft
Address:	4AA44h-4AA47h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_145_B
Reset:	soft
Address:	4AA48h-4AA4Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_146_B
Reset:	soft

Address:	4AA4Ch-4AA4Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_147_B
Reset:	soft
Address:	4AA50h-4AA53h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_148_B
Reset:	soft
Address:	4AA54h-4AA57h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_149_B
Reset:	soft
Address:	4AA58h-4AA5Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_150_B
Reset:	soft
Address:	4AA5Ch-4AA5Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_151_B
Reset:	soft
Address:	4AA60h-4AA63h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_152_B
Reset:	soft
Address:	4AA64h-4AA67h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_153_B
Reset:	soft
Address:	4AA68h-4AA6Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_154_B
Reset:	soft
Address:	4AA6Ch-4AA6Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_155_B
Reset:	soft

Address:	4AA70h-4AA73h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_156_B
Reset:	soft
Address:	4AA74h-4AA77h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_157_B
Reset:	soft
Address:	4AA78h-4AA7Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_158_B
Reset:	soft
Address:	4AA7Ch-4AA7Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_159_B
Reset:	soft
Address:	4AA80h-4AA83h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_160_B
Reset:	soft
Address:	4AA84h-4AA87h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_161_B
Reset:	soft
Address:	4AA88h-4AA8Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_162_B
Reset:	soft
Address:	4AA8Ch-4AA8Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_163_B
Reset:	soft
Address:	4AA90h-4AA93h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_164_B
Reset:	soft

Address:	4AA94h-4AA97h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_165_B
Reset:	soft
Address:	4AA98h-4AA9Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_166_B
Reset:	soft
Address:	4AA9Ch-4AA9Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_167_B
Reset:	soft
Address:	4AAA0h-4AAA3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_168_B
Reset:	soft
Address:	4AAA4h-4AAA7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_169_B
Reset:	soft
Address:	4AAA8h-4AAABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_170_B
Reset:	soft
Address:	4AAACh-4AAAFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_171_B
Reset:	soft
Address:	4AAB0h-4AAB3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_172_B
Reset:	soft
Address:	4AAB4h-4AAB7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_173_B
Reset:	soft

Address:	4AAB8h-4AABBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_174_B
Reset:	soft
Address:	4AABCh-4AABFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_175_B
Reset:	soft
Address:	4AAC0h-4AAC3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_176_B
Reset:	soft
Address:	4AAC4h-4AAC7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_177_B
Reset:	soft
Address:	4AAC8h-4AACBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_178_B
Reset:	soft
Address:	4AACCh-4AACFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_179_B
Reset:	soft
Address:	4AAD0h-4AAD3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_180_B
Reset:	soft
Address:	4AAD4h-4AAD7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_181_B
Reset:	soft
Address:	4AAD8h-4AADBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_182_B
Reset:	soft

Address:	4AADCh-4AADFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_183_B
Reset:	soft
Address:	4AAE0h-4AAE3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_184_B
Reset:	soft
Address:	4AAE4h-4AAE7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_185_B
Reset:	soft
Address:	4AAE8h-4AAEBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_186_B
Reset:	soft
Address:	4AAECh-4AAEFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_187_B
Reset:	soft
Address:	4AAF0h-4AAF3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_188_B
Reset:	soft
Address:	4AAF4h-4AAF7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_189_B
Reset:	soft
Address:	4AAF8h-4AAFBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_190_B
Reset:	soft
Address:	4AAFCh-4AAFFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_191_B
Reset:	soft

Address:	4AB00h-4AB03h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_192_B
Reset:	soft
Address:	4AB04h-4AB07h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_193_B
Reset:	soft
Address:	4AB08h-4AB0Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_194_B
Reset:	soft
Address:	4AB0Ch-4AB0Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_195_B
Reset:	soft
Address:	4AB10h-4AB13h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_196_B
Reset:	soft
Address:	4AB14h-4AB17h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_197_B
Reset:	soft
Address:	4AB18h-4AB1Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_198_B
Reset:	soft
Address:	4AB1Ch-4AB1Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_199_B
Reset:	soft
Address:	4AB20h-4AB23h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_200_B
Reset:	soft

Address:	4AB24h-4AB27h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_201_B
Reset:	soft
Address:	4AB28h-4AB2Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_202_B
Reset:	soft
Address:	4AB2Ch-4AB2Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_203_B
Reset:	soft
Address:	4AB30h-4AB33h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_204_B
Reset:	soft
Address:	4AB34h-4AB37h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_205_B
Reset:	soft
Address:	4AB38h-4AB3Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_206_B
Reset:	soft
Address:	4AB3Ch-4AB3Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_207_B
Reset:	soft
Address:	4AB40h-4AB43h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_208_B
Reset:	soft
Address:	4AB44h-4AB47h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_209_B
Reset:	soft

Address:	4AB48h-4AB4Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_210_B
Reset:	soft
Address:	4AB4Ch-4AB4Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_211_B
Reset:	soft
Address:	4AB50h-4AB53h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_212_B
Reset:	soft
Address:	4AB54h-4AB57h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_213_B
Reset:	soft
Address:	4AB58h-4AB5Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_214_B
Reset:	soft
Address:	4AB5Ch-4AB5Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_215_B
Reset:	soft
Address:	4AB60h-4AB63h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_216_B
Reset:	soft
Address:	4AB64h-4AB67h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_217_B
Reset:	soft
Address:	4AB68h-4AB6Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_218_B
Reset:	soft

Address:	4AB6Ch-4AB6Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_219_B
Reset:	soft
Address:	4AB70h-4AB73h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_220_B
Reset:	soft
Address:	4AB74h-4AB77h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_221_B
Reset:	soft
Address:	4AB78h-4AB7Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_222_B
Reset:	soft
Address:	4AB7Ch-4AB7Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_223_B
Reset:	soft
Address:	4AB80h-4AB83h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_224_B
Reset:	soft
Address:	4AB84h-4AB87h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_225_B
Reset:	soft
Address:	4AB88h-4AB8Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_226_B
Reset:	soft
Address:	4AB8Ch-4AB8Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_227_B
Reset:	soft

Address:	4AB90h-4AB93h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_228_B
Reset:	soft
Address:	4AB94h-4AB97h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_229_B
Reset:	soft
Address:	4AB98h-4AB9Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_230_B
Reset:	soft
Address:	4AB9Ch-4AB9Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_231_B
Reset:	soft
Address:	4ABA0h-4ABA3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_232_B
Reset:	soft
Address:	4ABA4h-4ABA7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_233_B
Reset:	soft
Address:	4ABA8h-4ABABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_234_B
Reset:	soft
Address:	4ABACh-4ABAFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_235_B
Reset:	soft
Address:	4ABB0h-4ABB3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_236_B
Reset:	soft

Address:	4ABB4h-4ABB7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_237_B
Reset:	soft
Address:	4ABB8h-4ABBBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_238_B
Reset:	soft
Address:	4ABBCh-4ABBFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_239_B
Reset:	soft
Address:	4ABC0h-4ABC3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_240_B
Reset:	soft
Address:	4ABC4h-4ABC7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_241_B
Reset:	soft
Address:	4ABC8h-4ABCBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_242_B
Reset:	soft
Address:	4ABCCh-4ABCFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_243_B
Reset:	soft
Address:	4ABD0h-4ABD3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_244_B
Reset:	soft
Address:	4ABD4h-4ABD7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_245_B
Reset:	soft

Address:	4ABD8h-4ABDBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_246_B
Reset:	soft
Address:	4ABDCh-4ABDFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_247_B
Reset:	soft
Address:	4ABE0h-4ABE3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_248_B
Reset:	soft
Address:	4ABE4h-4ABE7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_249_B
Reset:	soft
Address:	4ABE8h-4ABEBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_250_B
Reset:	soft
Address:	4ABECh-4ABEFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_251_B
Reset:	soft
Address:	4ABF0h-4ABF3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_252_B
Reset:	soft
Address:	4ABF4h-4ABF7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_253_B
Reset:	soft
Address:	4ABF8h-4ABFBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_254_B
Reset:	soft

Address:	4ABFCh-4ABFFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_255_B
Reset:	soft
Address:	4B000h-4B003h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_0_C
Reset:	soft
Address:	4B004h-4B007h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_1_C
Reset:	soft
Address:	4B008h-4B00Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_2_C
Reset:	soft
Address:	4B00Ch-4B00Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_3_C
Reset:	soft
Address:	4B010h-4B013h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_4_C
Reset:	soft
Address:	4B014h-4B017h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_5_C
Reset:	soft
Address:	4B018h-4B01Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_6_C
Reset:	soft
Address:	4B01Ch-4B01Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_7_C
Reset:	soft

Address:	4B020h-4B023h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_8_C
Reset:	soft
Address:	4B024h-4B027h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_9_C
Reset:	soft
Address:	4B028h-4B02Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_10_C
Reset:	soft
Address:	4B02Ch-4B02Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_11_C
Reset:	soft
Address:	4B030h-4B033h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_12_C
Reset:	soft
Address:	4B034h-4B037h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_13_C
Reset:	soft
Address:	4B038h-4B03Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_14_C
Reset:	soft
Address:	4B03Ch-4B03Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_15_C
Reset:	soft
Address:	4B040h-4B043h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_16_C
Reset:	soft

Address:	4B044h-4B047h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_17_C
Reset:	soft
Address:	4B048h-4B04Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_18_C
Reset:	soft
Address:	4B04Ch-4B04Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_19_C
Reset:	soft
Address:	4B050h-4B053h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_20_C
Reset:	soft
Address:	4B054h-4B057h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_21_C
Reset:	soft
Address:	4B058h-4B05Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_22_C
Reset:	soft
Address:	4B05Ch-4B05Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_23_C
Reset:	soft
Address:	4B060h-4B063h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_24_C
Reset:	soft
Address:	4B064h-4B067h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_25_C
Reset:	soft

Address:	4B068h-4B06Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_26_C
Reset:	soft
Address:	4B06Ch-4B06Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_27_C
Reset:	soft
Address:	4B070h-4B073h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_28_C
Reset:	soft
Address:	4B074h-4B077h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_29_C
Reset:	soft
Address:	4B078h-4B07Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_30_C
Reset:	soft
Address:	4B07Ch-4B07Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_31_C
Reset:	soft
Address:	4B080h-4B083h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_32_C
Reset:	soft
Address:	4B084h-4B087h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_33_C
Reset:	soft
Address:	4B088h-4B08Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_34_C
Reset:	soft

Address:	4B08Ch-4B08Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_35_C
Reset:	soft
Address:	4B090h-4B093h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_36_C
Reset:	soft
Address:	4B094h-4B097h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_37_C
Reset:	soft
Address:	4B098h-4B09Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_38_C
Reset:	soft
Address:	4B09Ch-4B09Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_39_C
Reset:	soft
Address:	4B0A0h-4B0A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_40_C
Reset:	soft
Address:	4B0A4h-4B0A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_41_C
Reset:	soft
Address:	4B0A8h-4B0ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_42_C
Reset:	soft
Address:	4B0ACh-4B0AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_43_C
Reset:	soft

Address:	4B0B0h-4B0B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_44_C
Reset:	soft
Address:	4B0B4h-4B0B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_45_C
Reset:	soft
Address:	4B0B8h-4B0BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_46_C
Reset:	soft
Address:	4B0BCh-4B0BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_47_C
Reset:	soft
Address:	4B0C0h-4B0C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_48_C
Reset:	soft
Address:	4B0C4h-4B0C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_49_C
Reset:	soft
Address:	4B0C8h-4B0CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_50_C
Reset:	soft
Address:	4B0CCh-4B0CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_51_C
Reset:	soft
Address:	4B0D0h-4B0D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_52_C
Reset:	soft

Address:	4B0D4h-4B0D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_53_C
Reset:	soft
Address:	4B0D8h-4B0DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_54_C
Reset:	soft
Address:	4B0DCh-4B0DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_55_C
Reset:	soft
Address:	4B0E0h-4B0E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_56_C
Reset:	soft
Address:	4B0E4h-4B0E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_57_C
Reset:	soft
Address:	4B0E8h-4B0EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_58_C
Reset:	soft
Address:	4B0ECh-4B0EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_59_C
Reset:	soft
Address:	4B0F0h-4B0F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_60_C
Reset:	soft
Address:	4B0F4h-4B0F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_61_C
Reset:	soft

Address:	4B0F8h-4B0FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_62_C
Reset:	soft
Address:	4B0FCh-4B0FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_63_C
Reset:	soft
Address:	4B100h-4B103h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_64_C
Reset:	soft
Address:	4B104h-4B107h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_65_C
Reset:	soft
Address:	4B108h-4B10Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_66_C
Reset:	soft
Address:	4B10Ch-4B10Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_67_C
Reset:	soft
Address:	4B110h-4B113h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_68_C
Reset:	soft
Address:	4B114h-4B117h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_69_C
Reset:	soft
Address:	4B118h-4B11Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_70_C
Reset:	soft

Address:	4B11Ch-4B11Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_71_C
Reset:	soft
Address:	4B120h-4B123h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_72_C
Reset:	soft
Address:	4B124h-4B127h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_73_C
Reset:	soft
Address:	4B128h-4B12Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_74_C
Reset:	soft
Address:	4B12Ch-4B12Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_75_C
Reset:	soft
Address:	4B130h-4B133h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_76_C
Reset:	soft
Address:	4B134h-4B137h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_77_C
Reset:	soft
Address:	4B138h-4B13Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_78_C
Reset:	soft
Address:	4B13Ch-4B13Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_79_C
Reset:	soft

Address:	4B140h-4B143h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_80_C
Reset:	soft
Address:	4B144h-4B147h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_81_C
Reset:	soft
Address:	4B148h-4B14Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_82_C
Reset:	soft
Address:	4B14Ch-4B14Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_83_C
Reset:	soft
Address:	4B150h-4B153h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_84_C
Reset:	soft
Address:	4B154h-4B157h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_85_C
Reset:	soft
Address:	4B158h-4B15Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_86_C
Reset:	soft
Address:	4B15Ch-4B15Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_87_C
Reset:	soft
Address:	4B160h-4B163h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_88_C
Reset:	soft

Address:	4B164h-4B167h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_89_C
Reset:	soft
Address:	4B168h-4B16Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_90_C
Reset:	soft
Address:	4B16Ch-4B16Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_91_C
Reset:	soft
Address:	4B170h-4B173h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_92_C
Reset:	soft
Address:	4B174h-4B177h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_93_C
Reset:	soft
Address:	4B178h-4B17Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_94_C
Reset:	soft
Address:	4B17Ch-4B17Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_95_C
Reset:	soft
Address:	4B180h-4B183h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_96_C
Reset:	soft
Address:	4B184h-4B187h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_97_C
Reset:	soft

Address:	4B188h-4B18Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_98_C
Reset:	soft
Address:	4B18Ch-4B18Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_99_C
Reset:	soft
Address:	4B190h-4B193h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_100_C
Reset:	soft
Address:	4B194h-4B197h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_101_C
Reset:	soft
Address:	4B198h-4B19Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_102_C
Reset:	soft
Address:	4B19Ch-4B19Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_103_C
Reset:	soft
Address:	4B1A0h-4B1A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_104_C
Reset:	soft
Address:	4B1A4h-4B1A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_105_C
Reset:	soft
Address:	4B1A8h-4B1ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_106_C
Reset:	soft

Address:	4B1ACh-4B1AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_107_C
Reset:	soft
Address:	4B1B0h-4B1B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_108_C
Reset:	soft
Address:	4B1B4h-4B1B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_109_C
Reset:	soft
Address:	4B1B8h-4B1BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_110_C
Reset:	soft
Address:	4B1BCh-4B1BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_111_C
Reset:	soft
Address:	4B1C0h-4B1C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_112_C
Reset:	soft
Address:	4B1C4h-4B1C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_113_C
Reset:	soft
Address:	4B1C8h-4B1CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_114_C
Reset:	soft
Address:	4B1CCh-4B1CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_115_C
Reset:	soft

Address:	4B1D0h-4B1D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_116_C
Reset:	soft
Address:	4B1D4h-4B1D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_117_C
Reset:	soft
Address:	4B1D8h-4B1DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_118_C
Reset:	soft
Address:	4B1DCh-4B1DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_119_C
Reset:	soft
Address:	4B1E0h-4B1E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_120_C
Reset:	soft
Address:	4B1E4h-4B1E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_121_C
Reset:	soft
Address:	4B1E8h-4B1EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_122_C
Reset:	soft
Address:	4B1ECh-4B1EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_123_C
Reset:	soft
Address:	4B1F0h-4B1F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_124_C
Reset:	soft

Address:	4B1F4h-4B1F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_125_C
Reset:	soft
Address:	4B1F8h-4B1FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_126_C
Reset:	soft
Address:	4B1FCh-4B1FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_127_C
Reset:	soft
Address:	4B200h-4B203h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_128_C
Reset:	soft
Address:	4B204h-4B207h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_129_C
Reset:	soft
Address:	4B208h-4B20Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_130_C
Reset:	soft
Address:	4B20Ch-4B20Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_131_C
Reset:	soft
Address:	4B210h-4B213h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_132_C
Reset:	soft
Address:	4B214h-4B217h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_133_C
Reset:	soft

Address:	4B218h-4B21Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_134_C
Reset:	soft
Address:	4B21Ch-4B21Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_135_C
Reset:	soft
Address:	4B220h-4B223h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_136_C
Reset:	soft
Address:	4B224h-4B227h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_137_C
Reset:	soft
Address:	4B228h-4B22Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_138_C
Reset:	soft
Address:	4B22Ch-4B22Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_139_C
Reset:	soft
Address:	4B230h-4B233h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_140_C
Reset:	soft
Address:	4B234h-4B237h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_141_C
Reset:	soft
Address:	4B238h-4B23Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_142_C
Reset:	soft

Address:	4B23Ch-4B23Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_143_C
Reset:	soft
Address:	4B240h-4B243h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_144_C
Reset:	soft
Address:	4B244h-4B247h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_145_C
Reset:	soft
Address:	4B248h-4B24Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_146_C
Reset:	soft
Address:	4B24Ch-4B24Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_147_C
Reset:	soft
Address:	4B250h-4B253h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_148_C
Reset:	soft
Address:	4B254h-4B257h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_149_C
Reset:	soft
Address:	4B258h-4B25Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_150_C
Reset:	soft
Address:	4B25Ch-4B25Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_151_C
Reset:	soft

Address:	4B260h-4B263h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_152_C
Reset:	soft
Address:	4B264h-4B267h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_153_C
Reset:	soft
Address:	4B268h-4B26Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_154_C
Reset:	soft
Address:	4B26Ch-4B26Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_155_C
Reset:	soft
Address:	4B270h-4B273h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_156_C
Reset:	soft
Address:	4B274h-4B277h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_157_C
Reset:	soft
Address:	4B278h-4B27Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_158_C
Reset:	soft
Address:	4B27Ch-4B27Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_159_C
Reset:	soft
Address:	4B280h-4B283h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_160_C
Reset:	soft

Address:	4B284h-4B287h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_161_C
Reset:	soft
Address:	4B288h-4B28Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_162_C
Reset:	soft
Address:	4B28Ch-4B28Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_163_C
Reset:	soft
Address:	4B290h-4B293h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_164_C
Reset:	soft
Address:	4B294h-4B297h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_165_C
Reset:	soft
Address:	4B298h-4B29Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_166_C
Reset:	soft
Address:	4B29Ch-4B29Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_167_C
Reset:	soft
Address:	4B2A0h-4B2A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_168_C
Reset:	soft
Address:	4B2A4h-4B2A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_169_C
Reset:	soft

Address:	4B2A8h-4B2ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_170_C
Reset:	soft
Address:	4B2ACh-4B2AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_171_C
Reset:	soft
Address:	4B2B0h-4B2B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_172_C
Reset:	soft
Address:	4B2B4h-4B2B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_173_C
Reset:	soft
Address:	4B2B8h-4B2BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_174_C
Reset:	soft
Address:	4B2BCh-4B2BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_175_C
Reset:	soft
Address:	4B2C0h-4B2C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_176_C
Reset:	soft
Address:	4B2C4h-4B2C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_177_C
Reset:	soft
Address:	4B2C8h-4B2CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_178_C
Reset:	soft

Address:	4B2CCh-4B2CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_179_C
Reset:	soft
Address:	4B2D0h-4B2D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_180_C
Reset:	soft
Address:	4B2D4h-4B2D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_181_C
Reset:	soft
Address:	4B2D8h-4B2DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_182_C
Reset:	soft
Address:	4B2DCh-4B2DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_183_C
Reset:	soft
Address:	4B2E0h-4B2E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_184_C
Reset:	soft
Address:	4B2E4h-4B2E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_185_C
Reset:	soft
Address:	4B2E8h-4B2EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_186_C
Reset:	soft
Address:	4B2ECh-4B2EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_187_C
Reset:	soft

Address:	4B2F0h-4B2F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_188_C
Reset:	soft
Address:	4B2F4h-4B2F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_189_C
Reset:	soft
Address:	4B2F8h-4B2FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_190_C
Reset:	soft
Address:	4B2FCh-4B2FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_191_C
Reset:	soft
Address:	4B300h-4B303h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_192_C
Reset:	soft
Address:	4B304h-4B307h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_193_C
Reset:	soft
Address:	4B308h-4B30Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_194_C
Reset:	soft
Address:	4B30Ch-4B30Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_195_C
Reset:	soft
Address:	4B310h-4B313h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_196_C
Reset:	soft

Address:	4B314h-4B317h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_197_C
Reset:	soft
Address:	4B318h-4B31Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_198_C
Reset:	soft
Address:	4B31Ch-4B31Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_199_C
Reset:	soft
Address:	4B320h-4B323h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_200_C
Reset:	soft
Address:	4B324h-4B327h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_201_C
Reset:	soft
Address:	4B328h-4B32Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_202_C
Reset:	soft
Address:	4B32Ch-4B32Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_203_C
Reset:	soft
Address:	4B330h-4B333h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_204_C
Reset:	soft
Address:	4B334h-4B337h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_205_C
Reset:	soft

Address:	4B338h-4B33Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_206_C
Reset:	soft
Address:	4B33Ch-4B33Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_207_C
Reset:	soft
Address:	4B340h-4B343h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_208_C
Reset:	soft
Address:	4B344h-4B347h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_209_C
Reset:	soft
Address:	4B348h-4B34Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_210_C
Reset:	soft
Address:	4B34Ch-4B34Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_211_C
Reset:	soft
Address:	4B350h-4B353h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_212_C
Reset:	soft
Address:	4B354h-4B357h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_213_C
Reset:	soft
Address:	4B358h-4B35Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_214_C
Reset:	soft

Address:	4B35Ch-4B35Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_215_C
Reset:	soft
Address:	4B360h-4B363h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_216_C
Reset:	soft
Address:	4B364h-4B367h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_217_C
Reset:	soft
Address:	4B368h-4B36Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_218_C
Reset:	soft
Address:	4B36Ch-4B36Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_219_C
Reset:	soft
Address:	4B370h-4B373h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_220_C
Reset:	soft
Address:	4B374h-4B377h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_221_C
Reset:	soft
Address:	4B378h-4B37Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_222_C
Reset:	soft
Address:	4B37Ch-4B37Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_223_C
Reset:	soft

Address:	4B380h-4B383h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_224_C
Reset:	soft
Address:	4B384h-4B387h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_225_C
Reset:	soft
Address:	4B388h-4B38Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_226_C
Reset:	soft
Address:	4B38Ch-4B38Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_227_C
Reset:	soft
Address:	4B390h-4B393h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_228_C
Reset:	soft
Address:	4B394h-4B397h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_229_C
Reset:	soft
Address:	4B398h-4B39Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_230_C
Reset:	soft
Address:	4B39Ch-4B39Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_231_C
Reset:	soft
Address:	4B3A0h-4B3A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_232_C
Reset:	soft

Address:	4B3A4h-4B3A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_233_C
Reset:	soft
Address:	4B3A8h-4B3ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_234_C
Reset:	soft
Address:	4B3ACh-4B3AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_235_C
Reset:	soft
Address:	4B3B0h-4B3B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_236_C
Reset:	soft
Address:	4B3B4h-4B3B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_237_C
Reset:	soft
Address:	4B3B8h-4B3BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_238_C
Reset:	soft
Address:	4B3BCh-4B3BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_239_C
Reset:	soft
Address:	4B3C0h-4B3C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_240_C
Reset:	soft
Address:	4B3C4h-4B3C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_241_C
Reset:	soft

Address:	4B3C8h-4B3CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_242_C
Reset:	soft
Address:	4B3CCh-4B3CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_243_C
Reset:	soft
Address:	4B3D0h-4B3D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_244_C
Reset:	soft
Address:	4B3D4h-4B3D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_245_C
Reset:	soft
Address:	4B3D8h-4B3DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_246_C
Reset:	soft
Address:	4B3DCh-4B3DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_247_C
Reset:	soft
Address:	4B3E0h-4B3E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_248_C
Reset:	soft
Address:	4B3E4h-4B3E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_249_C
Reset:	soft
Address:	4B3E8h-4B3EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_250_C
Reset:	soft

Address:	4B3ECh-4B3EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_251_C
Reset:	soft
Address:	4B3F0h-4B3F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_252_C
Reset:	soft
Address:	4B3F4h-4B3F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_253_C
Reset:	soft
Address:	4B3F8h-4B3FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_254_C
Reset:	soft
Address:	4B3FCh-4B3FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_255_C
Reset:	soft
Address:	4B800h-4B803h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_0_D
Reset:	soft
Address:	4B804h-4B807h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_1_D
Reset:	soft
Address:	4B808h-4B80Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_2_D
Reset:	soft
Address:	4B80Ch-4B80Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_3_D
Reset:	soft

Address:	4B810h-4B813h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_4_D
Reset:	soft
Address:	4B814h-4B817h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_5_D
Reset:	soft
Address:	4B818h-4B81Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_6_D
Reset:	soft
Address:	4B81Ch-4B81Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_7_D
Reset:	soft
Address:	4B820h-4B823h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_8_D
Reset:	soft
Address:	4B824h-4B827h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_9_D
Reset:	soft
Address:	4B828h-4B82Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_10_D
Reset:	soft
Address:	4B82Ch-4B82Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_11_D
Reset:	soft
Address:	4B830h-4B833h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_12_D
Reset:	soft

Address:	4B834h-4B837h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_13_D
Reset:	soft
Address:	4B838h-4B83Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_14_D
Reset:	soft
Address:	4B83Ch-4B83Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_15_D
Reset:	soft
Address:	4B840h-4B843h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_16_D
Reset:	soft
Address:	4B844h-4B847h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_17_D
Reset:	soft
Address:	4B848h-4B84Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_18_D
Reset:	soft
Address:	4B84Ch-4B84Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_19_D
Reset:	soft
Address:	4B850h-4B853h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_20_D
Reset:	soft
Address:	4B854h-4B857h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_21_D
Reset:	soft

Address:	4B858h-4B85Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_22_D
Reset:	soft
Address:	4B85Ch-4B85Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_23_D
Reset:	soft
Address:	4B860h-4B863h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_24_D
Reset:	soft
Address:	4B864h-4B867h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_25_D
Reset:	soft
Address:	4B868h-4B86Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_26_D
Reset:	soft
Address:	4B86Ch-4B86Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_27_D
Reset:	soft
Address:	4B870h-4B873h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_28_D
Reset:	soft
Address:	4B874h-4B877h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_29_D
Reset:	soft
Address:	4B878h-4B87Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_30_D
Reset:	soft

Address:	4B87Ch-4B87Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_31_D
Reset:	soft
Address:	4B880h-4B883h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_32_D
Reset:	soft
Address:	4B884h-4B887h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_33_D
Reset:	soft
Address:	4B888h-4B88Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_34_D
Reset:	soft
Address:	4B88Ch-4B88Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_35_D
Reset:	soft
Address:	4B890h-4B893h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_36_D
Reset:	soft
Address:	4B894h-4B897h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_37_D
Reset:	soft
Address:	4B898h-4B89Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_38_D
Reset:	soft
Address:	4B89Ch-4B89Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_39_D
Reset:	soft

Address:	4B8A0h-4B8A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_40_D
Reset:	soft
Address:	4B8A4h-4B8A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_41_D
Reset:	soft
Address:	4B8A8h-4B8ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_42_D
Reset:	soft
Address:	4B8ACh-4B8AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_43_D
Reset:	soft
Address:	4B8B0h-4B8B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_44_D
Reset:	soft
Address:	4B8B4h-4B8B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_45_D
Reset:	soft
Address:	4B8B8h-4B8BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_46_D
Reset:	soft
Address:	4B8BCh-4B8BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_47_D
Reset:	soft
Address:	4B8C0h-4B8C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_48_D
Reset:	soft

Address:	4B8C4h-4B8C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_49_D
Reset:	soft
Address:	4B8C8h-4B8CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_50_D
Reset:	soft
Address:	4B8CCh-4B8CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_51_D
Reset:	soft
Address:	4B8D0h-4B8D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_52_D
Reset:	soft
Address:	4B8D4h-4B8D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_53_D
Reset:	soft
Address:	4B8D8h-4B8DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_54_D
Reset:	soft
Address:	4B8DCh-4B8DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_55_D
Reset:	soft
Address:	4B8E0h-4B8E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_56_D
Reset:	soft
Address:	4B8E4h-4B8E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_57_D
Reset:	soft

Address:	4B8E8h-4B8EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_58_D
Reset:	soft
Address:	4B8ECh-4B8EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_59_D
Reset:	soft
Address:	4B8F0h-4B8F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_60_D
Reset:	soft
Address:	4B8F4h-4B8F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_61_D
Reset:	soft
Address:	4B8F8h-4B8FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_62_D
Reset:	soft
Address:	4B8FCh-4B8FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_63_D
Reset:	soft
Address:	4B900h-4B903h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_64_D
Reset:	soft
Address:	4B904h-4B907h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_65_D
Reset:	soft
Address:	4B908h-4B90Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_66_D
Reset:	soft

Address:	4B90Ch-4B90Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_67_D
Reset:	soft
Address:	4B910h-4B913h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_68_D
Reset:	soft
Address:	4B914h-4B917h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_69_D
Reset:	soft
Address:	4B918h-4B91Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_70_D
Reset:	soft
Address:	4B91Ch-4B91Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_71_D
Reset:	soft
Address:	4B920h-4B923h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_72_D
Reset:	soft
Address:	4B924h-4B927h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_73_D
Reset:	soft
Address:	4B928h-4B92Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_74_D
Reset:	soft
Address:	4B92Ch-4B92Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_75_D
Reset:	soft

Address:	4B930h-4B933h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_76_D
Reset:	soft
Address:	4B934h-4B937h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_77_D
Reset:	soft
Address:	4B938h-4B93Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_78_D
Reset:	soft
Address:	4B93Ch-4B93Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_79_D
Reset:	soft
Address:	4B940h-4B943h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_80_D
Reset:	soft
Address:	4B944h-4B947h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_81_D
Reset:	soft
Address:	4B948h-4B94Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_82_D
Reset:	soft
Address:	4B94Ch-4B94Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_83_D
Reset:	soft
Address:	4B950h-4B953h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_84_D
Reset:	soft

Address:	4B954h-4B957h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_85_D
Reset:	soft
Address:	4B958h-4B95Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_86_D
Reset:	soft
Address:	4B95Ch-4B95Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_87_D
Reset:	soft
Address:	4B960h-4B963h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_88_D
Reset:	soft
Address:	4B964h-4B967h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_89_D
Reset:	soft
Address:	4B968h-4B96Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_90_D
Reset:	soft
Address:	4B96Ch-4B96Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_91_D
Reset:	soft
Address:	4B970h-4B973h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_92_D
Reset:	soft
Address:	4B974h-4B977h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_93_D
Reset:	soft

Address:	4B978h-4B97Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_94_D
Reset:	soft
Address:	4B97Ch-4B97Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_95_D
Reset:	soft
Address:	4B980h-4B983h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_96_D
Reset:	soft
Address:	4B984h-4B987h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_97_D
Reset:	soft
Address:	4B988h-4B98Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_98_D
Reset:	soft
Address:	4B98Ch-4B98Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_99_D
Reset:	soft
Address:	4B990h-4B993h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_100_D
Reset:	soft
Address:	4B994h-4B997h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_101_D
Reset:	soft
Address:	4B998h-4B99Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_102_D
Reset:	soft

Address:	4B99Ch-4B99Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_103_D
Reset:	soft
Address:	4B9A0h-4B9A3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_104_D
Reset:	soft
Address:	4B9A4h-4B9A7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_105_D
Reset:	soft
Address:	4B9A8h-4B9ABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_106_D
Reset:	soft
Address:	4B9ACh-4B9AFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_107_D
Reset:	soft
Address:	4B9B0h-4B9B3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_108_D
Reset:	soft
Address:	4B9B4h-4B9B7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_109_D
Reset:	soft
Address:	4B9B8h-4B9BBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_110_D
Reset:	soft
Address:	4B9BCh-4B9BFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_111_D
Reset:	soft

Address:	4B9C0h-4B9C3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_112_D
Reset:	soft
Address:	4B9C4h-4B9C7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_113_D
Reset:	soft
Address:	4B9C8h-4B9CBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_114_D
Reset:	soft
Address:	4B9CCh-4B9CFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_115_D
Reset:	soft
Address:	4B9D0h-4B9D3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_116_D
Reset:	soft
Address:	4B9D4h-4B9D7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_117_D
Reset:	soft
Address:	4B9D8h-4B9DBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_118_D
Reset:	soft
Address:	4B9DCh-4B9DFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_119_D
Reset:	soft
Address:	4B9E0h-4B9E3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_120_D
Reset:	soft

Address:	4B9E4h-4B9E7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_121_D
Reset:	soft
Address:	4B9E8h-4B9EBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_122_D
Reset:	soft
Address:	4B9ECh-4B9EFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_123_D
Reset:	soft
Address:	4B9F0h-4B9F3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_124_D
Reset:	soft
Address:	4B9F4h-4B9F7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_125_D
Reset:	soft
Address:	4B9F8h-4B9FBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_126_D
Reset:	soft
Address:	4B9FCh-4B9FFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_127_D
Reset:	soft
Address:	4BA00h-4BA03h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_128_D
Reset:	soft
Address:	4BA04h-4BA07h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_129_D
Reset:	soft

Address:	4BA08h-4BA0Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_130_D
Reset:	soft
Address:	4BA0Ch-4BA0Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_131_D
Reset:	soft
Address:	4BA10h-4BA13h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_132_D
Reset:	soft
Address:	4BA14h-4BA17h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_133_D
Reset:	soft
Address:	4BA18h-4BA1Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_134_D
Reset:	soft
Address:	4BA1Ch-4BA1Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_135_D
Reset:	soft
Address:	4BA20h-4BA23h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_136_D
Reset:	soft
Address:	4BA24h-4BA27h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_137_D
Reset:	soft
Address:	4BA28h-4BA2Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_138_D
Reset:	soft

Address:	4BA2Ch-4BA2Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_139_D
Reset:	soft
Address:	4BA30h-4BA33h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_140_D
Reset:	soft
Address:	4BA34h-4BA37h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_141_D
Reset:	soft
Address:	4BA38h-4BA3Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_142_D
Reset:	soft
Address:	4BA3Ch-4BA3Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_143_D
Reset:	soft
Address:	4BA40h-4BA43h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_144_D
Reset:	soft
Address:	4BA44h-4BA47h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_145_D
Reset:	soft
Address:	4BA48h-4BA4Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_146_D
Reset:	soft
Address:	4BA4Ch-4BA4Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_147_D
Reset:	soft

Address:	4BA50h-4BA53h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_148_D
Reset:	soft
Address:	4BA54h-4BA57h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_149_D
Reset:	soft
Address:	4BA58h-4BA5Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_150_D
Reset:	soft
Address:	4BA5Ch-4BA5Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_151_D
Reset:	soft
Address:	4BA60h-4BA63h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_152_D
Reset:	soft
Address:	4BA64h-4BA67h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_153_D
Reset:	soft
Address:	4BA68h-4BA6Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_154_D
Reset:	soft
Address:	4BA6Ch-4BA6Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_155_D
Reset:	soft
Address:	4BA70h-4BA73h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_156_D
Reset:	soft

Address:	4BA74h-4BA77h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_157_D
Reset:	soft
Address:	4BA78h-4BA7Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_158_D
Reset:	soft
Address:	4BA7Ch-4BA7Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_159_D
Reset:	soft
Address:	4BA80h-4BA83h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_160_D
Reset:	soft
Address:	4BA84h-4BA87h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_161_D
Reset:	soft
Address:	4BA88h-4BA8Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_162_D
Reset:	soft
Address:	4BA8Ch-4BA8Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_163_D
Reset:	soft
Address:	4BA90h-4BA93h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_164_D
Reset:	soft
Address:	4BA94h-4BA97h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_165_D
Reset:	soft

Address:	4BA98h-4BA9Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_166_D
Reset:	soft
Address:	4BA9Ch-4BA9Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_167_D
Reset:	soft
Address:	4BAA0h-4BAA3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_168_D
Reset:	soft
Address:	4BAA4h-4BAA7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_169_D
Reset:	soft
Address:	4BAA8h-4BAABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_170_D
Reset:	soft
Address:	4BAACh-4BAAFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_171_D
Reset:	soft
Address:	4BAB0h-4BAB3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_172_D
Reset:	soft
Address:	4BAB4h-4BAB7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_173_D
Reset:	soft
Address:	4BAB8h-4BABBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_174_D
Reset:	soft

Address:	4BABCh-4BABFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_175_D
Reset:	soft
Address:	4BAC0h-4BAC3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_176_D
Reset:	soft
Address:	4BAC4h-4BAC7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_177_D
Reset:	soft
Address:	4BAC8h-4BACBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_178_D
Reset:	soft
Address:	4BACCh-4BACFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_179_D
Reset:	soft
Address:	4BAD0h-4BAD3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_180_D
Reset:	soft
Address:	4BAD4h-4BAD7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_181_D
Reset:	soft
Address:	4BAD8h-4BADBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_182_D
Reset:	soft
Address:	4BADCh-4BADFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_183_D
Reset:	soft

Address:	4BAE0h-4BAE3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_184_D
Reset:	soft
Address:	4BAE4h-4BAE7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_185_D
Reset:	soft
Address:	4BAE8h-4BAEBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_186_D
Reset:	soft
Address:	4BAECh-4BAEFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_187_D
Reset:	soft
Address:	4BAF0h-4BAF3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_188_D
Reset:	soft
Address:	4BAF4h-4BAF7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_189_D
Reset:	soft
Address:	4BAF8h-4BAFBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_190_D
Reset:	soft
Address:	4BAFCh-4BAFFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_191_D
Reset:	soft
Address:	4BB00h-4BB03h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_192_D
Reset:	soft

Address:	4BB04h-4BB07h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_193_D
Reset:	soft
Address:	4BB08h-4BB0Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_194_D
Reset:	soft
Address:	4BB0Ch-4BB0Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_195_D
Reset:	soft
Address:	4BB10h-4BB13h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_196_D
Reset:	soft
Address:	4BB14h-4BB17h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_197_D
Reset:	soft
Address:	4BB18h-4BB1Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_198_D
Reset:	soft
Address:	4BB1Ch-4BB1Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_199_D
Reset:	soft
Address:	4BB20h-4BB23h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_200_D
Reset:	soft
Address:	4BB24h-4BB27h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_201_D
Reset:	soft

Address:	4BB28h-4BB2Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_202_D
Reset:	soft
Address:	4BB2Ch-4BB2Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_203_D
Reset:	soft
Address:	4BB30h-4BB33h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_204_D
Reset:	soft
Address:	4BB34h-4BB37h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_205_D
Reset:	soft
Address:	4BB38h-4BB3Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_206_D
Reset:	soft
Address:	4BB3Ch-4BB3Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_207_D
Reset:	soft
Address:	4BB40h-4BB43h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_208_D
Reset:	soft
Address:	4BB44h-4BB47h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_209_D
Reset:	soft
Address:	4BB48h-4BB4Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_210_D
Reset:	soft

Address:	4BB4Ch-4BB4Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_211_D
Reset:	soft
Address:	4BB50h-4BB53h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_212_D
Reset:	soft
Address:	4BB54h-4BB57h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_213_D
Reset:	soft
Address:	4BB58h-4BB5Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_214_D
Reset:	soft
Address:	4BB5Ch-4BB5Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_215_D
Reset:	soft
Address:	4BB60h-4BB63h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_216_D
Reset:	soft
Address:	4BB64h-4BB67h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_217_D
Reset:	soft
Address:	4BB68h-4BB6Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_218_D
Reset:	soft
Address:	4BB6Ch-4BB6Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_219_D
Reset:	soft

Address:	4BB70h-4BB73h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_220_D
Reset:	soft
Address:	4BB74h-4BB77h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_221_D
Reset:	soft
Address:	4BB78h-4BB7Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_222_D
Reset:	soft
Address:	4BB7Ch-4BB7Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_223_D
Reset:	soft
Address:	4BB80h-4BB83h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_224_D
Reset:	soft
Address:	4BB84h-4BB87h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_225_D
Reset:	soft
Address:	4BB88h-4BB8Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_226_D
Reset:	soft
Address:	4BB8Ch-4BB8Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_227_D
Reset:	soft
Address:	4BB90h-4BB93h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_228_D
Reset:	soft

Address:	4BB94h-4BB97h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_229_D
Reset:	soft
Address:	4BB98h-4BB9Bh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_230_D
Reset:	soft
Address:	4BB9Ch-4BB9Fh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_231_D
Reset:	soft
Address:	4BBA0h-4BBA3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_232_D
Reset:	soft
Address:	4BBA4h-4BBA7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_233_D
Reset:	soft
Address:	4BBA8h-4BBABh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_234_D
Reset:	soft
Address:	4BBACh-4BBAFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_235_D
Reset:	soft
Address:	4BBB0h-4BBB3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_236_D
Reset:	soft
Address:	4BBB4h-4BBB7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_237_D
Reset:	soft

Address:	4BBB8h-4BBBBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_238_D
Reset:	soft
Address:	4BBBCh-4BBBFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_239_D
Reset:	soft
Address:	4BBC0h-4BBC3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_240_D
Reset:	soft
Address:	4BBC4h-4BBC7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_241_D
Reset:	soft
Address:	4BBC8h-4BBCBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_242_D
Reset:	soft
Address:	4BBCCh-4BBCFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_243_D
Reset:	soft
Address:	4BBD0h-4BBD3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_244_D
Reset:	soft
Address:	4BBD4h-4BBD7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_245_D
Reset:	soft
Address:	4BBD8h-4BBDBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_246_D
Reset:	soft

Address:	4BBDCh-4BBDFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_247_D
Reset:	soft
Address:	4BBE0h-4BBE3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_248_D
Reset:	soft
Address:	4BBE4h-4BBE7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_249_D
Reset:	soft
Address:	4BBE8h-4BBEBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_250_D
Reset:	soft
Address:	4BBECh-4BBEFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_251_D
Reset:	soft
Address:	4BBF0h-4BBF3h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_252_D
Reset:	soft
Address:	4BBF4h-4BBF7h
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_253_D
Reset:	soft
Address:	4BBF8h-4BBFBh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_254_D
Reset:	soft
Address:	4BBFCh-4BBFFh
Name:	Pipe Legacy Palette
ShortName:	PAL_LGC_255_D
Reset:	soft
There are 256 instances of this register format per display pipe.	

Restriction
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**Red Legacy Palette Entry** Default Value: UUh Access: R/W Red legacy palette entry value.
	15:8	**Green Legacy Palette Entry** Default Value: UUh Access: R/W Green legacy palette entry value.
	7:0	**Blue Legacy Palette Entry** Default Value: UUh Access: R/W Blue legacy palette entry value.

PAL_PREC_DATA

PAL_PREC_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A404h-4A407h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_A
Reset:	soft
Address:	4AC04h-4AC07h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_B
Reset:	soft
Address:	4B404h-4B407h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_C
Reset:	soft
Address:	4BC04h-4BC07h
Name:	Pipe Precision Palette Data
ShortName:	PAL_PREC_DATA_D
Reset:	soft

These are the precision palette entries used for the 10 bpc, split, and 12 bpc gamma. The Precision Palette Index Value indicates the precision palette location to be accessed through this register.

Programming Notes

For 10 bpc, program with the color 10 bit palette entry fraction value. For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value. For 12 bpc gamma even indexes, program the MSbs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs. For split gamma indexes 0 to 511, program with the first gamma (before CSC) color 10 bit palette entry fraction value.For split gamma indexes 512 to 1023, program with the second gamma (after CSC) color 10 bit palette entry fraction value.

For 12 bit Logarithmic Gamma Mode, the first 510 gamma entries are stored in the precision palette with 16 bits per color in a 0.16 format with 0 integer and 16 fractional bits (upper 10 bits in odd indexes, lower 6 bits in even indexes)

Restriction

This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

<table>
<tr><th>DWord</th><th>Bit</th><th>Description</th></tr>
<tr><td>0</td><td>31:30</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>29:20</td><td>Red Precision Palette Entry<table><tr><td>Default Value:</td><td>UUUUUUUUUUb</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Red precision palette entry value.</td></tr>
<tr><td></td><td>19:10</td><td>Green Precision Palette Entry<table><tr><td>Default Value:</td><td>UUUUUUUUUUb</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Green precision palette entry value.</td></tr>
<tr><td></td><td>9:0</td><td>Blue Precision Palette Entry<table><tr><td>Default Value:</td><td>UUUUUUUUUUb</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Blue precision palette entry value.</td></tr>
</table>

PAL_PREC_INDEX

PAL_PREC_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A400h-4A403h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_A
Reset:	soft
Address:	4AC00h-4AC03h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_B
Reset:	soft
Address:	4B400h-4B403h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_C
Reset:	soft
Address:	4BC00h-4BC03h
Name:	Pipe Precision Palette Index
ShortName:	PAL_PREC_INDEX_D
Reset:	soft

This index controls access to the array of precision palette data values.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Index Auto Increment** Access: R/W This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment – Increment the index value with each read or write to the data register.
	14:10	**Reserved** Access: RO Format: MBZ

9:0	**Index Value** Access: R/W This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. **Value** / **Name** [0,1023]

PAL_PREC_MULTI_SEG_DATA

PAL_PREC_MULTI_SEG_DATA

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

These are the precision palette entries used for the multi segment gamma. The Precision Palette Index Value indicates the precision palette location to be accessed through this register.

Programming Notes

For 10 bpc, program with the color 10 bit palette entry fraction value. For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value. For 12 bpc gamma even indexes, program the MSbs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs.

Restriction

This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:20	**Red Precision Palette Entry** Default Value: UUUUUUUUUUb Access: R/W Red precision palette entry value.
	19:10	**Green Precision Palette Entry** Default Value: UUUUUUUUUUb Access: R/W Green precision palette entry value.
	9:0	**Blue Precision Palette Entry** Default Value: UUUUUUUUUUb Access: R/W Blue precision palette entry value.

PAL_PREC_MULTI_SEG_INDEX

PAL_PREC_MULTI_SEG_INDEX

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

This index controls access to the array of precision palette data values used in the multi-segment gamma mode.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Index Auto Increment** Access: R/W This field enables the index auto increment. Value / Name / Description 0b / No Increment / Do not automatically increment the index value. 1b / Auto Increment / Increment the index value with each read or write to the data register.
	14:5	**Reserved** Access: RO Format: MBZ
	4:0	**Index Value** Access: R/W This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. Value / Name [0,17] /

PASID Capability

PASID_CAP_0_2_0_PCI - PASID Capability

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00114h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

DWord	Bit	Description
0	15:13	**Reserved** Access: RO Format: MBZ
	12:8	**Maximum PASID Width** Default Value: 10100b Access: RO _Custom_GTIReset: BUS Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).
	7:4	**Reserved** Access: RO Format: MBZ
	3	**Reserved** Access: RO Format: MBZ
	2	**Privilege Mode Supported** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests-with-PASID.
	1	**Execute Permission Supported** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0. 0 : The Endpoint will never Set the Execute Requested bit. 1 : The Endpoint supports sending TLPs that have the Execute Requests bit set.

PASID_CAP_0_2_0_PCI - PASID Capability		
	0	**Reserved** Access: RO Format: MBZ

PASID Control

PASID_CTRL_0_2_0_PCI - PASID Control		
Register Space:	PCI: 0/2/0	
Size (in bits):	16	
Address:	00116h	
Process Address Space ID (PASID) control for Device-2.		

DWord	Bit	Description
0	15:4	**Reserved** Access: RO Format: MBZ
	3	**Reserved** Access: RO Format: MBZ
	2	**Privileged Mode Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests-with-PASID.
	1	**Execute Permission Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS If Set, the Endpoint is permitted to request execute permission in requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with the Execute Request Enable field Set.
	0	**PASID Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS If Set, the Endpoint is permitted to generate requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. If Privileged Mode Supported field in PASID Capability register is Clear, then this field is treated as Reserved (0). Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with Supervisor Request Enable field Set. For compatibility reasons, this field is implemented as RW.

PASID Extended Capability Header

PASID_EXTCAP_0_2_0_PCI - PASID Extended Capability Header

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00110h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 001000000000b Access: RO _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list.
	19:16	**Version** Default Value: 0001b Access: RO _Custom_GTIReset: BUS Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000011011b Access: RO _Custom_GTIReset: BUS Hardwired to the PASID Extended Capability ID

PAT Index

PAT_INDEX - PAT Index	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	04800h
Name:	PAT INDEX 0
ShortName:	PAT_INDEX_0
Address:	04804h
Name:	PAT INDEX 1
ShortName:	PAT_INDEX_1
Address:	04808h
Name:	PAT INDEX 2
ShortName:	PAT_INDEX_2
Address:	0480Ch
Name:	PAT INDEX 3
ShortName:	PAT_INDEX_3
Address:	04810h
Name:	PAT INDEX 4
ShortName:	PAT_INDEX_4
Address:	04814h
Name:	PAT INDEX 5
ShortName:	PAT_INDEX_5
Address:	04818h
Name:	PAT INDEX 6
ShortName:	PAT_INDEX_6
Address:	0481Ch
Name:	PAT INDEX 7
ShortName:	PAT_INDEX_7

DWord	Bit	Description
0	31:4	**Reserved** Access: RO Format: MBZ
	3:2	**Reserved** Access: RO Format: MBZ

PAT_INDEX - PAT Index		
	1:0	**Mem Type** Default Value: 11b Access: R/W 00: Uncacheable(UC) 01: Write Combining(WC) 10: Write through(WT) 11: Write back(WB)

PCI Command

PCICMD_0_2_0_PCI - PCI Command

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00004h

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant primary accesses to main memory.

DWord	Bit	Description
0	15:11	**Reserved** Access: RO Format: MBZ
	10	**Interrupt Disable** Access: RO INTA signaling is not supported. This hardwired value implies no INTA interrupts will be generated. The PCIe spec indicates that if not implemented, bit should be RO and 0b. Note: It is counterintuitive as interrupt disable=0 indicates interrupts disabled but 0b and RO imply not implemented. Value: 0b — Name:
	9	**Fast Back-to-Back** Default Value: 0b Access: RO _Custom_GTIReset: BUS Not Implemented. Hardwired to 0.
	8	**SERR Enable** Access: R/W _Custom_GTIReset: BUS When set, this bit enables reporting of Non-fatal and Fatal errors detected by the Function to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control register. Value: 0b — Name:
	7	**Wait Cycle Control** Default Value: 0b Access: RO _Custom_GTIReset: BUS Not Implemented. Hardwired to 0.

PCICMD_0_2_0_PCI - PCI Command

6 — Parity Error Enable

Access:	R/W
_Custom_GTIReset:	BUS

This bit controls the logging of poisoned TLPs in the primary Data parity error bit of the status register.

Value	Name
0b	

5 — Video Palette Snooping

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

This bit is hardwired to 0 to disable snooping.

4 — Memory Write and Invalidate Enable

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 0. The IGD does not support memory write and invalidate commands.

3 — Special Cycle Enable

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

This bit is hardwired to 0. The IGD ignores Special cycles.

2 — Bus Primary Enable

Default Value:	0b
Access:	R/W
_Custom_GTIReset:	BUS

0: Disable IGD bus primarying. 1: Enable the IGD to function as a PCI compliant primary.

1 — Memory Access Enable

Default Value:	0b
Access:	R/W
_Custom_GTIReset:	BUS

This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.

PCICMD_0_2_0_PCI - PCI Command

	0	**I/O Access Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable. This field is RO 1'b0 if DEV2CTL[0] IOBARDIS at offset 0x58 is 1b. Read-only with 0 defaults when display is not present.

PCI Express Capability

PCIECAP_0_2_0_PCI - PCI Express Capability

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00072h

PCI Express Capability

DWord	Bit	Description
0	15:14	**Reserved** Access: RO Format: MBZ
	13:9	**Interrupt Message Number** Default Value: 00000b Access: RO _Custom_GTIReset: BUS This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Since this device only supports one MSI vector, this field is hardwired to 0.
	8	**Slot Implemented** Default Value: 0b Access: RO _Custom_GTIReset: BUS This field is hardwired to 0 for an endpoint device.
	7:4	**Device Type** Default Value: 0000b Access: RO _Custom_GTIReset: BUS This field is hardwired to 0h to indicate a PCIe Endpoint.
	3:0	**Capability Version** Default Value: 0010b Access: RO _Custom_GTIReset: BUS This field is hardwired to 2h per the PCI Express Base Specification.

PCI Express Capability Header

PCIECAPHDR_0_2_0_PCI - PCI Express Capability Header		
Register Space:	PCI: 0/2/0	
Size (in bits):	16	
Address:	00070h	
PCI Express Capability Header		
DWord	**Bit**	**Description**
0	15:8	**Next Capability Pointer** Default Value: 10101100b Access: RO _Custom_GTIReset: BUS This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.
	7:0	**Capability Identifier** Default Value: 00010000b Access: RO _Custom_GTIReset: BUS This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.

PCI Express Device Control

DEVICECTL_0_2_0_PCI - PCI Express Device Control

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00078h

PCI Express Device Control

DWord	Bit	Description
0	15	**Initiate Function Level Reset** Default Value: 0b Access: R/W _Custom_GTIReset: BUS A write of 1b initiates Function Level Reset to the Function. During FLR, a read will return 1b since device 2 reads abort. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.
	14:12	**Max Read Request Size** Default Value: 000b Access: RO _Custom_GTIReset: BUS Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.
	11	**Enable No Snoop** Default Value: 1b Access: R/W _Custom_GTIReset: BUS If this bit is Set, the Function is permitted to Set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Note that setting this bit to 1b should not cause a Function to Set the No Snoop attribute on all transactions that it initiates. Even when this bit is Set, a Function is only permitted to Set the No Snoop attribute on a transaction when it can guarantee that the address of the transaction is not stored in any cache in the system. This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates. Default value of this bit is 1b.

DEVICECTL_0_2_0_PCI - PCI Express Device Control

10	**Aux Power PM Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Functions that do not implement this capability hardwire this bit to 0b.
9	**Phantom Functions Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Functions that do not implement this capability hardwire this bit to 0b.
8	**Extended Tag field Enable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS When Set, this bit enables a function to use an 8-bit Tag field as a requester. If the bit is clear, the function is restricted to a 5-bit Tag field. Functions that do not implement this capability hardware this bit to 0b.
7:5	**Max Payload Size** Default Value: 000b Access: RO _Custom_GTIReset: BUS Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.
4	**Enable Relaxed Ordering** Default Value: 1b Access: R/W _Custom_GTIReset: BUS If this bit is Set, the Function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. Default value of this bit is 1b.

DEVICECTL_0_2_0_PCI - PCI Express Device Control

	3	**Unsupported Request Response Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS A PCIe endpoint. This bit, in conjunction with other bits, controls the signaling of Unsupported Request Errors by sending error Messages (see Section 6.2.5.). For a multi-Function device, this bit controls error reporting for each Function from point-of-view of the respective Function this bit to 0b.
	2	**Fatal Error Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit, in conjunction with other bits, controls sending ERR_FATAL Messages (see Section 6.2.5 and Section 6.2.6 for details).
	1	**Non-Fatal Error Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages (see Section 6.2.5 and Section 6.2.6 for details).
	0	**Correctable Error Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit, in conjunction with other bits, controls sending ERR_COR Messages (see Section 6.2.5 and Section 6.2.6 for details).

PCI Express Device Status Register

DEVICESTS_0_2_0_PCI - PCI Express Device Status Register

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	0007Ah

PCI Express Capability Structure

DWord	Bit	Description
0	15:6	**Reserved** Access: RO Format: MBZ
	5	**Transactions Pending** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed. A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
	4	**Aux Power Detected** Default Value: 0b Access: RO _Custom_GTIReset: BUS Functions that require Aux power report this bit as Set if Aux power is detected by the Function. Hardwired to 0b, the integrated graphics device does not require Aux power.
	3	**Unsupported Request Detected** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS This bit indicates the Function received an Unsupported Request.
	2	**Fatal Error Detected** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS This bit indicates status of fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.

DEVICESTS_0_2_0_PCI - PCI Express Device Status Register

	1	**Non-Fatal Error Detected** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS This bit indicates status of non fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.
	0	**Correctable Error Detected** Default Value: 0b Access: R/WC _Custom_GTIReset: BUS This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.

PCI Mirror of GMCH Graphics Control

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00050h

Mirror of GGC register from GTTMMADR Space at offset 0x108040.

DWord	Bit	Description
0	15:8	**GMS** Default Value: 05h Access: RO Variant _Custom_GTIReset: BUS Mirrored from GTTMMADR Space offset 0x108040. This field reflects amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. It corresponds to DSM (Data Stolen Memory region) region. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Fh: Reserved 40h: 2048MB 41h - EFh: Reserved F0h: 4MB F1h: 8MB F2h: 12MB F3h: 16MB F4h: 20MB

F5h: 24MB
F6h: 28MB
F7h: 32MB
F8h: 36MB
F9h: 40MB
FAh: 44MB
FBh: 48MB
FCh: 52MB
FDh: 56MB
FEh: 60MB
FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.

7:6 **GGMS**

Default Value:	00b
Access:	RO Variant
_Custom_GTIReset:	BUS

Mirrored from GTTMMADR Space offset 0x108040.
This field is used to select the amount of Main Memory that is pre-allocated to support the Graphics Translation Table.
0x0:No Preallocated Memory
0x1:2MB of Preallocated Memory
0x2:4MB of Preallocated Memory
0x3:8MB of Preallocated Memory

5:3 **Reserved**

Access:	RO
Format:	MBZ

2 **VAMEN**

Default Value:	0b
Access:	RO Variant
_Custom_GTIReset:	BUS

Mirrored from GTTMMADR Space offset 0x108040.
Enables the use of the iGFX engines for Versatile Acceleration.
0 - GFX engines are in GFX Mode. Gfx Device Class Code is 030000h.
1 - GFX engines are in Versatile Acceleration Mode. Gfx Device Class Code is 038000h.

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control

	1	**IVD** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS Mirrored from GTTMMADR Space offset 0x108040. 0: Enable. Gfx Device claims VGA memory and IO cycles, the Sub-Class Code within Class Code register is 00. 1: Disable. Gfx Device does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Class Code register is 80.
	0	**SPARE** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS Mirrored from GTTMMADR Space offset 0x108040.

PCI Status

PCISTS2_0_2_0_PCI - PCI Status

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	00006h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant primary abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

DWord	Bit	Description
0	15	**Detected Parity Error** Access: R/W One Clear _Custom_GTIReset: BUS Set whenever a poisoned TLP is received, regardless of Parity Error Response bit in the command register. This bit is set by a function whenever it receives a poisoned TLP, regardless of the state Parity Error Response bit in the Command register. Value: 0b — Name:
	14	**Signaled System Error** Access: R/W One Clear _Custom_GTIReset: BUS Set if ERR_FATAL or ERR_NONFATAL message sent and SERR Enable in command register=1. Gfx device sets after sending ERR_FATAL or ERR_NONFATAL message. Value: 0b — Name:
	13	**Received Primary Abort Status** Access: R/W One Clear _Custom_GTIReset: BUS Received completion with an unsupported Request (UR) completion status. Set if Gfx device receives UR completion Valid Values. Value: 0b — Name:
	12	**Received Target Abort Status** Access: R/W One Clear _Custom_GTIReset: BUS Set if requester receives completion with completer abort. Set if SGunit receives Target Abort completion. Value: 0b — Name:

PCISTS2_0_2_0_PCI - PCI Status

11	**Signaled Target Abort Status**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 0. The IGD does not use target abort semantics.

10:9	**DEVSEL Timing**

Default Value:	00b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 00.

8	**Primary Data Parity Error Detected**

Default Value:	0b
Access:	R/W One Clear
_Custom_GTIReset:	BUS

This bit is set by an Endpoint Function if the Parity Error Response bit in the Command register is 1b and either of the following two conditions occurs:

- Endpoint receives a Poisoned Completion
- Endpoint transmits a Poisoned Request

If the Parity Error Response bit is 0b, this bit is never set.

7	**Fast Back-to-Back**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 0 to be compliant to PCI Express Base Spec (rev 3.0).

6	**User Defined Format**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 0.

5	**66 MHz PCI Capable**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 0.

PCISTS2_0_2_0_PCI - PCI Status

	4	**Capability List** Default Value: 1b Access: RO _Custom_GTIReset: BUS This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
	3	**Interrupt Status** Access: RO Read only '0 since INT signal is not supported. Value: 0b — Name:
	2:0	**Reserved** Access: RO Format: MBZ

PCU Interrupt Definition

PCU Interrupt Definition

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	444E0h-444EFh
Name:	PCU Interrupts
ShortName:	PCU_INTERRUPT

This table indicates which events are mapped to each bit of the PCU Interrupt registers.
0x444E0 = ISR
0x444E4 = IMR
0x444E8 = IIR
0x444EC = IER

DWord	Bit	Description
0	31	**DDIA DC9 HPD** _Custom_GTIReset: BUS This field indicates DDIA hotplug activity was detected during DC9.
	30	**DDIB DC9 HPD** _Custom_GTIReset: BUS This field indicates DDIB hotplug activity was detected during DC9.
	29	**DDIC DC9 HPD** _Custom_GTIReset: BUS This field indicates DDIC hotplug activity was detected during DC9.
	28	**Spare_28** _Custom_GTIReset: BUS Spare bit
	27	**Spare_27** _Custom_GTIReset: BUS Spare bit
	26	**Spare_26** _Custom_GTIReset: BUS Spare bit
	25	**PCU_Pcode2driver_Mailbox_Event** _Custom_GTIReset: BUS

PCU Interrupt Definition

	24	**PCU_Thermal_Event** _Custom_GTIReset: BUS
	23	**Spare_23** _Custom_GTIReset: BUS Spare bit
	22	**Spare_22** _Custom_GTIReset: BUS Spare bit
	21	**Spare_21** _Custom_GTIReset: BUS Spare bit
	20	**Spare_20** _Custom_GTIReset: BUS Spare bit
	19	**Spare_19** _Custom_GTIReset: BUS Spare bit
	18	**Spare_18** _Custom_GTIReset: BUS Spare bit
	17	**Spare_17** _Custom_GTIReset: BUS Spare bit
	16	**Spare_16** _Custom_GTIReset: BUS Spare bit
	15	**Spare_15** _Custom_GTIReset: BUS Spare bit

PCU Interrupt Definition

	14	**Spare_14** _Custom_GTIReset: BUS Spare bit
	13	**Spare_13** _Custom_GTIReset: BUS Spare bit
	12	**Spare_12** _Custom_GTIReset: BUS Spare bit
	11	**Spare_11** _Custom_GTIReset: BUS Spare bit
	10	**Spare_10** _Custom_GTIReset: BUS Spare bit
	9	**Spare_9** _Custom_GTIReset: BUS Spare bit
	8	**Spare_8** _Custom_GTIReset: BUS Spare bit
	7	**Spare_7** _Custom_GTIReset: BUS Spare bit
	6	**Spare_6** _Custom_GTIReset: BUS Spare bit
	5	**Spare_5** _Custom_GTIReset: BUS Spare bit

PCU Interrupt Definition		
	4	**Spare_4** _Custom_GTIReset: BUS Spare bit
	3	**Spare_3** _Custom_GTIReset: BUS Spare bit
	2	**Spare_2** _Custom_GTIReset: BUS Spare bit
	1	**Spare_1** _Custom_GTIReset: BUS KVMR Release Display Enable - This field indicates that KVMR is no longer requesting driver to enable a display output.
	0	**Spare_0** _Custom_GTIReset: BUS KVMR Request Display Enable -This field indicates that KVMR is requesting driver to enable a display output.

Persistent Batch Buffer State Register

PRT_BB_STATE - Persistent Batch Buffer State Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02120h-02127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_RCSUNIT_CTX
Address:	22120h-22127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_BCSUNIT_CTX
Address:	1C0120h-1C0127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VCSUNIT0_CTX
Address:	1C4120h-1C4127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VCSUNIT1_CTX
Address:	1C8120h-1C8127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VECSUNIT0_CTX
Address:	1D0120h-1D0127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VCSUNIT2_CTX
Address:	1D4120h-1D4127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VCSUNIT3_CTX
Address:	1D8120h-1D8127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VECSUNIT1_CTX
Address:	1E0120h-1E0127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VCSUNIT4_CTX
Address:	1E4120h-1E4127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VCSUNIT5_CTX

PRT_BB_STATE - Persistent Batch Buffer State Register

Address:	1E8120h-1E8127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VECSUNIT2_CTX

Address:	1F0120h-1F0127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VCSUNIT6_CTX

Address:	1F4120h-1F4127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VCSUNIT7_CTX

Address:	1F8120h-1F8127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_VECSUNIT3_CTX

Address:	1A120h-1A127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_CCSUNIT0_CTX

Address:	1C120h-1C127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_CCSUNIT1_CTX

Address:	1E120h-1E127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_CCSUNIT2_CTX

Address:	26120h-26127h
Name:	PRT_BB_STATE
ShortName:	PRT_BB_STATE_CCSUNIT3_CTX

This register holds the details of the Persistent Batch Buffer. This register have valid values only when the Persistent Batch Buffer Valid bit is set to1.
This register is part of the context state and context save/restored on a context switch.

DWord	Bit	Description
0..1	63:57	**Reserved** Access: RO Format: MBZ
	56:48	**Reserved** Access: RO Format: MBZ

PRT_BB_STATE - Persistent Batch Buffer State Register

	47:32	**Persistent Batch Buffer Head Pointer UDW** This field specifies the DWord-aligned Graphics Memory Address Upper DWORD of the persistent batch buffer.
	31:2	**Persistent Batch Buffer Head Pointer LDW** Access: R/W Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address Lower DWROD of the persistent batch buffer.
	1	**Address Space Indicator** Access: R/W **Value** / **Name** / **Description** 0h / GGTT **[Default]** / This Batch buffer is located in GGTT memory and is privileged 1h / PPGTT / This Batch buffer is located in PPGTT memory and is non-privileged.
	0	**Persistent Batch Buffer Valid** Access: R/W Format: U1 **Value** / **Name** / **Description** 0h / Invalid **[Default]** / Persistent Batch buffer Invalid 1h / Valid / Persistent Batch buffer Valid

PF Resizable BAR Capability

PF_RESIZE_BAR_CAP_0_2_0_PCI - PF Resizable BAR Capability

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00424h

PF Resizable capability reports support for PF Resizing of Gfx device PF LMEMBAR sizes.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:12	**PFSUPSIZES** Default Value: 111111111111b Access: RO Variant _Custom_GTIReset: BUS Bits 14:12 are hardwired to reset value shown. Bits 23:15 are controlled by fuses and are override-able via CSC writing to an MMIO register. ---- Bit 12=Function will operate with BAR sized to 256MB. Bit 13=Function will operate with BAR sized to 512MB. Bit 14=Function will operate with BAR sized to 1GB. Bit 15=Function will operate with BAR sized to 2GB. Bit 16=Function will operate with BAR sized to 4GB. Bit 17=Function will operate with BAR sized to 8GB. Bit 18=Function will operate with BAR sized to 16GB. Bit 19=Function will operate with BAR sized to 32GB. Bit 20=Function will operate with BAR sized to 64GB. Bit 21=Function will operate with BAR sized to 128GB. Bit 22=Function will operate with BAR sized to 256GB. Bit 23=Function will operate with BAR sized to 512GB.

PF_RESIZE_BAR_CAP_0_2_0_PCI - PF Resizable BAR Capability

	11:4	**PFUNSUPSIZES** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s. Bit 4=Function will operate with BAR sized to 1MB. Bit 5=Function will operate with BAR sized to 2MB. Bit 6=Function will operate with BAR sized to 4MB. Bit 7=Function will operate with BAR sized to 8MB. Bit 8=Function will operate with BAR sized to 16MB. Bit 9=Function will operate with BAR sized to 32MB. Bit 10=Function will operate with BAR sized to 64MB. Bit 11=Function will operate with BAR sized to 128MB.
	3:0	**Reserved** Access: RO Format: MBZ

PF Resizable BAR Control

PF_RESIZABLE_BAR_CTRL_0_2_0_PCI - PF Resizable BAR Control

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00428h

PF Resizable BAR control for Gfx device.

DWord	Bit	Description
0	31:14	**Reserved** Access: RO Format: MBZ
	13:8	**PF BAR Size** Access: R/W _Custom_GTIReset: BUS PF Bar Size - This is an encode value. 0=1MB (2^20) 1=2MB (2^21) 2=4MB (2^22) 3=8MB (2^23) ... 08=256MB (default) ... 13=8GB 14=16GB 15=32GB 16=64GB ... 43=8EB (2^63) The default value of this field is equal to the default size of the address space that the PFBAR resource is requesting via the PFBAR's Read-only bits. Behavior is undefined if a value is written in the field and the corresponding supported size bit is not Set in the PF Resizable BAR Capability or PF Resizable BAR control registers. When this register field is programmed, the value is immediately reflected in the size of the resource, as encoded in the number of read-only bits in the PF BAR. Value: 001000b — Name: **[Default]**

PF_RESIZABLE_BAR_CTRL_0_2_0_PCI - PF Resizable BAR Control

	7:5	**Num of Resizable BARs** Default Value: 001b Access: RO _Custom_GTIReset: BUS Hardwired to 1. Indicates the total number of resizable BARs in the capability structure for the function. The value of this field must be in the range of 1h to 6h.
	4:0	**Bar Index** Default Value: 02h Access: RO _Custom_GTIReset: BUS 0=PF BAR at offset 10h 1=PF BAR at offset 14h 2=PF BAR at offset 18h 3=PF BAR at offset 1Ch 4=PF BAR at offset 20h 5=VF BARat offset 24h For a 64-bit Base address register, the BAR index indicates the lower Dword. This value indicates which BAR supports a negotiable size.

PF Resizable Capability Header

PF_RESIZE_CAPHDR_0_2_0_PCI - PF Resizable Capability Header

Register Space: PCI: 0/2/0
Size (in bits): 32

Address: 00420h

PF Resizable capability allows the PF LMEMBAR value to be resized.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Access: RO Variant _Custom_GTIReset: BUS **Description**: If SRIOV is enabled by fuse, this is a hardwired pointer to the next item in the capabilities list (0x220 VF Resizable BAR Extended Capability Header). If SRIOV is disabled by fuse, this is a hardwired pointer to the next item in the capabilities list (0x400 LTR Extended Capability Header). 001000100000b **[Default]** 010000000000b
	19:16	**Version** Default Value: 0001b Access: RO _Custom_GTIReset: BUS Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000010101b Access: RO _Custom_GTIReset: BUS Hardwired to 0015h which is the PCI Express Extended Cap ID for the Resizable BAR capability.

PHY_MISC

PHY_MISC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	64C00h-64C03h
Name:	PHY_MISC_A
ShortName:	PHY_MISC_A
Reset:	global
Address:	64C04h-64C07h
Name:	PHY_MISC_B
ShortName:	PHY_MISC_B
Reset:	global
Address:	64C08h-64C0Bh
Name:	PHY_MISC_C
ShortName:	PHY_MISC_C
Reset:	global
Address:	64C0Ch-64C0Fh
Name:	PHY_MISC_D
ShortName:	PHY_MISC_D
Reset:	global
Address:	64C14h-64C17h
Name:	PHY_MISC_TC1
ShortName:	PHY_MISC_TC1
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.

DWord	Bit	Description	
0	31	**Reserved**	
		Access:	R/W
	30	**Reserved**	
		Access:	R/W
	29	**Reserved**	
		Access:	R/W
	28	**Reserved**	
		Access:	R/W

PHY_MISC

	27:24	**Reserved** Access: RO Format: MBZ
	23	**dp_tx0_ack** Default Value: 0b Access: RO indicates the requested TX setting is completed. Stays asserted until the request input is de-asserted. Also asserts during lane reset.
	22	**dp_tx1_ack** Default Value: 0b Access: RO See tx0 ack description.
	21	**dp_tx2_ack** Default Value: 0b Access: RO See tx0 ack description.
	20	**dp_tx3_ack** Default Value: 0b Access: RO See tx0 ack description.
	19:12	**Reserved** Access: RO Format: MBZ
	11:10	**Reserved** Access: R/W
	9:8	**Reserved** Access: R/W
	7:6	**Reserved** Access: R/W
	5:4	**Reserved** Access: R/W
	3:0	**Reserved** Access: RO Format: MBZ

PHY_MISC1

PHY_MISC1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	64D00h-64D03h
Name:	PHY_MISC1_A
ShortName:	PHY_MISC1_A
Reset:	global
Address:	64D04h-64D07h
Name:	PHY_MISC1_B
ShortName:	PHY_MISC1_B
Reset:	global
Address:	64D08h-64D0Bh
Name:	PHY_MISC1_C
ShortName:	PHY_MISC1_C
Reset:	global
Address:	64D0Ch-64D0Fh
Name:	PHY_MISC1_D
ShortName:	PHY_MISC1_D
Reset:	global
Address:	64D14h-64D17h
Name:	PHY_MISC1_TC1
ShortName:	PHY_MISC1_TC1
Reset:	global

This register is on the ungated clock and the chip reset, not the FLR.

DWord	Bit	Description
0	31	**dp_tx0_data_en** Default Value: 0b Access: R/W output driver is de-asserted when dp_txX_data_en is low OR when lane is not in P0.
	30	**dp_tx0_disable** Default Value: 0b Access: R/W Asynchronous disable of terminations

PHY_MISC1

		This can be changed only when TX clock is disabled (txX_pstate[1:0]=P2/P3 or txX_reset=1.
	29	**dp_tx0_reset** Default Value: 0b Access: R/W TX reset. Resets TX datapath, all the transmitter settings and state machines, including common-mode adjustments and receiver detection state machines.
	28	**dp_tx0_clk_rdy** Default Value: 0b Access: R/W TX input clock ready. When dp_txX_clk is active and stable, dp_txX_clk_rdy should be asserted at the same time for all TX lanes and remain active as long as the link is active (for example, P0) even if some of the lanes in the link are powered down or in reset. .
	27	**dp_tx1_data_en** Default Value: 0b Access: R/W output driver is de-asserted when dp_txX_data_en is low OR when lane is not in P0.
	26	**dp_tx1_disable** Default Value: 0b Access: R/W Asynchronous disable of terminations This can be changed only when TX clock is disabled (txX_pstate[1:0]=P2/P3 or txX_reset=1.
	25	**dp_tx1_reset** Default Value: 0b Access: R/W TX reset. Resets TX datapath, all the transmitter settings and state machines, including common-mode adjustments and receiver detection state machines.
	24	**dp_tx1_clk_rdy** Default Value: 0b Access: R/W TX input clock ready. When dp_txX_clk is active and stable, dp_txX_clk_rdy should be asserted at the same time for all TX lanes and remain active as long as the link is active (for example, P0) even if some of the lanes in the link are powered down or in reset. .
	23	**dp_tx2_data_en** Default Value: 0b

PHY_MISC1

	Access:	R/W

output driver is de-asserted when dp_txX_data_en is low OR when lane is not in P0.

22 **dp_tx2_disable**

Default Value:	0b
Access:	R/W

Asynchronous disable of terminations
This can be changed only when TX clock is disabled (txX_pstate[1:0]=P2/P3 or txX_reset=1.

21 **dp_tx2_reset**

Default Value:	0b
Access:	R/W

TX reset. Resets TX datapath, all the transmitter settings and state machines, including common-mode adjustments and receiver detection state machines.

20 **dp_tx2_clk_rdy**

Default Value:	0b
Access:	R/W

TX input clock ready. When dp_txX_clk is active and stable, dp_txX_clk_rdy should be asserted at the same time for all TX lanes and remain active as long as the link is active (for example, P0) even if some of the lanes in the link are powered down or in reset. .

19 **dp_tx3_data_en**

Default Value:	0b
Access:	R/W

output driver is de-asserted when dp_txX_data_en is low OR when lane is not in P0.

18 **dp_tx3_disable**

Default Value:	0b
Access:	R/W

Asynchronous disable of terminations
This can be changed only when TX clock is disabled (txX_pstate[1:0]=P2/P3 or txX_reset=1.

17 **dp_tx3_reset**

Default Value:	0b
Access:	R/W

TX reset. Resets TX datapath, all the transmitter settings and state machines, including common-mode adjustments and receiver detection state machines.

16 **dp_tx3_clk_rdy**

PHY_MISC1			
		Default Value:	0b
		Access:	R/W
		TX input clock ready. When dp_txX_clk is active and stable, dp_txX_clk_rdy should be asserted at the same time for all TX lanes and remain active as long as the link is active (for example, P0) even if some of the lanes in the link are powered down or in reset. .	
	15:1	**Reserved**	
		Access:	RO
		Format:	MBZ
	0	**Reserved**	
		Access:	R/W

Pinned Surface Mapping Size Register

PINNED_SURFACE_SIZE - Pinned Surface Mapping Size Register

Register Space: MMIO: 0/2/0

Size (in bits): 32

Pinned Surface Mapping Size register

DWord	Bit	Description
0	31:12	**Size** Default Value: 0000000000000000000b Access: R/W _Custom_GTIReset: DEV Size of the surface(s) in 4KB pages. Must be > 0.
	11:1	**Reserved** Access: RO Format: MBZ
	0	**Valid** Default Value: 0b Access: R/W _Custom_GTIReset: DEV 1'b0: This entry is not valid 1'b1: This entry is valid

Pinned Surface Per Process Virtual Address Base Register

PINNED_SURFACE_PPBASE_H - Pinned Surface Per Process Virtual Address Base Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32

Pinned Surface Per Process Virtual Address Base register

DWord	Bit	Description
0	31:0	**Per Process Virtual Base_H** Default Value: 0000h Access: R/W _Custom_GTIReset: DEV Per Process Virtual Address Base - PPBASE[47:16] 4KB Page number of the surface(s) in Per-Process Virtual Address Space (ie, index into the PPGTT)

Pinned Surface Process ID Register

PINNED_SURFACE_PROCESS_ID - Pinned Surface Process ID Register

Register Space: MMIO: 0/2/0

Size (in bits): 32

Pinned Surface Process ID register

DWord	Bit	Description
0	31:0	**Process ID** Default Value: 0000h Access: R/W _Custom_GTIReset: DEV ID of the Process that owns the pinned surfaces represented by this register.

Pinned Surface Virtual Address Base Register

PINNED_SURFACE_ADDR_BASE - Pinned Surface Virtual Address Base Register

Register Space: MMIO: 0/2/0

Size (in bits): 32

Pinned Surface Virtual Address Base register

DWord	Bit	Description
0	31:28	**Per Process Virtual Base_L** Default Value: 0000b Access: R/W _Custom_GTIReset: DEV Per Process Virtual Address Base - PPBASE[15:12] 4KB Page number of the surface(s) in Per-Process Virtual Address Space (ie, index into the PPGTT)
	27:20	**Reserved** Access: RO Format: MBZ
	19:0	**Global Virtual Address Base** Default Value: 00000000000000000000b Access: R/W _Custom_GTIReset: DEV 4KB Page number of the surface(s) in Global Virtual Address Space (ie, index into the GGTT). The entire range from Base to Base+Size-1 must fall within the Pinned Range of the GGTT.

PIPE_ARB_CTL

PIPE_ARB_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled

Address:	70028h-7002Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_A
Reset:	soft

Address:	71028h-7102Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_B
Reset:	soft

Address:	72028h-7202Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_C
Reset:	soft

Address:	73028h-7302Bh
Name:	Pipe Arbiter Control
ShortName:	PIPE_ARB_CTL_D
Reset:	soft

There is one instance of this register per pipe.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:21	**Reserved** Access: RO Format: MBZ
	20	**Disable Weighted Arbitration** Access: Double Buffered This field disables the weighted pipe slice arbitration. 0b: Enable **[Default]** 1b: Disable

PIPE_ARB_CTL

	19	**Reserved** Access: Double Buffered
	18:16	**Additional Slots** Access: Double Buffered These additional Slots gets added to each arbitration cycle during which the clients gets serviced in a round robin manner.A programmed value of 1b results in 1 additional slot.
	15:14	**Reserved** Access: RO Format: MBZ
	13	**Use Programmed Slots** Access: Double Buffered When this field is set, HW uses the Slots programmed in the PLANE_CTL register instead of the HW defaults.
	12	**Disable Block Valid Check** Access: Double Buffered The field disables the block valid check done at pipe arbiter.

Value	Name
0b	Enable
1b	Disable

	11:10	**DSB Arbitration Interval** Access: Double Buffered This field defines the DSB requests service interval in the pipe arbitration.

Value	Name
00b	16 clocks
01b	32 clocks
10b	64 clocks **[Default]**
11b	128 clocks

	9:8	**Request Vs Data Arbitration** Access: Double Buffered This field selects the arbitration weightage for the Streamer and the DDB requests.

Value	Name	Description
00b		Allow 1 Streamer requests every 2 DDB requests.
01b		Allow 1 Streamer requests every 4 DDB requests.
10b	**[Default]**	Allow 1 Streamer requests every 8 DDB requests.
11b		Allow 1 Streamer requests every 16 DDB requests.

	7:6	**Reserved**

PIPE_ARB_CTL

		Access: RO
		Format: MBZ
	5:0	**Frame Start Drain Delay** Access: Double Buffered This field contains the time, in microseconds, the pipe waits before draining the data from the Display Buffer.

Value	Name
[0-31]	
15	**[Default]**

PIPE_BOTTOM_COLOR

PIPE_BOTTOM_COLOR

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled

Address:	70034h-70037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_A
Reset:	soft

Address:	71034h-71037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_B
Reset:	soft

Address:	72034h-72037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_C
Reset:	soft

Address:	73034h-73037h
Name:	Pipe Bottom Color
ShortName:	PIPE_BOTTOM_COLOR_D
Reset:	soft

This register sets the color that appears underneath the bottom most plane in the pipe blender Z-order.The value for each color channel is represented in an unsigned 0.10 format with 0 integer and 10 fractional bits.

DWord	Bit	Description
0	31	**Pipe Gamma Enable** Access: Double Buffered This bit enables pipe gamma correction for the bottom color. This field is deprecated. Value / Name: 0b – Disable 1b – Enable
	30	**Pipe CSC Enable** Access: Double Buffered

PIPE_BOTTOM_COLOR

		This bit enables pipe color space conversion for the bottom color. This field is deprecated. Value: 0b — Name: Disable Value: 1b — Name: Enable
	29:20	**V R Bottom Color** Access: Double Buffered Format: U0.10 This field sets the bottom color for the V or Red channel.
	19:10	**Y G Bottom Color** Access: Double Buffered Format: U0.10 This field sets the bottom color for the Y or Green channel.
	9:0	**U B Bottom Color** Access: Double Buffered Format: U0.10 This field sets the bottom color for the U or Blue channel.

PIPE_DB_CTL

PIPE_DB_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70070h-70073h
Name:	Pipe Double Buffer Control
ShortName:	PIPE_DB_CTL_A
Reset:	soft
Address:	71070h-71073h
Name:	Pipe Double Buffer Control
ShortName:	PIPE_DB_CTL_B
Reset:	soft
Address:	72070h-72073h
Name:	Pipe Double Buffer Control
ShortName:	PIPE_DB_CTL_C
Reset:	soft
Address:	73070h-73073h
Name:	Pipe Double Buffer Control
ShortName:	PIPE_DB_CTL_D
Reset:	soft

DWord	Bit	Description
0	31	**Internal DB Stall 4** Access: R/W This field stalls double buffering (temporarily prevents double buffer updates) for pipe and transcoder resources that have allowed it. Value: 0b — Name: Unmask Value: 1b — Name: Mask
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Internal DB Stall 3** Access: R/W This field stalls double buffering (temporarily prevents double buffer updates) for pipe and transcoder resources that have allowed it.

PIPE_DB_CTL

	Value	Name
	0b	Unmask
	1b	Mask

22:16 Reserved

Access:	RO
Format:	MBZ

15 Internal DB Stall 2

Access:	R/W

This field stalls double buffering (temporarily prevents double buffer updates) for pipe and transcoder resources that have allowed it.

Value	Name
0b	Unmask
1b	Mask

14:8 Reserved

Access:	RO
Format:	MBZ

7 Internal DB Stall 1

Access:	R/W

This field stalls double buffering (temporarily prevents double buffer updates) for pipe and transcoder resources that have allowed it.

Value	Name
0b	Unmask
1b	Mask

6:0 Reserved

Access:	RO
Format:	MBZ

PIPE_DMCSCANLINECOMP

PIPE_DMCSCANLINECOMP

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7000Ch-7000Fh
Name:	Pipe Scan Line Compare for DMC
ShortName:	PIPE_DMCSCANLINECOMP_A
Reset:	soft
Address:	7100Ch-7100Fh
Name:	Pipe Scan Line Compare for DMC
ShortName:	PIPE_DMCSCANLINECOMP_B
Reset:	soft
Address:	7200Ch-7200Fh
Name:	Pipe Scan Line Compare for DMC
ShortName:	PIPE_DMCSCANLINECOMP_C
Reset:	soft
Address:	7300Ch-7300Fh
Name:	Pipe Scan Line Compare for DMC
ShortName:	PIPE_DMCSCANLINECOMP_D
Reset:	soft

DWord	Bit	Description
0	31	**Enable Compare** Access: R/W This field enables the scan line compare for DMC event generation. When this register is written with this bit set to 1b, the display engine will, trigger a scan line event after reaching the programmed scan line number. It will do the same on every frame. Value / Name: 0b: Do nothing 1b: Enable compare Restriction: Do not enable this register if the event is not needed in the DMC.
	30:20	**Reserved** Access: RO Format: MBZ

PIPE_DMCSCANLINECOMP		
	19:0	**Scan Line Value** Access: R/W This field specifies the ending scan line number of the scan line window.

PIPE_DSS_CTL1

PIPE_DSS_CTL1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	78000h-78003h
Name:	PIPE DSS Control 1
ShortName:	PIPE_DSS_CTL1_PA
Reset:	soft
Address:	78200h-78203h
Name:	PIPE DSS Control 1
ShortName:	PIPE_DSS_CTL1_PB
Reset:	soft
Address:	78400h-78403h
Name:	PIPE DSS Control 1
ShortName:	PIPE_DSS_CTL1_PC
Reset:	soft
Address:	78600h-78603h
Name:	PIPE DSS Control 1
ShortName:	PIPE_DSS_CTL1_PD
Reset:	soft

Display stream splitter and joiner control.

DWord	Bit	Description
0	31	**Splitter Enable** Access: R/W This field enables stream splitting. This bit must be set to enable MSO configuration. Value / Name: 0b – Disable 1b – Enable Restriction: Restriction: Splitter enable is supported for pipe A only.
	30	**Joiner Enable** Access: R/W This field enables stream joiner after compression. Value / Name: 0b – Disable

PIPE_DSS_CTL1

	1b	Enable

29 Big_Joiner_Enable

Access:	R/W

Description
When big_joiner_enable is '1', this dssunit will be working with another dssunit in adjacent pipe either as a primary or as a secondary.
This bit should not be asserted when uncompressed pipe streams are joined.

Value	Name
0b	Disable
1b	Enable

28 Primary_Big_Joiner_Enable

Access:	R/W

Description
This bit indicates that this pipe is the primary/secondary when Big_Joiner_Enable bit is set in this register.
This bit should not be asserted when uncompressed pipe streams are joined.

Value	Name
0b	Secondary
1b	Primary

27 Reserved

Access:	R/W

26:25 Splitter Configuration

Access:	R/W

MSO support; stream splitting configurations. Make sure splitter is enabled using bit [31] of this register.

MSO mode	Splitter Enable	Splitter Configuration
Not supported	0	XX
2x1	1	00
2x2	1	00
4x1	1	01

Value	Name
00b	2-segment
01b	4-segment

PIPE_DSS_CTL1

24	**Dual Link Mode**

Access:	R/W

This field selects the split pattern. Applicable only if splitter mode is enabled through DSS configuration bits.

Value	Name
0b	Front-Back mode
1b	Interleave mode

23:22	**Reserved**

Access:	RO
Format:	MBZ

21	**Uncompressed Joiner Primary**

Access:	R/W

Description
When enabled as primary of uncompressed stream joiner, this DSS unit will consume pixel stream from **adjacent** pipe DSS unit. Pipe D DSS unit can have additional 4PPC interface to support Pipe Macros. Recommendation is to connect only Pipe A/B/C interface.
Uncompressed joiner must not be enabled when big/ultra joiners are enabled on the same pipe and vice versa.

Value	Name
0b	not primary
1b	primary

20	**Uncompressed Joiner Secondary**

Access:	R/W

Description
When enabled as secondary of uncompressed stream joiner, this DSS unit will drive pixel stream to **adjacent** pipe DSS unit. Pipe D DSS unit can have additional 4PPC interface to support Pipe Macros. Recommendation is to connect only Pipe A/B/C interface.
Uncompressed joiner must not be enabled when big/ultra joiners are enabled on the same pipe and vice versa.

Value	Name
0b	not secondary
1b	secondary

PIPE_DSS_CTL1

	19:16	**Overlap** Access: R/W **Description** MIPI use case (mainly dual link mode): This field specifies the number of pixels of overlap. 1 to 15 = valid integer number of overlap pixels. 0 = Sink device requires no overlap pixels. eDP use case: This field specifies the number of overlap pixels the sink device uses in the active data. 1 to 8 = valid integer number of overlap pixels. 0 = Sink device requires no overlap pixels.
	15:12	**Reserved** Access: RO Format: MBZ
	11:0	**Left DL buffer Target Depth** Access: R/W This field indicates the number of pixels to hold in the secondary link buffer before enabling the timing generator, so the Primary and Secondary client controllers are in sync. Valid only when operating in front back dual link mode. Value should only be programmed for the Secondary client controller. If bit 31 is set then the target for the Secondary controller must be non-zero. Maximum value is 1440 decimal.

PIPE_DSS_CTL2

PIPE_DSS_CTL2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	78004h-78007h
Name:	PIPE DSS Control 2
ShortName:	PIPE_DSS_CTL2_PA
Reset:	soft

Address:	78204h-78207h
Name:	PIPE DSS Control 2
ShortName:	PIPE_DSS_CTL2_PB
Reset:	soft

Address:	78404h-78407h
Name:	PIPE DSS Control 2
ShortName:	PIPE_DSS_CTL2_PC
Reset:	soft

Address:	78604h-78607h
Name:	PIPE DSS Control 2
ShortName:	PIPE_DSS_CTL2_PD
Reset:	soft

Display stream splitter

DWord	Bit	Description
0	31	**Left Branch VDSC Enable** Access: R/W This bit enables Display Stream Compression on left branch. Its double buffered to rising edge of vblank. Restriction: Display stream compression is supported for pipe active sizes up to 4096 pixels. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30	**Reserved** Access: RO Format: MBZ

PIPE_DSS_CTL2

29:27	**Reserved**
	Access: RO
	Format: MBZ
26	**Spare 26**
	Access: R/W
25	**Spare 25**
	Access: R/W
24	**Spare 24**
	Access: R/W
23	**Reserved**
	Access: RO
	Format: MBZ
22:19	**Reserved**
	Access: RO
	Format: MBZ
18:17	**Reserved**
	Access: RO
	Format: MBZ
16	**Reserved**
	Access: RO
	Format: MBZ
15	**Right Branch VDSC Enable**
	Access: R/W
	Display stream compression on right branch enable/disable. It is double buffered on rising edge of vblank.
	Restriction: Display stream compression is supported for pipe active sizes up to 4096 pixels.

Value	Name
0b	Disable
1b	Enable

14	**Spare 14**
	Access: R/W
13	**Spare 13**
	Access: R/W
12	**Spare 12**
	Access: R/W

PIPE_DSS_CTL2		
	11:0	**Right DL Buffer Target Depth** Access: R/W This field indicates the number of pixels to hold in the secondary link buffer before enabling the timing generator, so the Primary and Secondary client controllers are in sync. Valid only when operating in front back dual link mode. Value should only be programmed for the Secondary controller. If bit 31 is set then the target for the Secondary controller must be non-zero. Maximum value is 1440 decimal. Default is 0.

PIPE_FLIPCNT

PIPE_FLIPCNT	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70044h-70047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_A
Reset:	soft
Address:	71044h-71047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_B
Reset:	soft
Address:	72044h-72047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_C
Reset:	soft
Address:	73044h-73047h
Name:	Pipe Flip Count
ShortName:	PIPE_FLIPCNT_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Flip Counter** Access: R/W This field provides read back of the display pipe flip counter. The counter increments on the start of each flip to the selected plane of this pipe. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane 1 surface address. It rolls over back to 0 after (2^32)-1 flips. Pipe flip counter is restricted to one plane at a time. The plane select is programmed in PIPE_MISC2->Flip Timestamp Plane Select.

PIPE_FLIPDONETMSTMP

PIPE_FLIPDONETMSTMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70054h-70057h
Name:	Pipe Flip Done Time Stamp
ShortName:	PIPE_FLIPDONETMSTMP_A
Reset:	soft
Address:	71054h-71057h
Name:	Pipe Flip Done Time Stamp
ShortName:	PIPE_FLIPDONETMSTMP_B
Reset:	soft
Address:	72054h-72057h
Name:	Pipe Flip Done Time Stamp
ShortName:	PIPE_FLIPDONETMSTMP_C
Reset:	soft
Address:	73054h-73057h
Name:	Pipe Flip Done Time Stamp
ShortName:	PIPE_FLIPDONETMSTMP_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Flip Done Time Stamp** Access: R/W This field provides read back of the display pipe flip done time stamp. The time stamp value is sampled when hardware latches on to the new surface and the flip done gets sent. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes to the plane. The TIMESTAMP_CTR register has the current time stamp value. Flip time stamp sampling is restricted to one plane at a time. The plane select is programmed in PIPE_MISC2->Flip Timestamp Plane Select.

PIPE_FLIPTMSTMP

PIPE_FLIPTMSTMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7004Ch-7004Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_A
Reset:	soft
Address:	7104Ch-7104Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_B
Reset:	soft
Address:	7204Ch-7204Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_C
Reset:	soft
Address:	7304Ch-7304Fh
Name:	Pipe Flip Time Stamp
ShortName:	PIPE_FLIPTMSTMP_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Flip Time Stamp** Access: R/W This field provides read back of the display pipe flip time stamp. The time stamp value is sampled on the start of each flip. The start of flip is when the plane surface address is updated, not when the flip completes. The flip can be through command streamer asynchronous and synchronous flips or MMIO writes. The TIMESTAMP_CTR register has the current time stamp value. Writes to this register will overwrite and update the time stamp value. Flip time stamp sampling is restricted to one plane at a time. The plane select is programmed in PIPE_MISC2->Flip Timestamp Plane Select.

PIPE_FRMCNT

PIPE_FRMCNT	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70040h-70043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_A
Reset:	soft
Address:	71040h-71043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_B
Reset:	soft
Address:	72040h-72043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_C
Reset:	soft
Address:	73040h-73043h
Name:	Pipe Frame Count
ShortName:	PIPE_FRMCNT_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Frame Counter** Access: R/W Provides read back of the display pipe frame counter. This counter increments on every start of vertical blank and rolls over back to 0 after (2^32)-1 frames.

PIPE_FRMTMSTMP

PIPE_FRMTMSTMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70048h-7004Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_A
Reset:	soft
Address:	71048h-7104Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_B
Reset:	soft
Address:	72048h-7204Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_C
Reset:	soft
Address:	73048h-7304Bh
Name:	Pipe Frame Time Stamp
ShortName:	PIPE_FRMTMSTMP_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Pipe Frame Time Stamp** Access: R/W This field provides read back of the display pipe frame time stamp. The time stamp value is sampled at every start of vertical blank. The TIMESTAMP_CTR register has the current time stamp value. Writes to this register will overwrite and update the time stamp value.

PIPE_ISOCREQ

PIPE_ISOCREQ - PIPE_ISOCREQ

Register Space:	MMIO: 0/2/0
Size (in bits):	64
Address:	70010h-70017h
Name:	Pipe Isoch Request
ShortName:	PIPE_ISOCREQ_A
Reset:	soft
Address:	71010h-71017h
Name:	Pipe Isoch Request
ShortName:	PIPE_ISOCREQ_B
Reset:	soft
Address:	72010h-72017h
Name:	Pipe Isoch Request
ShortName:	PIPE_ISOCREQ_C
Reset:	soft
Address:	73010h-73017h
Name:	Pipe Isoch Request
ShortName:	PIPE_ISOCREQ_D
Reset:	soft

When enabled, the write to DWord 1 (higher address DWord) of this register triggers an IsocReq to be sent with the last written values from both DWords.

DWord	Bit	Description
0	31:16	**LTR** Access: R/W This field specifies the latency tolerance (LTR) for this pipe in microseconds.
	15:0	**Bandwidth** Access: R/W This field specifies the bandwidth requirement for this pipe in multiples of 100 MB/s.
1	31	**Enable** Access: R/W This field enables IsocReq to be sent when DWord 1 of this register is written. Value: 1b — Name: Enable Value: 0b — Name: Disable

PIPE_ISOCREQ - PIPE_ISOCREQ		
	30:8	**Reserved** Access: RO Format: MBZ
	7:0	**Delay** Access: R/W This field specifies the downwards transition delay for this pipe in milliseconds.

PIPE_ISOCREQ_OFFSET

PIPE_ISOCREQ_OFFSET - PIPE_ISOCREQ_OFFSET

Register Space:	MMIO: 0/2/0
Size (in bits):	64

Address:	70018h-7001Fh
Name:	Pipe Isoch Offset addition
ShortName:	PIPE_ISOCREQ_OFFSET_A
Reset:	soft

Address:	71018h-7101Fh
Name:	Pipe Isoch Offset addition
ShortName:	PIPE_ISOCREQ_OFFSET_B
Reset:	soft

Address:	72018h-7201Fh
Name:	Pipe Isoch Offset addition
ShortName:	PIPE_ISOCREQ_OFFSET_C
Reset:	soft

Address:	73018h-7301Fh
Name:	Pipe Isoch Offset addition
ShortName:	PIPE_ISOCREQ_OFFSET_D
Reset:	soft

The values programmed in this register will added as offsets to the LTR, BW and Delay. SW must ensure to clear these registers if no offset is desired to be added.
For example, if LTR offset is programmed to 0x0100 in this register, then this value is added to the LTR value programmed in PIPE_ISOCREQ.

DWord	Bit	Description
0	31:16	**LTR offset** Access: R/W This field specifies the latency tolerance (LTR) offset to be added to LTR value in PIPE_ISOCREQ for this pipe in microseconds.
	15:0	**Bandwidth offset** Access: R/W This field specifies the bandwidth requirement offset to be addedto BW value in the PIPE_ISOCREQ register
1	31:8	**Reserved** Access: RO Format: MBZ

PIPE_ISOCREQ_OFFSET - PIPE_ISOCREQ_OFFSET		
	7:0	**Delay Offset** Access: R/W This field specifies the offset to be added to the downwards transition delay programmed in the PIPE_ISOCREQ.

PIPE_MISC

PIPE_MISC

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled

Address:	70030h-70033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_A
Reset:	soft

Address:	71030h-71033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_B
Reset:	soft

Address:	72030h-72033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_C
Reset:	soft

Address:	73030h-73033h
Name:	Pipe Miscellaneous
ShortName:	PIPE_MISC_D
Reset:	soft

DWord	Bit	Description
0	31:30	**Stereo Mask Pipe Int** Access: Double Buffered This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in interrupts during stereo 3D mode. **Value / Name / Description** 00b / Mask None / No masking. Report both the left and right eye vertical events. 01b / Mask Left / Mask the left eye vertical events. Only report right eye events. 10b / Mask Right / Mask the right eye vertical events. Only report left eye events. 11b / Reserved / Reserved **Restriction** This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.

PIPE_MISC

29:28 **Stereo Mask Pipe Render**

Access:	Double Buffered

This field controls which pipe vertical timing (vertical blank, scan line, and vertical sync) events will be reported in render responses during stereo 3D mode.

Value	Name	Description
00b	Mask None	No masking. Report both the left and right eye vertical events.
01b	Mask Left	Mask the left eye vertical events. Only report right eye events.
10b	Mask Right	Mask the right eye vertical events. Only report left eye events.
11b	Reserved	Reserved

Restriction
This field must be programmed prior to enabling stereo 3D mode and must not be changed while stereo 3D is enabled. In the stacked frame mode the vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame, so masking may cause unexpected behavior for those events.

27 **YUV420 Enable**

Access:	Double Buffered

This field enables YUV420 output from this pipe. This is only for use with HDMI and DP.

Value	Name
0b	Disable
1b	Enable

Restriction
This field must be programmed prior to enabling the transcoder attached to this pipe.

26 **YUV420 Mode**

Access:	Double Buffered

This field specifies the mode in which YUV420 pixels are generated by this pipe.

Value	Name	Description
0b	Bypass	[] Bypass mode defeatured. Only full blend mode supported.
1b	Full blend	

25 **Pipe Gamma Input Clamp Disable**

Access:	Double Buffered

This field controls the pipe post csc gamma input clamp operation. When this bit is set to 0b the negative pixel values get clamped to zero at the gamma input.

Value	Name
0b	Enable **[Default]**
1b	Disable

PIPE_MISC

24 **Allow DB Stall**

Access:	R/W

This field controls whether double buffer updates are allowed to be stalled for the double buffered pipe registers.

Value	Name
0b	Not Allowed
1b	Allowed **[Default]**

23 **HDR Mode**

Access:	Double Buffered

This field enables the HDR mode, allowing for higher precision output from the HDR supporting planes and bypassing the SDR planes in blending.

In addition to setting bit 8 of this register (Pixel Rounding),this bit must be set to 1b to passthrough the frame buffer pixels unmodified across the pipe.

Value	Name
0b	Disable
1b	Enable

22 **Change Mask for LDPST**

Access:	Double Buffered

This field controls the change tracking for the LACE. Change tracking can be used by PSR/SRD and WD

Value	Name
0b	Not Masked
1b	Masked

21 **Change Mask for Register Write**

Access:	Double Buffered

This field controls change tracking for the pipe register write. Change tracking can be used by PSR/SRD and WD.

Value	Name
0b	Not Masked
1b	Masked

20 **Change Mask for Vblank Vsync Int**

Access:	Double Buffered

This field controls change tracking for the vblank or vsync interrupt enable. Change tracking can be used by PSR/SRD and WD.

Value	Name
0b	Not Masked
1b	Masked

PIPE_MISC

19 Reserved

Access:	Double Buffered

18 Reserved

Access:	Double Buffered

17 Reserved

Access:	Double Buffered

16 Reserved

Access:	Double Buffered

15:14 Rotation Info

Access:	Double Buffered

This field indicates to internal KVMR screen capture that the display has been rotated through software or hardware rotation. Select the closest value if the rotation is not an exact multiple of 90 degrees. Hardware rotation of the display output is controlled through the plane control registers, not through this field.

Value	Name	Description
00b	None	No rotation on this pipe
01b	90	90 degree rotation on this pipe
10b	180	180 degree rotation on this pipe
11b	270	270 degree rotation on this pipe

Restriction
This field must be programmed in order for internal KVMR screen capture to work correctly when display is rotated by software or hardware.

13 Reserved

Access:	RO
Format:	MBZ

12 OLED Compensation

Access:	Double Buffered

This field enables the OLED compensation on the pipe. When this bit is set, plane 5 is used as the OLED compensation plane with up to 10 bits per channel precision. OLED compensation must be used only when the pipe is configured to output RGB format.
The OLED compensation plane size must be same as the pipe active size.

Value	Name
0b	Disable
1b	Enable

PIPE_MISC

11 Pipe output color space select

Access:	Double Buffered

This field indicates the output color space. This field affects the values of the pipe border and some capture functions. This field does not affect the planes, pipe CSC, or ports.

Value	Name
0b	RGB
1b	YUV

Restriction
This field must be set to match the color space that will be output from the pipe CSC or output from the planes if they pipe CSC is bypassed.

10 xvYCC Color Range Limit

Access:	Double Buffered

This field limits the color range of the pipe output to 1 to 254 for 8-bit components, 4 to 1019 for 10bit components, and 16 to 4079 for 12-bit components. Values outside of the range will be clamped to fit within the range.

Value	Name	Description
0b	Full	Do not limit the range
1b	Limit	Limit range

9 Pixel Extension

Access:	Double Buffered

This field controls how the pixel extension is handled in the pipe.
In scenarios where the frame buffers bpc is larger or equal to the port output bpc, this bit may be programmed to 'Zero Extend'.

Value	Name
0b	MSB Extend **[Default]**
1b	Zero Extend

8 Pixel Rounding

Access:	Double Buffered

This field controls the pixel rounding at the end of the pipe.
This bit must be set to 1b to passthrough the frame buffer pixels unmodified across the pipe.

Value	Name
0b	Round Up **[Default]**
1b	Truncate

PIPE_MISC

7:5 Dithering BPC

Access:	Double Buffered

This field selects the number of bits per color to be used in dithering.

Value	Name	Description
000b	8 bpc	8 bits per color
001b	10 bpc	10 bits per color
010b	6 bpc	6 bits per color
Others	Reserved	Reserved

Programming Notes
When dithering is enabled, the value selected here should match the bits per color selected in the Transcoder DDI Function Control register attached to this pipe.

4 Dithering enable

Access:	Double Buffered

This field enables dithering.

Value	Name
0b	Disable
1b	Enable

3:2 Dithering type

Access:	Double Buffered

This field selects the dithering type.

Value	Name	Description
00b	Spatial	Spatial
01b	ST1	Spatio-Temporal 1
10b	ST2	Spatio-Temporal 2
11b	Temporal	Temporal

1 Reserved

Access:	RO
Format:	MBZ

0 Reserved

Access:	Double Buffered

PIPE_MISC2

PIPE_MISC2	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled

Address:	7002Ch-7002Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_A
Reset:	soft

Address:	7102Ch-7102Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_B
Reset:	soft

Address:	7202Ch-7202Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_C
Reset:	soft

Address:	7302Ch-7302Fh
Name:	Pipe Miscellaneous 2
ShortName:	PIPE_MISC2_D
Reset:	soft

There is one instance of this register per pipe.

DWord	Bit	Description
0	31:24	**Underrun bubble counter** Default Value: 00000000b Access: Double Buffered **Description** This field controls the number of bubbles (clocks without valid pixel data) that the pipe underrun recovery logic will ignore at the start of a line. This is used to avoid false underrun detection and recovery with features that generate small bubbles. HW will ignore bubbles from end of line until the programmable number of valid pixels specified by this counter value. Beyond this count value, underrun events will be flagged.

When underrun recovery is enabled, this field must be programmed for features that create bubbles

- Pipe or plane scaling = 80 pixels
- Chroma Up-Sampling (CUS) without pipe scaling = 20 pixels
- FBC without pipe scaling = 20 pixels
- Pipe joining with seam pixels being dropped = number of dropped pixels from PIPE_SEAM_EXCESS
    - Add to the pixels for other features.

The Scalers are downstream of the CUS/FBC, so any bubbles from the CUS/FBC will be absorbed by the Scaler if scaling is enabled (i.e. those bubbles are not additive with scaler and the bubbles between lines from the Scaler takes precedence when programming this field).

Pipe underrun recovery is disabled by setting bit 30 of the register at the following offsets

- Pipe A: 0x70038
- Pipe B: 0x71038
- Pipe C: 0x72038
- Pipe D: 0x73038

Underrun recovery is not supported. Do not enable it.

23:20 **TLB Throttle**

Default Value:	8
Access:	Double Buffered

This field specifies how often the TLB requests are sent. If the programmed value is x, TLBs requests are sent once in x clocks if there are competing data requests.

19 **Underrun Manual Pixel Override**

Access:	Double Buffered

Enable/Disable manual pixel override

Value	Name
0b	HW Override Pixel
1b	SW (manual) Override Pixel

18:16 **Underrun Replacement Pixel Value**

Access:	Double Buffered

Value	Name	Description
000b	All Color Channels 0 **[Default]**	All color channels forced to all 0's value.
001b	Red and Green 0 Blue 1	Red and Green color channels forced to all 0's value. Blue forced to all 1's.
010b	Red and Blue 0 Green 1	Red and Blue color channels forced to all 0's value. Green forced to all 1's.

PIPE_MISC2

011b	Red 0 Green and Blue 1	Red color channel forced to all 0's value. Green and Blue forced to all 1's.
100b	Green and Blue 0 Red 1	Green and Blue color channels forced to all 0's value. Red forced to all 1's.
101b	Green 0 Red and Blue 1	Green color channel forced to all 0's value. Red and Blue forced to all 1's.
110b	Red and Green 1 Blue 0	Red and Green color channels forced to all 1's value. Blue forced to all 0's.
111b	All Color Channels 1	Red, Green and Blue color channels forced to all 1's value.

15:12 **IPC Demote Req Chunk Size**

Default Value:	8
Access:	Double Buffered

This field limits the request burst sizes while in IPC demote. A value of 0 disables the inflight limit.

11 **YUV 422 mode**

Access:	Double Buffered

YUV 422 mode enable in DP and HDMI modes. YUV 420 enable bit in PIPE_MISC should not be set when this is set.

Value	Name
0b	Disable
1b	Enable

Restriction
This field must be programmed prior to enabling the transcoder attached to this pipe.

10:9 **Reserved**

Access:	RO
Format:	MBZ

8 **ASFU Flip exception**

Access:	Double Buffered

Value	Name	Description
1b	mask	Add exception for Flip for global register update event and Pipe register update event.
0b	No mask	Do not add exception for Flip for global register update event and Pipe register update event.

7 **Reserved**

Access:	RO
Format:	MBZ

PIPE_MISC2

	6:4	**Scanline Plane Select** Access: Double Buffered This field specifies the plane for which scanline compare fetch line is captured. A programmed value of 0b selects plane 1. **Value** / **Name** [0h-6h]
	3	**Reserved** Access: RO Format: MBZ
	2:0	**Flip Info Plane Select** Access: Double Buffered This field specifies the plane for which flip information is captured. A programmed value of 0b selects plane 1. **Value** / **Name** [0h-6h]

PIPE_MISC3

PIPE_MISC3	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	7005Ch-7005Fh
Name:	Pipe Miscellaneous 3
ShortName:	PIPE_MISC3_A
Reset:	soft
Address:	7105Ch-7105Fh
Name:	Pipe Miscellaneous 3
ShortName:	PIPE_MISC3_B
Reset:	soft
Address:	7205Ch-7205Fh
Name:	Pipe Miscellaneous 3
ShortName:	PIPE_MISC3_C
Reset:	soft
Address:	7305Ch-7305Fh
Name:	Pipe Miscellaneous 3
ShortName:	PIPE_MISC3_D
Reset:	soft
There is one instance of this register per pipe.	

DWord	Bit	Description
0	31:16	**Reserved** Access: Double Buffered
	15:0	**Highest recovery counter status** Access: R/WC This field indicates pixel underrun value from last failure.

PIPE_MISC4

PIPE_MISC4	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	70060h-70063h
Name:	Pipe Miscellaneous 4
ShortName:	PIPE_MISC4_A
Reset:	soft
Address:	71060h-71063h
Name:	Pipe Miscellaneous 4
ShortName:	PIPE_MISC4_B
Reset:	soft
Address:	72060h-72063h
Name:	Pipe Miscellaneous 4
ShortName:	PIPE_MISC4_C
Reset:	soft
Address:	73060h-73063h
Name:	Pipe Miscellaneous 4
ShortName:	PIPE_MISC4_D
Reset:	soft

There is one instance of this register per pipe.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:24	**Reserved** Access: RO Format: MBZ
	23:17	**Left filter coeff** Access: R/W This field indicates left filter coefficient for YUV 422 subsampling. Valid range for the coefficient is [0-64]. The sum of left, center and right filter coefficients must be 64.

PIPE_MISC4

Value	Name
0010000b	**[Default]**
0000000b	

16	**Reserved**
Access:	RO
Format:	MBZ

15:9	**Center filter coeff**
Access:	R/W

This field indicates center filter coefficient for YUV 422 subsampling.
Valid range for the coefficient is [0-64].
The sum of left, center and right filter coefficients must be 64.

Value	Name
0100000b	**[Default]**
1000000b	

8	**Reserved**
Access:	RO
Format:	MBZ

7:1	**Right filter coeff**
Access:	R/W

This field indicates right filter coefficient for YUV 422 subsampling.
Valid range for the coefficient is [0-64].
The sum of left, center and right filter coefficients must be 64.

Value	Name
0010000b	**[Default]**
0000000b	

0	**Reserved**
Access:	RO
Format:	MBZ

PIPE_SCANLINE

PIPE_SCANLINE

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	70000h-70003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_A
Reset:	soft
Address:	71000h-71003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_B
Reset:	soft
Address:	72000h-72003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_C
Reset:	soft
Address:	73000h-73003h
Name:	Pipe Scan Line
ShortName:	PIPE_SCANLINE_D
Reset:	soft

This register enables the read back of the pipe vertical line counter. The value increments at the leading edge of HSYNC. The value resets to line zero at the first active line of the display. In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.

DWord	Bit	Description
0	31	**Current Field** Access: RO This is an indication of the current display field. Value / Name / Description: 0b / Odd / First field (odd field) 1b / Even / Second field (even field)
	30:20	**Reserved** Access: RO Format: MBZ
	19:0	**Line Counter for Display** Access: RO

PIPE_SCANLINE		
		This is an indication of the current display scan line. **Programming Notes** The line count value is from the display output timing generator, representing the scan line currently being output to a receiver. Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.

PIPE_SCANLINECOMP

PIPE_SCANLINECOMP	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70004h-70007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_A
Reset:	soft
Address:	71004h-71007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_B
Reset:	soft
Address:	72004h-72007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_C
Reset:	soft
Address:	73004h-73007h
Name:	Pipe Scan Line Compare
ShortName:	PIPE_SCANLINECOMP_D
Reset:	soft

This register is used to initiate a display scan line compare. This MMIO driven scan line compare cannot be used at the same time as the command streamer driven scan line compare on the same pipe. When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line >= start scan line) and the end scan line value (current scan line <= end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing. The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are configured for that. The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0. The programmable range can include the vertical blank. In interlaced display timings, the current scan line is the current line of the current interlaced field. Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register. There is one instance of this register per pipe.

Restriction
A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value.When using LRI care must be taken to follow all

PIPE_SCANLINECOMP

the programming rules for LRI targeting the display engine.

DWord	Bit	Description
0	31	**Initiate Compare** Access: R/W This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing. **Value** / **Name** 0b: Do nothing 1b: Initiate compare **Restriction** Do not write this register again until after any previous scan line compare has completed.
	30	**Inclusive Exclusive Select** Access: R/W This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window. **Value** / **Name** / **Description** 0b / Exclusive / Exclusive mode: trigger scan line event when inside the scan line window 1b / Inclusive / Inclusive mode: trigger scan line event when outside the scan line window
	29	**Counter Select** Access: R/W This field selects whether the scan line compare is done using the pipe timing generator scanline counter or a plane scanline counter. The pipe timing generator counts the scanlines being output from display. The plane counts the scan lines being fetched from the frame buffer. **Value** / **Name** / **Description** 0b / Timing generator / Use the scanline count from the pipe timing generator 1b / Plane / Use the scanline count from plane selected in PIPE_MISC2. **Programming Notes** Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.
	28:16	**Start Scan Line** Access: R/W This field specifies the starting scan line number of the scan line window.

PIPE_SCANLINECOMP

	15	**Render Response Destination** Access: R/W This bit indicates what destination to send the scan line event render response to. Value / Name / Description 0b / CS / Send scan line event response to CS 1b / BCS / Send scan line event response to BCS
	14:13	**Reserved** Access: RO Format: MBZ
	12:0	**End Scan Line** Access: R/W This field specifies the ending scan line number of the scan line window.

PIPE_SEAM_EXCESS

PIPE_SEAM_EXCESS - PIPE_SEAM_EXCESS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank OR pipe disabled
Address:	60020h-60023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_A
Reset:	soft
Address:	61020h-61023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_B
Reset:	soft
Address:	62020h-62023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_C
Reset:	soft
Address:	63020h-63023h
Name:	Pipe Seam Excess
ShortName:	PIPE_SEAM_EXCESS_D
Reset:	soft

This register defines the number of excess pixels within the Pipe window (on the right or left) that the Scaler will need to remove from the post scaled image.
When an image is split across two Pipes, scaled, and then joined at the Port, the Scalers within each Pipe will operate on a split image that contains overlap pixels around where the final seam will be to facilitate a seamless join at the Port. For example, if the left portion of an image is being scaled in Pipe A and the right portion of the image is being scaled in Pipe B, then there will be an excess number of pixels (i.e. overlap pixels) on the right side of the Pipe A image and an excess number of pixels on the left side of the Pipe B image. The overlap pixels of the window within each of the Pipes need to be dropped by the Scaler before they are delivered to the Port.
Notes:

1. Dropping of the overlap/excess pixels is done at the very end of the Pipe within the Scaler regardless of whether a Scaler is bound to the Pipe, or not.
2. The values programmed within this register are one-based (i.e., a programming of 1 equals 1 pixel of excess)
3. The values programmed within this register will be added to the Horizontal Active programming of the TRANS_HTOTAL register of the port bound to this pipe. I.e., the pipe will see a Horizontal size equal to Horizontal Active + Left Excess Amount + Right Excess Amount

PIPE_SEAM_EXCESS - PIPE_SEAM_EXCESS

Restriction:

1. The number of excess pixels cannot exceed the size of the horizontal blank, otherwise there will not be enough time to throw them away before starting the next line and the image will be corrupted
2. Pillarbox boarders must be even
3. The source size on each pipe, including pre-scale excess, must be a multiple of 2. When the Pipe output format is YUV 420 with full blend, the source size is required to be a multiple of 4.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Right Excess Amount** Access: Double Buffered This field defines the number of excess pixels to drop, if any, on the right side of the Pipe window
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Left Excess Amount** Access: Double Buffered This field defines the number of excess pixels to drop, if any, on the left side of the Pipe window

PIPE_SRCSZ

PIPE_SRCSZ	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank

Address:	6001Ch-6001Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_A
Reset:	soft

Address:	6101Ch-6101Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_B
Reset:	soft

Address:	6201Ch-6201Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_C
Reset:	soft

Address:	6301Ch-6301Fh
Name:	Pipe Source Image Size
ShortName:	PIPE_SRCSZ_D
Reset:	soft

There is one instance of this register for each pipe.

Programming Notes

In VGA display mode, this register is ignored and the VGA size from the VGA registers is used instead.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Horizontal Source Size** Access: Double Buffered This field specifies Horizontal Source Size. This determines the horizontal size of the image created by the display planes. This field is programmed to the number of pixels desired minus one. **Restriction** • This register must always be programmed to the same value as the Horizontal Active, except when panel fitting is enabled or DSC pixel replication is enabled.

PIPE_SRCSZ

		• Refer to PS_CTRL for size restrictions when panel fitting is enabled. • Horizontal source size must always be even. The programmed value must be odd.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Vertical Source Size** Access: Double Buffered This field specifies Vertical Source Size. This determines the vertical size of the image created by the display planes. This field is programmed to the number of lines desired minus one. **Restriction** Vertical source sizes larger than 4320 lines are not supported. This register must always be programmed to the same value as the Vertical Active, except when panel fitting is enabled. Refer to PS_CTRL for size restrictions when panel fitting is enabled.

PIPE_STATUS

PIPE_STATUS	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
CrashLogSaved:	true
CrashLogPriority:	1
CrashLogVisibility:	public
ExternalLongName:	DE Pipe Status
ExternalDescription:	Display engine pipe status
Address:	70058h-7005Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_A
Reset:	soft
Address:	71058h-7105Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_B
Reset:	soft
Address:	72058h-7205Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_C
Reset:	soft
Address:	73058h-7305Bh
Name:	Pipe Status
ShortName:	PIPE_STATUS_D
Reset:	soft

DWord	Bit	Description
0	31	**Underrun** Access: R/WC This field indicates that there is an underrun on the transcoder attached to this pipe.
	30	**Vblank** Access: R/WC The field is set at the start of the vertical blank of the transcoder attached to this pipe.
	29	**Frame start** Access: R/WC The field is set at the frame start of the transcoder attached to this pipe.

PIPE_STATUS

	28	**Pipe Soft Underrun** Access: R/WC This bit when set indicates that HW is using replacement pixel at underrun locations.
	27	**Pipe Hard Underrun** Access: R/WC This bit when set indicates that the HW is repeating the last valid pixel at underrun locations.
	26	**Port underrun** Access: R/WC This bit when set indicates that the pipe has sent all the pixels at expected rate but there is an underrun due to logic downstream to the pipes.
	25	**Not Used 25** Access: R/WC
	24	**Not Used 24** Access: R/WC
	23	**Not Used 23** Access: R/WC
	22	**Not Used 22** Access: R/WC
	21	**Not Used 21** Access: R/WC
	20	**Not Used 20** Access: R/WC
	19	**Not Used 19** Access: R/WC
	18	**Not Used 18** Access: R/WC
	17	**Not Used 17** Access: R/WC
	16	**Not Used 16** Access: R/WC
	15	**Not Used 15** Access: R/WC
	14	**Not Used 14** Access: R/WC

PIPE_STATUS

	13	**Not Used 13** Access: R/WC
	12	**Not Used 12** Access: R/WC
	11	**Not Used 11** Access: R/WC
	10	**Not Used 10** Access: R/WC
	9	**Not Used 9** Access: R/WC
	8	**Not Used 8** Access: R/WC
	7	**Not Used 7** Access: R/WC
	6	**BW Credits Pending At VBlank** Access: R/WC A '1' indicates that the there are some pending MBUS BW-Credits at the start of VBlank. Sticky bit cleared by a write of '1'
	5	**B Credits Pending At VBlank** Access: R/WC A '1' indicates that the there are some pending MBUS B-Credits at the start of VBlank. Sticky bit cleared by a write of '1'
	4	**A Credits Pending At VBlank** Access: R/WC A '1' indicates that the there are some pending MBUS A-Credits at the start of VBlank. Sticky bit cleared by a write of '1'
	3	**Not Used 3** Access: R/WC
	2	**Not used 2** Access: R/WC
	1	**Valid Block At FrameStart** Access: R/WC A '1' indicates that a valid block is still present in Display Buffer at frame start. Sticky bit cleared by a write of '1'.
	0	**Valid Block Overwritten**

PIPE_STATUS			
		Access:	R/WC
		A '1' indicates that a valid block in Display Buffer was overwritten. Sticky bit cleared by a write of '1'.	

PIPEDMC_CONTROL

PIPEDMC_CONTROL - PIPEDMC_CONTROL

Register Space:	MMIO: 0/2/0
Size (in bits):	32

Address:	45250h-45253h
Name:	Pipe DMC Control
ShortName:	PIPEDMC_CONTROL_A
Reset:	soft

Address:	45254h-45257h
Name:	Pipe DMC Control
ShortName:	PIPEDMC_CONTROL_B
Reset:	soft

Address:	45258h-4525Bh
Name:	Pipe DMC Control
ShortName:	PIPEDMC_CONTROL_C
Reset:	soft

Address:	4525Ch-4525Fh
Name:	Pipe DMC Control
ShortName:	PIPEDMC_CONTROL_D
Reset:	soft

This Register is to add pipe DMC enable. To use pipeDMC driver must enable pipeDMC first.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**pipedmc_enable** Access: R/W Setting this bit enables the pipeDMC.

Pixel Shader Scheduling Mode

PSS_MODE - Pixel Shader Scheduling Mode

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	07038h
Name:	Pixel Shader Scheduling Mode
ShortName:	PSS_MODE

Mode registers for Pixel Shader Scheduling.

DWord	Bit	Description
0	31:16	**Mask** Access: WO _Custom_GTIReset: DEV Must be set to modify corresponding bit in Bits 15:0 (All implemented bits)
	15:14	**8x8 History buffer size** Access: R/W Format: U2 _Custom_GTIReset: DEV Selects the depth of the 8x8 history buffer and if recent filtering is enabled. When recent filtering is enabled, an 8x8 will not be added to the history buffer if it was recently added to the history buffer. Value / Name: 0h: Full Size with Recent Filtering Enabled **[Default]** 1h: Half Size with Recent Filtering Enabled 2h: Quarter Size with Recent Filtering Enabled 3h: Full Size with Recent Filtering Disabled
	13:10	**Maximum Allowed PS Thread Dependencies** Default Value: 8h Access: R/W Format: U4 _Custom_GTIReset: DEV Sets the maximum number of dependencies that a pixel shader thread can have. If a thread requires more than this number, thread dispatch will be stalled until enough threads that this thread is dependent on have retired. Since maximum number of dependencies in a Pixel Shader is 8 (for fused-SIMD16, corresponding to 8 2X2 pixel block; fused-SIMD32 corresponding to 8 4x2 pixel blocks), programming a value higher than 0X8 is illegal. If HW chooses to launch lower SIMD thread e.g. fused-SIMD8, it will not have more than 4 dependencies. Hence, programming 0x8 guarantees maximum dependencies for all SIMD width dispatches.

PSS_MODE - Pixel Shader Scheduling Mode

9 — 3D Scoreboard Address XOR Disable

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Enabled **[Default]**	3D Scoreboard Address calculation includes XOR of higher bits
1h	Disabled	3D Scoreboard Address calculation based on lower address bits only

8 — Reserved

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

7 — Stalling behavior disable for PS Dispatch for PTBR

Access:	R/W
_Custom_GTIReset:	DEV

This bit, when enabled, allows PS dispatch function to not stall when no TILE ID is free for incoming new tile access under PTBR. Although this behavior is non stalling, it has a potential to reduce number of color pixel blocks from tile cache in certain cases.

Value	Name	Description
0	**[Default]**	This is a default value and default behavior is to have PS dispatch stall when there are no free TILE_IDs available for incoming new access on a new TILE under PTBR.
1		When this bit is set, PS dispatch does not stall for a new incoming tile but simply uses the next TILE_ID without waiting for it to be free. SW should enable this bit if there are perf downsides with stalling behavior and additional discard BW is not significant.

6:5 — Thread Scheduler Mode

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Selects the PSD selection policy

Value	Name	Description
0h	Round-Robin **[Default]**	Scheduler issues grant number of threads to the selected PSD. Once grant has expired it may continue to dispatch grace number of threads as long as they came from the same scheduler event. Once grant duration has expired and current scheduler event will not fit within grace, selected PSD is advanced.

PSS_MODE - Pixel Shader Scheduling Mode

1h	Round-Robin with match	Scheduler issues grant number of threads to the selected PSD. Once grant has expired it may continue to dispatch grace number of threads as long as they came from the same scheduler event or match the history buffer for the selected PSD. Once grant duration has expired and current scheduler event will not fit within grace, selected PSD is advanced.
2h	Dynamic	Scheduler issues grant number of threads to the selected PSD. Once grant has expired it may continue to dispatch grace number of threads as long as they came from the same scheduler event. Once grant duration has expired and current scheduler event will not fit within grace, next selected PSD is based on EU load.
3h	Dynamic with match	Scheduler issues grant number of threads to the selected PSD. Once grant has expired it may continue to dispatch grace number of threads as long as they came from the same scheduler event or match the history buffer for the selected PSD. Once grant duration has expired and current scheduler event will not fit within grace, next selected PSD is based on EU load.

4 **Disable 4x4 schedule optimization**

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

If set, prevent scheduler from attempting to pack 4x4 at SIMD16 alignment.

Value	Name
0h	4x4 packed at SIMD16 alignment if possible **[Default]**
1h	scheduler does not consider 4x4 when packing threads

3 **Disable 4x2 schedule optimization**

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

If set, prevent scheduler from attempting to pack 4x2 at SIMD8 alignment.

Value	Name
0h	4x2 packed at SIMD8 alignment if possible **[Default]**
1h	scheduler does not consider 4x2 when packing threads

2 **Disable fused thread scheduling**

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

If set, scheduler will only populate the first thread of a fused thread. A fused thread will still be dispatched but will only contain a single thread.

PSS_MODE - Pixel Shader Scheduling Mode

Value	Name
0h	Fused thread enabled **[Default]**
1h	Fused thread disabled

1:0 **Limit maximum number of polys per fused-thread**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

Limit the scheduler to pack no more than the indicated number polys into a single fused-thread.

Value	Name
0h	Polys per fused-thread is not limited **[Default]**
1h	Maximum polys per fused-thread limited to 1
2h	Maximum polys per fused-thread limited to 2
3h	Maximum polys per fused-thread limited to 3

Pixel Shader Scheduling Mode 2

PSS_MODE2 - Pixel Shader Scheduling Mode 2

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0703Ch
Name:	Pixel Shader Scheduling Mode
ShortName:	PSS_MODE2

Mode register for Pixel Shader Scheduling.

DWord	Bit	Description
0	31:16	**Mask** Access: WO _Custom_GTIReset: DEV Must be set to modify corresponding bit in Bits 15:0 (All implemented bits)
	15:14	**PSD Dispatch Grant** Access: R/W Format: U2 _Custom_GTIReset: DEV Grant duration is the minimum number of threads the scheduler will dispatch to a PSD before selecting a new PSD Value / Name: 0h: 1_15 **[Default]** 1h: 2_15 2h: 4_15 3h: 6_15
	13:12	**PSD Dispatch Grace** Access: R/W Format: U2 _Custom_GTIReset: DEV Grace duration is the number of threads the scheduler will dispatch to a PSD once the grant duration has expired if scheduled event passes grace conditions (e.g. via scheduler mode) Value / Name: 0h: 0_13 **[Default]** 1h: 2_13 2h: 4_13 3h: 8_13

PSS_MODE2 - Pixel Shader Scheduling Mode 2

11:10 **PSD Perfect Burst**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

When PSD selection policy has independent perfect selector, this setting indicates the maximum number of perfect dispatches (8x8/8x4) to the same PSD due to matching previous perfect (or history buffer if +match scheduling policy)

Value	Name
0h	1_11 **[Default]**
1h	2_11
2h	4_11
3h	8_11

9 **PSD Selector Policy**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Selects if perfect dispatches (8x8/8x4) have independent PSD selection, or if there is a single PSD selector for all threads dispatched.

Value	Name
0h	Unified Selector **[Default]**
1h	Independent Perfect Selector

8 **PS Load Bias match size**

Access:	R/W
_Custom_GTIReset:	DEV

Select the granularity of xy compare for determining if the incoming 8x8 matches history buffer used for **8x8 Match PS Load Bias**.

Value	Name
0h	8x8 **[Default]**
1h	16x16

7:6 **8x8 Match PS Load Bias**

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

When scheduler is in dynamic mode, PSS will create a load imbalance by the selected number of threads when a new 8x8 matches history buffer or any partially collected threads. This will direct matching 8x8 to the same PSD when load is not extremely skewed.

PSS_MODE2 - Pixel Shader Scheduling Mode 2

Value	Name
0h	2_7 **[Default]**
1h	4_7
2h	8_7
3h	0_7

5 **Scoreboard Stall Flush Control**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Start Thread Group **[Default]**	pipe_control with **Stall at Scoreboard** set creates a new thread group instead of stalling at scoreboard. PS threads launched after pipe_control will have sendc dependency to all threads before pipe_control. This is a pipelined flush and will not drain EUs of PS threads.
1h	Scoreboard Stall	pipe_control with **Stall at Scoreboard**set stalls at PSS scoreboard until all previous threads have completed. This will drain EUs of all PS threads.

Programming Notes
Pipe_control with **PS sync stall** set without any other PSS visible flush set (depth/color) replaces **Stall at Scoreboard** in description.

4 **Thread Group Dependency Control**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name
0h	Use 9th dependency to enforce ordering between thread groups. **[Default]**
1h	Perform stall at PSSunit when thread group changes.

3 **Over-subscribe PS thread allocation**

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

Value	Name
0h	Number of enabled threads does not affect PS thread scheduling **[Default]**
1h	Number of PS threads scheduled per-PSD will not exceed number of enabled threads

PSS_MODE2 - Pixel Shader Scheduling Mode 2

2:0 **PS Dispatch Time-out Values**

Access:	R/W
_Custom_GTIReset:	DEV

Valid values other than 111, allow SW to program number of clocks PS dispatch function wait to combine fuse thread sequence (aka bundle).
Setting 111 disables the time-out mechanism and will wait indefinitely for an event to end the collection of pixels.

Value	Name	Description	Programming Notes
0h	32_2	PS dispatch function waits for 32 clocks for gathering more pixels in the current bundle.	
1h	64	PS dispatch function waits for 64 clocks for gathering more pixels in the current bundle.	
2h	128	PS dispatch function waits for 128 clocks for gathering more pixels in the current bundle.	
3h	256	PS dispatch function waits for 256 clocks for gathering more pixels in the current bundle.	
4h	512	PS dispatch function waits for 512 clocks for gathering more pixels in the current bundle.	
5h	1024	PS dispatch function waits for 1024 clocks for gathering more pixels in the current bundle.	
6h	2048 **[Default]**	PS dispatch function waits for 2048 clocks for gathering more pixels in the current bundle.	
7h		PSD waits indefinitely to assemble a bundle before dispatching a PS.	This value may not be programmed if non-promoted depth or stencil is enabled.

Pixel Shader Scheduling Mode 3

PSS_MODE3 - Pixel Shader Scheduling Mode 3

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	07700h
Name:	Pixel Shader Scheduling Mode
ShortName:	PSS_MODE3

Mode register for Pixel Shader Scheduling.

DWord	Bit	Description
0	31:16	**Mask** Access: WO _Custom_GTIReset: DEV Must be set to modify corresponding bit in Bits 15:0 (All implemented bits)
	15:9	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	8	**Force Aligned** Access: R/W Format: Disable _Custom_GTIReset: DEV Value / Name / Description: 0h / Normal **[Default]** / An 8x8 that is eligible for aligned, may have its DQs scheduled via free/oldest. 1h / Force Aligned Dispatch / An 8x8 that is eligible for aligned+ scheduling will not have its DQs selected for free/oldest.
	7	**Disabled Perfect Scheduler** Access: R/W Format: Disable _Custom_GTIReset: DEV Value / Name / Description: 0h / Perfect Scheduler Enabled **[Default]** / 8x8 that are 8 or 16 quads may be dispatch around the partial thread are dispatched as the minimum number of threads. 1h / Perfect Scheduler Disabled / Perfect threads are not dispatched.

PSS_MODE3 - Pixel Shader Scheduling Mode 3

6 Disabled Preferred Scheduler

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Preferred Scheduler Enabled **[Default]**	Preferred 8x8 is an aligned 8x8 that does not leave a partial thread after being scheduled.
1h	Preferred Scheduler Disabled	Preferred 8x8 are not selected.

5 Disabled Aligned Scheduler

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Aligned Scheduler Enabled **[Default]**	8x8 that are two or more quads may be scheduled as an entire 8x8 to combine with the partial thread
1h	Aligned Scheduler Disabled	Aligned 8x8 are not selected.

4 Disabled Oldest Scheduler

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Oldest Scheduler Enabled **[Default]**	Elevate priority of the oldest 8x8 in the future queue when Out-of-Order Age counter reaches max
1h	Oldest Scheduler Disabled	Oldest 8x8 in future queue is never elevated in priority.

3:2 Out-of-Order Age Counter Max

Access:	R/W
Format:	U2
_Custom_GTIReset:	DEV

The number of scheduler events that are allowed to go around the oldest 8x8 before oldest 8x8 is elevated to highest priority.

Value	Name
0h	4_3 **[Default]**
1h	8_3

PSS_MODE3 - Pixel Shader Scheduling Mode 3

		2h: 1_3 3h: 2_3
	1:0	**Future Queue Size** Access: R/W Format: U2 _Custom_GTIReset: DEV Set the number of future queue entries that are eligible for scheduling. 0h: 4_1 **[Default]** 1h: 1_1 2h: 2_1 3h: 3_1

Pixel Shader Scheduling Mode 4

PSS_MODE4 - Pixel Shader Scheduling Mode 4

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	07704h
Name:	Pixel Shader Scheduling Mode
ShortName:	PSS_MODE4

Mode register for Pixel Shader Scheduling.

DWord	Bit	Description
0	31:16	**Mask** Access: WO _Custom_GTIReset: DEV Must be set to modify corresponding bit in Bits 15:0 (All implemented bits)
	15:7	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	6	**Enable Extended Coarse Pixel Sizes** Access: R/W Format: Enable _Custom_GTIReset: DEV Hardware supports all Coarse pixel sizes up to 16 samples per-CP. The VRS spec does not include some CPsizes. This bit allows the hardware to support the CPsizes beyond the VRS spec.
	5	**Enable Almost Perfect** Access: R/W Format: Enable _Custom_GTIReset: DEV When Simple Shader is set, almost_perfect is enabled. When simple shader is not set, this bit may be used to enabled almost_perfect.

Bit 6 values:

Value	Name	Description
0h	VRS Compliant **[Default]**	Hardware supports only VRS compliant coarse pixel sizes. Any requested CPsize over the limit is clamped to VRS limit
1h	Extended Coarse Pixel Sizes	Hardware supports additional coarse pixel sizes beyond VRS spec requirements when CPS_MODE_CONSTANT. This includes all 16 sample CP sizes.

Bit 5 values:

Value	Name	Description
0h	Normal_5 **[Default]**	Perfect dispatch will not be selected when 8x8 is one quad short of perfect thread.

PSS_MODE4 - Pixel Shader Scheduling Mode 4

1h	Enable Almost-Perfect	An 8x8 with one quad short of perfect thread will be dispatched as perfect thread with a single quad disabled.

4 **Relaxed 4x4 pair handling**

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Normal_4 **[Default]**	An 8x8 with two QuadQuads (e.g., 4x4) will be scheduled such that both QQ are in the same thread.
1h	Relaxed	Scheduler does not attempt to keep multiple QQ from same 8x8 in same thread.

3 **Fulsim Compatible - Reserved**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Reserved for future fulsim compatibility bits.

Value	Name	Description
0h	Normal_3 **[Default]**	Normal
1h	Maximize Fulsim Compatibility	Future fulsim compatibility requirements. This will result in reduced hardware performance.

Programming Notes
Set bit to 1h to maximize compatibility with fulsim. Hardware has reduced performance when this bit is set.

2 **Fulsim Compatible - Stall Scheduler Intra-poly grid change**

Access:	R/W
Format:	Enable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	**[Default]**	Hardware does not stall scheduler clock after dependency update.
1h	StallOnIntraPolyGrid	If a grid change is loaded into the future queue that is within a poly, then hardware blocks scheduler until grid change is scheduled. This will result in reduced hardware performance, but scheduler policies (allow_gap) will match fulsim.

PSS_MODE4 - Pixel Shader Scheduling Mode 4

		Programming Notes Set this bit to 1 to maximize compatibility with fulsim. Hardware has reduced performance when this bit is set.
	1	**Fulsim Compatible - Stall Scheduler on Dependency update** Access: R/W Format: Enable _Custom_GTIReset: DEV **Value** / **Name** / **Description** 0h / Normal_1 **[Default]** / Hardware does not stall scheduler clock after dependency update. 1h / StallOnDepClear / Hardware blocks scheduler the clock after dependency update so that next scheduler event will match with fulsim. This will result in reduced hardware performance, but dependencies will match fulsim. **Programming Notes** Set this bit to 1 to maximize compatibility with fulsim. Hardware has reduced performance when this bit is set.
	0	**Fulsim Compatible - Disable Extra Future Queue Entries** Access: R/W Format: Enable _Custom_GTIReset: DEV **Value** / **Name** / **Description** 0h / Normal_0 **[Default]** / Hardware uses extended Future Queue Size that has two extra entries for performance reasons. 1h / Disable Extra FQ entries / Hardware does not load more than **Future Queue Depth** entries into the future queue. This will result in reduced hardware performance, but dependencies will match fulsim. **Programming Notes** Set this bit to maximize compatibility with fulsim. Hardware has reduced performance when this bit is set.

PLANE_AFLIP_WIN_CTL

PLANE_AFLIP_WIN_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70484h-70487h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_4_A
Reset:	soft
Address:	70584h-70587h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_5_A
Reset:	soft
Address:	71484h-71487h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_4_B
Reset:	soft
Address:	71584h-71587h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_5_B
Reset:	soft
Address:	72484h-72487h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_4_C
Reset:	soft
Address:	72584h-72587h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_5_C
Reset:	soft
Address:	73484h-73487h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_4_D
Reset:	soft
Address:	73584h-73587h

PLANE_AFLIP_WIN_CTL	
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_5_D
Reset:	soft
Address:	70184h-70187h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_1_A
Reset:	soft
Address:	70284h-70287h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_2_A
Reset:	soft
Address:	70384h-70387h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_3_A
Reset:	soft
Address:	71184h-71187h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_1_B
Reset:	soft
Address:	71284h-71287h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_2_B
Reset:	soft
Address:	71384h-71387h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_3_B
Reset:	soft
Address:	72184h-72187h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_1_C
Reset:	soft
Address:	72284h-72287h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_2_C
Reset:	soft
Address:	72384h-72387h

PLANE_AFLIP_WIN_CTL

Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_3_C
Reset:	soft

Address:	73184h-73187h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_1_D
Reset:	soft

Address:	73284h-73287h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_2_D
Reset:	soft

Address:	73384h-73387h
Name:	Plane AFlip Window Control
ShortName:	PLANE_AFLIP_WIN_CTL_3_D
Reset:	soft

DWord	Bit	Description
0	31	**Async Flip Window Disable** Access: Double Buffered When this bit is set, it will revert async flip operation to legacy behavior. Async flip windowing will be ignored. Note that hardware disables async flip windowing when a linear surface is used. 0b: Enable 1b: Disable
	30	**Fetch Not Completed** Access: R/WC This is a sticky bit that is set to 1 when a fetch has not been completed when a window crossing is reached. Clear by writing 1 to this bit.
	29	**Illegal Aflip Window** Access: R/WC This is a sticky bit that is set to 1 when the segment windows have been programmed with illegal values. Clear by writing 1 to this bit.
	28:21	**Reserved** Access: RO Format: MBZ

PLANE_AFLIP_WIN_CTL

	20:16	**First Window Segments** Access: Double Buffered This field indicates the size in segments of the first window. **Value** / **Name** 00110b / 6 **[Default]** [1,31] /
	15:5	**Reserved** Access: RO Format: MBZ
	4:0	**Second Window Segments** Access: Double Buffered This field indicates the size in segments of the second window. **Value** / **Name** 00001b / 1 **[Default]** [1,31] /

PLANE_BUF_CFG

PLANE_BUF_CFG	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, plane not enabled, or pipe not enabled
Address:	7017Ch-7017Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_A
Reset:	soft
Address:	7117Ch-7117Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_B
Reset:	soft
Address:	7217Ch-7217Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_C
Reset:	soft
Address:	7317Ch-7317Fh
Name:	Cursor Buffer Config
ShortName:	CUR_BUF_CFG_D
Reset:	soft
Address:	7057Ch-7057Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_A
Reset:	soft
Address:	7067Ch-7067Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_A
Reset:	soft
Address:	7157Ch-7157Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_B
Reset:	soft
Address:	7167Ch-7167Fh

PLANE_BUF_CFG	
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_B
Reset:	soft
Address:	7257Ch-7257Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_C
Reset:	soft
Address:	7267Ch-7267Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_C
Reset:	soft
Address:	7357Ch-7357Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_4_D
Reset:	soft
Address:	7367Ch-7367Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_5_D
Reset:	soft
Address:	7027Ch-7027Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_A
Reset:	soft
Address:	7037Ch-7037Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_A
Reset:	soft
Address:	7047Ch-7047Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_A
Reset:	soft
Address:	7127Ch-7127Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_B
Reset:	soft
Address:	7137Ch-7137Fh

PLANE_BUF_CFG

Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_B
Reset:	soft

Address:	7147Ch-7147Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_B
Reset:	soft

Address:	7227Ch-7227Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_C
Reset:	soft

Address:	7237Ch-7237Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_C
Reset:	soft

Address:	7247Ch-7247Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_C
Reset:	soft

Address:	7327Ch-7327Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_1_D
Reset:	soft

Address:	7337Ch-7337Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_2_D
Reset:	soft

Address:	7347Ch-7347Fh
Name:	Plane Buffer Config
ShortName:	PLANE_BUF_CFG_3_D
Reset:	soft

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">PLANE_BUF_CFG</th></tr>
<tr><td></td><td>27</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>26:16</td><td>Buffer End<table><tr><td>Default Value:</td><td>000h</td></tr><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field contains the buffer end position for this plane.</td></tr>
<tr><td></td><td>15:12</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>11</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>10:0</td><td>Buffer Start<table><tr><td>Default Value:</td><td>000h</td></tr><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field contains the buffer start position for this plane.</td></tr>
</table>

PLANE_CC_VAL

PLANE_CC_VAL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	64
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704B4h-704BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_A
Reset:	soft
Address:	705B4h-705BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_A
Reset:	soft
Address:	714B4h-714BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_B
Reset:	soft
Address:	715B4h-715BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_B
Reset:	soft
Address:	724B4h-724BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_C
Reset:	soft
Address:	725B4h-725BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_C
Reset:	soft
Address:	734B4h-734BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_4_D
Reset:	soft
Address:	735B4h-735BBh

PLANE_CC_VAL	
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_5_D
Reset:	soft
Address:	701B4h-701BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_A
Reset:	soft
Address:	702B4h-702BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_A
Reset:	soft
Address:	703B4h-703BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_A
Reset:	soft
Address:	711B4h-711BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_B
Reset:	soft
Address:	712B4h-712BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_B
Reset:	soft
Address:	713B4h-713BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_B
Reset:	soft
Address:	721B4h-721BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_C
Reset:	soft
Address:	722B4h-722BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_C
Reset:	soft
Address:	723B4h-723BBh

PLANE_CC_VAL

Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_C
Reset:	soft

Address:	731B4h-731BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_1_D
Reset:	soft

Address:	732B4h-732BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_2_D
Reset:	soft

Address:	733B4h-733BBh
Name:	Plane Clear Color Value
ShortName:	PLANE_CC_VAL_3_D
Reset:	soft

This register programs the clear color value to be used with render decompression. The value is used only when render decompression and clear color are both enabled in the plane control register.
The register value can be updated when flipping to a new surface with new clear color value. It does not need to be updated if the new surface has the same clear color value as the previous surface.

DWord	Bit	Description
0	31:0	**Clear Color Value DW0** Access: Double Buffered This field gives the 32 bit value of the clear color.
1	31:0	**Clear Color Value DW1** Access: Double Buffered This field gives the upper 32 bit value of the clear color. This field is used only with 64 bits formats, ignored otherwise.

PLANE_COLOR_CTL

PLANE_COLOR_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704CCh-704CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_A
Reset:	soft
Address:	705CCh-705CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_A
Reset:	soft
Address:	714CCh-714CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_B
Reset:	soft
Address:	715CCh-715CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_B
Reset:	soft
Address:	724CCh-724CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_C
Reset:	soft
Address:	725CCh-725CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_C
Reset:	soft
Address:	734CCh-734CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_4_D
Reset:	soft
Address:	735CCh-735CFh

PLANE_COLOR_CTL	
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_5_D
Reset:	soft
Address:	701CCh-701CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_A
Reset:	soft
Address:	702CCh-702CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_A
Reset:	soft
Address:	703CCh-703CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_A
Reset:	soft
Address:	711CCh-711CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_B
Reset:	soft
Address:	712CCh-712CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_B
Reset:	soft
Address:	713CCh-713CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_B
Reset:	soft
Address:	721CCh-721CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_C
Reset:	soft
Address:	722CCh-722CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_C
Reset:	soft
Address:	723CCh-723CFh

PLANE_COLOR_CTL

Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_C
Reset:	soft

Address:	731CCh-731CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_1_D
Reset:	soft

Address:	732CCh-732CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_2_D
Reset:	soft

Address:	733CCh-733CFh
Name:	Plane Color Control
ShortName:	PLANE_COLOR_CTL_3_D
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30	**Pipe Gamma Enable** Access: Double Buffered This bit enables pipe gamma correction for the plane pixel data. This field is deprecated. Use 'GAMMA_MODE.Post CSC Gamma Enable' for enabling pipe gamma across all pixels from all planes. 0b Disable 1b Enable
	29	**Remove YUV Offset** Access: Double Buffered This field controls whether the plane removes or preserves the 1/2 offset on U and V components when the source pixel format is YUV and the plane YUV to RGB CSC is disabled. This bit has no effect on RGB source pixel formats 0b Remove: Remove 1/2 offset on UV components 1b Preserve: Preserve 1/2 offset on UV components

PLANE_COLOR_CTL

28 YUV Range Correction Disable

Access:	Double Buffered

Setting this bit disables the YUV range correction logic inside the plane. The range correction logic is used to expand the compressed range YUV to full range YUV. The Y channel is expanded from the 8 bit +16 to +235 range to full range. The U and V channels are expanded from the 8 bit -112 to +112 range to full range. Extended range values will be preserved after the expansion. This bit has no effect on RGB source pixel formats since they automatically bypass range correction.

Value	Name
0b	Enable
1b	Disable

27:24 Reserved

Access:	RO
Format:	MBZ

23 Pipe CSC Enable

Access:	Double Buffered

This bit enables pipe color space conversion and the pipe pre color space conversion gamma for the plane pixel data. This is separate from the color conversion logic within the plane.

This field is deprecated.
Use 'CSC_MODE.Pipe CSC Enable', 'GAMMA_MODE.Pre CSC Gamma Enable' for enabling pipe color space conversion and gamma respectively across all pixels from all planes. Plane CSC must be used for plane specific color space conversion.

Value	Name
0b	Disable
1b	Enable

22 Reserved

Access:	Double Buffered

21 Plane CSC Enable

Access:	Double Buffered

This field enables the plane color space conversion. This field applies only to planes 1 through 3.

Value	Name
0b	Disable
1b	Enable

20 Plane Input CSC Enable

Access:	Double Buffered

This field enables the plane input color space conversion. This field applies only to planes 1 through 3.

PLANE_COLOR_CTL

Value	Name
0b	Disable
1b	Enable

19:17 **Plane CSC Mode**

Access:	Double Buffered

Description
This field specifies the mode of plane color space conversion operation.
This is used only for planes 4 through 5. For planes 1 through 3, CSC is programmed in PLANE_CSC_* registers.

Value	Name	Description
000b	Bypass	Pixel data bypasses the plane color space conversion
001b	YUV601 to RGB601	YUV BT.601 to RGB BT.601 conversion.
010b	YUV709 to RGB709	YUV BT.709 to RGB BT.709 conversion.
011b	YUV2020 to RGB2020	YUV BT.2020 to RGB BT.2020 conversion.
100b	RGB709 to RGB2020	RGB BT.709 to RGB BT.2020 conversion.

16 **Reserved**

Access:	RO
Format:	MBZ

15 **Plane Post CSC Gamma Multi Segment Enable**

Access:	Double Buffered

This bit enables plane post CSC gamma multi segment processing. It is only used for HDR tone Mapping. It is only valid if Plane Gamma (bit[13]) is enabled.

Value	Name
1b	Enable
0b	Disable **[Default]**

14 **Plane Pre CSC Gamma Enable**

Access:	Double Buffered

This bit controls plane internal pre-CSC gamma correction.

Value	Name
1b	Enable
0b	Disable

13 **Plane Gamma Disable**

Access:	Double Buffered

This bit controls plane internal post-CSC gamma correction.

PLANE_COLOR_CTL

Value	Name
1b	Disable
0b	Enable

12 **Plane Gamma Mode**

Access:	Double Buffered

This field specifies the plane gamma mode of operation. This field is ignored if plane gamma is disabled.

Value	Name	Description
0b	Direct **[Default]**	Direct mode is used for regular plane gamma programming. Lookup is based on incoming pixel individual r, g, b values. The output is a computed by lookup of two nearest points and interpolation.
1b	Multiply	Multiplymode is used when plane gamma is used for HDR tone mapping. The lookup is based on the luminance of the incoming pixel where the luminance is calculated using the following equation: luma = (Kr * red) + (Kg * green) + (Kb * blue) The coefficients (K) used to determine the luminance are programmable from the LM_LUMA_COEFF / PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH registers. An adjustment factor 'F' is computed by lookup of two nearest points and interpolation. Output is computed by multiplying each color channel with the adjustment factor F.

11 **Plane Gamma Multiplier Precision**

Access:	Double Buffered

This field specifies the plane gamma entry format in the multiplier mode. This field is ignored in the direct lookup mode. The gamma entries can be programmed in either unsigned 0.24 format or unsigned 8.16 format.

Value	Name
0b	U0.24 **[Default]**
1b	U8.16

10 **Color Correction Dithering Enable**

Access:	Double Buffered

This bit enables spatial dithering at the outlet of the post CSC gamma or at the outlet of CSC when post CSC gamma is disabled. This bit only applies to HDR planes

Value	Name
0b	Disabled
1b	Enabled

9:6 **Reserved**

Access:	RO
Format:	MBZ

PLANE_COLOR_CTL

5:4 **Alpha Mode**

Access:	Double Buffered

This field controls how the plane will use per pixel alpha data from frame buffer. Constant plane alpha is defined in PLANE_KEYMSK and PLANE_KEYMAX registers.

RGB 64-bit - only alpha in 0-1 range supported with 8 bit granularity.
RGB 64-bit UINT - only 8 upper bits of alpha used.
RGB 2:10:10:10 - 2 bit alpha expanded out to 8 bit to give full range of opacity.
XR_BIAS 10:10:10 - 2 bit alpha expanded out to 8 bit to give full range of opacity.

Value	Name	Description
00b	Disable	Alpha channel ignored.
10b	Enable with SW pre-multiply	Alpha channel used. Color channels should be pre-multiplied with alpha by software.
11b	Enable with HW pre-multiply	Alpha channel used. Color channels will be pre-multiplied with alpha by hardware.

Restriction
Per pixel alpha is supported only with RGB pixel formats.
FBC is not compatible with per pixel alpha.

3 **Reserved**

Access:	RO
Format:	MBZ

2:0 **Smooth Sync Dither Step Size**

Access:	Double Buffered

This field specifies the number of lines to hold a given dither value within the Smooth Sync dithering region before incrementing the dither value.
Step Size $=2^{n}$
Where "n" is the value of this field

Value	Name
000b	Step size of 1
001b	Step size of 2
010b	Step size of 4
011b	Step size of 8
100b	Step size of 16

PLANE_CSC_COEFF

PLANE_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70210h-70227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_A
Reset:	soft
Address:	70310h-70327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_A
Reset:	soft
Address:	70410h-70427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_A
Reset:	soft
Address:	71210h-71227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_B
Reset:	soft
Address:	71310h-71327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_B
Reset:	soft
Address:	71410h-71427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_B
Reset:	soft
Address:	72210h-72227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_C
Reset:	soft
Address:	72310h-72327h

PLANE_CSC_COEFF

Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_C
Reset:	soft

Address:	72410h-72427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_C
Reset:	soft

Address:	73210h-73227h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_1_D
Reset:	soft

Address:	73310h-73327h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_2_D
Reset:	soft

Address:	73410h-73427h
Name:	Plane CSC Coefficients
ShortName:	PLANE_CSC_COEFF_3_D
Reset:	soft

Programming Notes

Refer to Color Space Conversion page for programming details and examples.

DWord	Bit	Description
0	31:16	**RY** Access: Double Buffered Format: CSC COEFFICIENT FORMAT
	15:0	**GY** Access: Double Buffered Format: CSC COEFFICIENT FORMAT
1	31:16	**BY** Access: Double Buffered Format: CSC COEFFICIENT FORMAT
	15:0	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">PLANE_CSC_COEFF</th></tr>
<tr><td>2</td><td>31:16</td><td>RU<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td></td><td>15:0</td><td>GU<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td>3</td><td>31:16</td><td>BU<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td></td><td>15:0</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>4</td><td>31:16</td><td>RV<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td></td><td>15:0</td><td>GV<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td>5</td><td>31:16</td><td>BV<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td></td><td>15:0</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
</table>

PLANE_CSC_POSTOFF

PLANE_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70234h-7023Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_A
Reset:	soft
Address:	70334h-7033Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_A
Reset:	soft
Address:	70434h-7043Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_A
Reset:	soft
Address:	71234h-7123Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_B
Reset:	soft
Address:	71334h-7133Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_B
Reset:	soft
Address:	71434h-7143Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_B
Reset:	soft
Address:	72234h-7223Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_C
Reset:	soft
Address:	72334h-7233Fh

PLANE_CSC_POSTOFF

Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_C
Reset:	soft

Address:	72434h-7243Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_C
Reset:	soft

Address:	73234h-7323Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_1_D
Reset:	soft

Address:	73334h-7333Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_2_D
Reset:	soft

Address:	73434h-7343Fh
Name:	Plane CSC Post-offset
ShortName:	PLANE_CSC_POSTOFF_3_D
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit plane color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

<table>
<tr><th colspan="3">PLANE_CSC_POSTOFF</th></tr>
<tr><td rowspan="2">2</td><td>31:13</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>12:0</td><td>PostCSC Low Offset<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
</table>

PLANE_CSC_PREOFF

PLANE_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70228h-70233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_A
Reset:	soft
Address:	70328h-70333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_A
Reset:	soft
Address:	70428h-70433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_A
Reset:	soft
Address:	71228h-71233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_B
Reset:	soft
Address:	71328h-71333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_B
Reset:	soft
Address:	71428h-71433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_B
Reset:	soft
Address:	72228h-72233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_C
Reset:	soft
Address:	72328h-72333h

PLANE_CSC_PREOFF

Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_C
Reset:	soft

Address:	72428h-72433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_C
Reset:	soft

Address:	73228h-73233h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_1_D
Reset:	soft

Address:	73328h-73333h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_2_D
Reset:	soft

Address:	73428h-73433h
Name:	Plane CSC Pre-offset
ShortName:	PLANE_CSC_PREOFF_3_D
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter plane color space conversion (CSC).
RGB modes: Red is in the High channel, Green in Medium, and Blue in Low.
YUV modes:V is in the High channel, Y in Medium, and U in Low.

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

<table>
<tr><th colspan="3">PLANE_CSC_PREOFF</th></tr>
<tr><td rowspan="2">2</td><td>31:13</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>12:0</td><td>PreCSC Low Offset<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
</table>

PLANE_CTL

PLANE_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70480h-70483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_A
Reset:	soft
Address:	70580h-70583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_A
Reset:	soft
Address:	71480h-71483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_B
Reset:	soft
Address:	71580h-71583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_B
Reset:	soft
Address:	72480h-72483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_C
Reset:	soft
Address:	72580h-72583h
Name:	Plane Control
ShortName:	PLANE_CTL_5_C
Reset:	soft
Address:	73480h-73483h
Name:	Plane Control
ShortName:	PLANE_CTL_4_D
Reset:	soft
Address:	73580h-73583h

PLANE_CTL	
Name:	Plane Control
ShortName:	PLANE_CTL_5_D
Reset:	soft
Address:	70180h-70183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_A
Reset:	soft
Address:	70280h-70283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_A
Reset:	soft
Address:	70380h-70383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_A
Reset:	soft
Address:	71180h-71183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_B
Reset:	soft
Address:	71280h-71283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_B
Reset:	soft
Address:	71380h-71383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_B
Reset:	soft
Address:	72180h-72183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_C
Reset:	soft
Address:	72280h-72283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_C
Reset:	soft
Address:	72380h-72383h

PLANE_CTL

Name:	Plane Control
ShortName:	PLANE_CTL_3_C
Reset:	soft

Address:	73180h-73183h
Name:	Plane Control
ShortName:	PLANE_CTL_1_D
Reset:	soft

Address:	73280h-73283h
Name:	Plane Control
ShortName:	PLANE_CTL_2_D
Reset:	soft

Address:	73380h-73383h
Name:	Plane Control
ShortName:	PLANE_CTL_3_D
Reset:	soft

The pipe scaler can be attached to a plane to scale the plane output before blending.

Restriction
Refer to 'Plane Capability and Interoperability' page for plane capabilities and restrictions.

DWord	Bit	Description
0	31	**Plane Enable** Access: Double Buffered When this bit is set, the plane will generate pixels for display. When cleared to zero, plane memory fetches cease and plane output is transparent. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:28	**Pipe Slice Arbitration Slots** Access: Double Buffered This field specifies the number of slots allocated to this plane in pipe slice request arbitration. This field is ignored when the 'PIPE_SLICE_ARBITRATION_CTL->Use Programmed Slots' is not set. This field is zero based; a programmed value of 0 results in 1 slot allocation.
	27:23	**Source Pixel Format** Access: Double Buffered This field selects the source pixel format for the plane. Before entering the blender, each source format is converted to the pipe pixel format. The 8-bpp indexed format will always use the pipe palette.

In planar YUV formats Y samples appear first in memory followed by interleaved UV samples. YUV 4:2:2 byte order is programmed separately. YUV 4:2:0 and YUV 4:4:4 byte order is not programmable.
RGB color order is programmed separately for some formats.
Refer to Universal Plane, Plane Pixel Formats section for color channel bit mappings.

YUV 4:2:0 P010, P012 and P016 formats share the same 16 bpc memory layout but use 10, 12 and 16 bits per channel respectively. The color values are stored in the most significant bits.

64-bit formats supported only on the HDR planes.
P01x output is only allowed from HDR planes.

Value	Name	Description
00000b	YUV 422 Packed 8 bpc	YUV 4:2:2 packed, 8 bpc
00010b	YUV 420 Planar 8 bpc	YUV 4:2:0 Planar, 8 bpc - NV12
00100b	RGB 2101010	RGB 2:10:10:10, 32 bit.
00110b	YUV 420 Planar 10 bpc	YUV 4:2:0 Planar, 10 bpc - P010
01000b	RGB 8888	RGB 8:8:8:8, 32 bit
01010b	YUV 420 Planar 12 bpc	YUV 4:2:0 Planar 12 bpc - P012
01100b	RGB 16161616 Float	RGB 16:16:16:16 Floating Point, 64 bit (FP16)
01110b	YUV 420 Planar 16 bpc	YUV 4:2:0 Planar, 16 bpc - P016
10000b	YUV 444 Packed 8 bpc	YUV 4:4:4 packed (MSB-X:Y:U:V), 8bpc
10100b	RGB 2101010 XR_BIAS	RGB 2:10:10:10 Extended Range Bias (MSB-X:B:G:R), 32 bit
11000b	Indexed 8 bit	Indexed 8-bit
11100b	RGB 565	RGB 5:6:5 (MSB-R:G:B), 16 bit
00001b	YUV 422 Packed 10 bpc	YUV 4:2:2 packed, 10 bpc - Y210
00011b	YUV 422 Packed 12 bpc	YUV 4:2:2 packed, 12 bpc - Y212
00101b	YUV 422 Packed 16 bpc	YUV 4:2:2 packed, 16 bpc - Y216
00111b	YUV 444 Packed 10 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 10 bpc - Y410
01001b	YUV 444 Packed 12 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 12 bpc - Y412
01011b	YUV 444 Packed 16 bpc	YUV 4:4:4 packed (MSB-X:V:Y:U), 16 bpc - Y416

Restriction
Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS source pixel formats.

22:21 **Key Enable**

Access:	Double Buffered

This field enables color keying. The key color, range, channel enables, and mask are programmed in PLANE_KEYVAL, PLANE_KEYMSK, and PLANE_KEYMAX.

PLANE_CTL

Value	Name	Description
00b	Disable	Disable keying for this plane.
01b	Source Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent.
10b	Destination Key Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane above will treat the pixels above as opaque only where this plane is key matched and the plane above is opaque. When plane gamma is enabled, the gamma processing may shift the pixel color values sent to blender and may cause it to not match the key color as desired. The recommendation is to use the pipe gamma when destination keying is enabled.
11b	Source Key Window Enable	This plane's pixels will be checked for a key match. The blend between this plane and the plane below will treat the key matched pixels as transparent only where the plane below is opaque.

Restriction
Plane color keying is not compatible with the Indexed 8-bit pixel format. Destination key/Source Key Window should be enabled only on one set (a pair) of planes, per pipe, at a time. Source key and Source Key Window must not be enabled on the bottom most active plane. Destination key must not be enabled on the top most active plane.

20 **RGB Color Order**

Access:	Double Buffered

This field is used to select the color order when using RGB data formats, except RGB 32-bit XR_BIAS 10:10:10 and 16-bit BGRX 5:6:5. For other formats, this field is ignored.

Value	Name	Description
0b	BGRX	BGRX (MSB-X:R:G:B)
1b	RGBX	RGBX (MSB-X:B:G:R)

19 **Planar YUV420 component**

Access:	Double Buffered

This field selects the planar YUV420 component for the plane when NV12/P0xx source pixel formats is used. This field must be set to '0b' for other (YUV non-planar/RGB) surface formats.

Value	Name	Description
0b	UV	Planes 1 to 3 can be configured as UV plane. Planes 4 and 5 must not be configured as a UV plane.
1b	Y	Planes 4 and 5 can be configured as Y plane. Planes 1 to 3 must not be configured as a Y plane.

PLANE_CTL

18 **Smooth Sync Plane Enable**

Access:	Double Buffered

When this bit is set, then this Plane will be enabled as the Back Plane of the two adjacent Smooth Sync Planes.
This Plane will advertise to its adjacent top Plane that that Plane is being used as the Front Plane of the Smooth Sync Plane pair

Value	Name
0b	Smooth Sync disabled
1b	Smooth Sync enabled

Restriction
1. There must be an adjacent top Plane to this Plane when setting this bit (i.e. cannot set this bit for the top most Plane) 2. The adjacent top Plane must be the same type as this Plane (i.e. HDR or SDR)

17:16 **YUV 422 Byte Order**

Access:	Double Buffered

This field is used to select the byte order for YUV 4:2:2 8bpc data formats. For other formats, this field is ignored.

Value	Name	Description
00b	YUYV	YUYV (MSB-V:Y2:U:Y1)
01b	UYVY	UYVY (MSB-Y2:V:Y1:U)
10b	YVYU	YVYU (MSB-U:Y2:V:Y1)
11b	VYUY	VYUY (MSB-Y2:U:Y1:V)

15 **Render Decomp**

Access:	Double Buffered

This bit enables the Display decompression of Render compressed surfaces.

Value	Name
0b	Disable
1b	Enable

Restriction
Color Clear is supported.
Only the Left-right cache-line pair decompression is supported. The compressed surface should be Y (Legacy) or Y F Tiled. Decompression is not supported with 90/270 degree rotation.
Decompression is supported with RGB8888, RGB1010102 and FP16 formats.
Decompression is supported on all planes and pipes.

14 **Reserved**

Access:	RO
Format:	MBZ

13 **Clear Color Disable**

Access:	Double Buffered

This field disables the render decompression clear color mode. It is ignored when the Render Decomp field is disabled. The color value must be programmed in PLANE_CC_VAL before flipping to the surface that uses clear color value.

Value	Name
1b	Disable
0b	Enable **[Default]**

12:10 **Tiled Surface**

Access:	Double Buffered

This field indicates that the surface data is in tiled memory. This bit may be updated through MMIO writes or through a command streamer initiated synchronous flip.

Value	Name
000b	Linear memory
001b	Tile X memory
101b	Tile 4 memory

Restriction
Interlaced mode is not supported with Y Tiling. Tile Ys is not supported.

9 **Async Address Update Enable**

Access:	R/W

This bit will enable asynchronous updates of the plane surface address when written by MMIO (MMIO asynchronous flips). The surface address will change as soon as possible. This bit is not double buffered and the changes will apply immediately. When performing an asynchronous update, only the plane surface can be updated. Changes to stride, pixel, format, compression, FBC, etc. are not allowed.

Value	Name	Description
0b	Sync	Surface Address MMIO writes will update synchronous to start of vertical blank
1b	Async	Surface Address MMIO writes will update asynchronous to start of vertical blank

Restriction
No command streamer (ring) flips to this plane are allowed when this bit is enabled. Command streamer flips will set a similar bit in the flip message that it sends to display.
Asynchronous S3D flips are not allowed.
Each async surface address write must be followed by a wait for flip done indication before writing the surface address register again.

PLANE_CTL

8 **Horizontal Flip**

Access:	Double Buffered

This field controls the horizontal flipping of the plane. When horizontal flipping is enabled with rotation, the horizontal flip operation is logically performed first followed by rotation. For further information refer to "Universal Plane" section.

Value	Name
0b	Disable **[Default]**
1b	Enable

Restriction
Horizontal flip is not supported with linear surface formats.

7:6 **Stereo Surface Vblank Mask**

Access:	Double Buffered

This field controls which vertical blank (left eye, right eye, or both) will be used for the plane surface address double-buffering during stereo 3D mode. This field is ignored when not in stereo 3D mode.

Value	Name	Description
00b	Mask None	Both the left and right eye vertical blanks will be used.
01b	Mask Left	Mask the left eye vertical blank. Only the right eye vertical blank will be used.
10b	Mask Right	Mask the right eye vertical blank. Only the left eye vertical blank will be used.

5 **Reserved**

Access:	Double Buffered

4 **Media Decomp**

Access:	Double Buffered

This bit enables the Display decompression of Media compressed surfaces. 'Media Decomp' and 'Render Decomp' are mutually exclusive and must not enabled at the same time for a given plane.

Media decompression is supported with NV12, P0xx, YUV422, YUV444, RGB8888, RGB1010102 and FP16 formats.

Value	Name
0b	Disable
1b	Enable

PLANE_CTL

	3	**Allow DB Stall** Access: R/W This field controls whether double buffer updates are allowed to be stalled for this plane. **Value** / **Name** 0b: Not Allowed 1b: Allowed **[Default]**
	2	**Reserved** Access: RO Format: MBZ
	1:0	**Plane Rotation** Access: Double Buffered This field controls hardware rotation of the plane. **Value** / **Name** 00b: No rotation 10b: 180 degree rotation **Programming Notes** Hardware does not change the plane position when rotation is enabled. Software may need to adjust the plane position to match the physical orientation of the display.

PLANE_CUS_CTL

PLANE_CUS_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	701C8h-701CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_A
Reset:	soft
Address:	702C8h-702CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_A
Reset:	soft
Address:	703C8h-703CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_A
Reset:	soft
Address:	711C8h-711CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_B
Reset:	soft
Address:	712C8h-712CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_B
Reset:	soft
Address:	713C8h-713CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_B
Reset:	soft
Address:	721C8h-721CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_C
Reset:	soft
Address:	722C8h-722CBh

PLANE_CUS_CTL

Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_C
Reset:	soft

Address:	723C8h-723CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_C
Reset:	soft

Address:	731C8h-731CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_1_D
Reset:	soft

Address:	732C8h-732CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_2_D
Reset:	soft

Address:	733C8h-733CBh
Name:	Plane Chroma Upsampler Control
ShortName:	PLANE_CUS_CTL_3_D
Reset:	soft

Description

This register programs the chroma upsampler for processing pixel streams from hybrid planar YUV 420 (NV12, P0xx) surfaces.
This dedicated chroma upsampling capability is available only in Planes 1 through 3.
The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios where the chroma is being filtered to the top left of the pixel.

YUV 420Chroma Siting	Horz Phase	Vert Phase	Programmed Horz Initial Phase	Programmed Horz Initial Phase Sign	Programmed Vert Initial Phase	Programmed Vert Initial Phase Sign
Top Left	0	0	0	0	0	0
Top	-0.25	0	0.25	1	0	0
Left (MPEG-2)	0	-0.25	0	0	0.25	1
Center (MPEG-1)	-0.25	-0.25	0.25	1	0.25	1

Restriction :
When the Chroma upsampler is enabled, then:

1. The maximum horizontal plane size allowed is 4096 pixels
2. The minimum horizontal plane size allowed is 8 pixels

PLANE_CUS_CTL

3. The minimum vertical plane size allowed is 4 lines
4. The horizontal and vertical plane size should be even

DWord	Bit	Description
0	31	**Chroma Upsampler Enable** Access: Double Buffered This field enables the plane chroma upsampler for handling hybrid planar YUV 420 (NV12, P0xx) formats. Value 0b: Disable Value 1b: Enable
	30	**Y Binding** Access: Double Buffered This field defines the Y plane from where the chroma upsampler will receive the Y pixels stream when processing hybrid planar YUV 420 (NV12, P0xx) formats. Value 0b: Plane 4 Value 1b: Plane 5
	29:24	**Reserved** Access: RO Format: MBZ
	23	**Reserved** Access: Double Buffered
	22	**Reserved** Access: RO Format: MBZ
	21:20	**Reserved** Access: Double Buffered
	19	**Horz Initial Phase Sign** Access: Double Buffered This field is defines the direction of the horizontal initial phase adjustment on the UV stream during upsampling. A positive initial phase will have an effect of shifting the UV pixels to the right with respect to the Y pixels whereas a negative initial phase will have an effect of shifting left. The sign bit must be zero if the initial phase is zero. Value 0b: Positive Initial Phase Value 1b: Negative Initial Phase

PLANE_CUS_CTL

18	**Reserved** Access: RO Format: MBZ
17:16	**Horz Initial Phase** Access: Double Buffered This field defines the horizontal initial phase adjustment required on the UV stream during upsampling. This field should be programmed based on the YUV 420 chroma siting.

Value	Name
00b	0
01b	0.25
10b	0.5
11b	Reserved

15	**Vert Initial Phase Sign** Access: Double Buffered This field defines the direction of the vertical initial phase adjustment on the UV stream during upsampling. A positive initial phase will have an effect of shifting the UV pixels down with respect to the Y pixels whereas a negative initial phase will have an effect of shifting up. The sign bit must be zero if the initial phase is zero.

Value	Name
0b	Positive Initial Phase
1b	Negative Initial Phase

14	**Reserved** Access: RO Format: MBZ
13:12	**Vert Initial Phase** Access: Double Buffered This field defines the vertical initial phase adjustment required on the UV stream during upsampling. This field should be programmed based on the YUV 420 chroma siting.

Value	Name
00b	0
01b	0.25
10b	0.5
11b	Reserved

11	**Reserved** Access: Double Buffered

PLANE_CUS_CTL

	10:9	**Power Up Delay** Access: Double Buffered This field indicates the wait (in CD clocks) between powering up the line buffer arrays.
	8	**Reserved** Access: Double Buffered
	7:6	**Reserved** Access: RO Format: MBZ
	5	**ECC Single Error** Access: R/WC This field indicates that an single bit error encountered at the ECC logic. Hardware will correct the single bit errors. Hardware will set the bit; SW can clear with a write of 1.
	4	**ECC Double Error** Access: R/WC This field indicates that an double bit error encountered at the ECC logic. Hardware will not correct the double bit errors. Hardware will set the bit; SW can clear with a write of 1.
	3:1	**Reserved** Access: RO Format: MBZ
	0	**Power Up In Progress** Access: RO This field is set when the chroma upsampler line buffers are being powered up. Chroma upsampler cannot handle pixel traffic when this bit is set.

PLANE_INPUT_CSC_COEFF

PLANE_INPUT_CSC_COEFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	192
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701E0h-701F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_A
Reset:	soft
Address:	702E0h-702F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_A
Reset:	soft
Address:	703E0h-703F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_A
Reset:	soft
Address:	711E0h-711F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_B
Reset:	soft
Address:	712E0h-712F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_B
Reset:	soft
Address:	713E0h-713F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_B
Reset:	soft
Address:	721E0h-721F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_C
Reset:	soft
Address:	722E0h-722F7h

PLANE_INPUT_CSC_COEFF

Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_C
Reset:	soft
Address:	723E0h-723F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_C
Reset:	soft
Address:	731E0h-731F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_1_D
Reset:	soft
Address:	732E0h-732F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_2_D
Reset:	soft
Address:	733E0h-733F7h
Name:	Plane Input CSC Coefficients
ShortName:	PLANE_INPUT_CSC_COEFF_3_D
Reset:	soft

DWord	Bit	Description
0	31:16	**RY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**GY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
1	31:16	**BY** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**
	15:0	**Reserved** Access: RO Format: MBZ
2	31:16	**RU** Access: Double Buffered Format: **CSC COEFFICIENT FORMAT**

<table>
<tr><th colspan="3">PLANE_INPUT_CSC_COEFF</th></tr>
<tr><td></td><td>15:0</td><td>GU<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td rowspan="2">3</td><td>31:16</td><td>BU<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td>15:0</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td rowspan="2">4</td><td>31:16</td><td>RV<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td>15:0</td><td>GV<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td rowspan="2">5</td><td>31:16</td><td>BV<table><tr><td>Access:</td><td>Double Buffered</td></tr><tr><td>Format:</td><td>CSC COEFFICIENT FORMAT</td></tr></table></td></tr>
<tr><td>15:0</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
</table>

PLANE_INPUT_CSC_POSTOFF

PLANE_INPUT_CSC_POSTOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	70204h-7020Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_A
Reset:	soft
Address:	70304h-7030Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_A
Reset:	soft
Address:	70404h-7040Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_A
Reset:	soft
Address:	71204h-7120Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_B
Reset:	soft
Address:	71304h-7130Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_B
Reset:	soft
Address:	71404h-7140Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_B
Reset:	soft
Address:	72204h-7220Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_C
Reset:	soft
Address:	72304h-7230Fh

PLANE_INPUT_CSC_POSTOFF

Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_C
Reset:	soft

Address:	72404h-7240Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_C
Reset:	soft

Address:	73204h-7320Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_1_D
Reset:	soft

Address:	73304h-7330Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_2_D
Reset:	soft

Address:	73404h-7340Fh
Name:	Plane Input CSC Post-offset
ShortName:	PLANE_INPUT_CSC_POSTOFF_3_D
Reset:	soft

The post-offset is intended to add an offset from 0 on the Y or RGB channels and to convert UV channels from 2's complement to excess 0.5 as they exit plane input color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PostCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

<table>
<tr><th colspan="3">PLANE_INPUT_CSC_POSTOFF</th></tr>
<tr><td rowspan="2">2</td><td>31:13</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>12:0</td><td>PostCSC Low Offset<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the low color channel as it exits CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
</table>

PLANE_INPUT_CSC_PREOFF

PLANE_INPUT_CSC_PREOFF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	96
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701F8h-70203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_A
Reset:	soft
Address:	702F8h-70303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_A
Reset:	soft
Address:	703F8h-70403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_A
Reset:	soft
Address:	711F8h-71203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_B
Reset:	soft
Address:	712F8h-71303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_B
Reset:	soft
Address:	713F8h-71403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_B
Reset:	soft
Address:	721F8h-72203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_C
Reset:	soft
Address:	722F8h-72303h

PLANE_INPUT_CSC_PREOFF

Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_C
Reset:	soft

Address:	723F8h-72403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_C
Reset:	soft

Address:	731F8h-73203h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_1_D
Reset:	soft

Address:	732F8h-73303h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_2_D
Reset:	soft

Address:	733F8h-73403h
Name:	Plane Input CSC Pre-offset
ShortName:	PLANE_INPUT_CSC_PREOFF_3_D
Reset:	soft

The pre-offset is intended to remove an offset from 0 on the Y or RGB channels and to convert UV channels from excess 0.5 to 2's complement as they enter plane input color space conversion (CSC).

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC High Offset** Access: Double Buffered This value is used to give an offset to the high color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).
1	31:13	**Reserved** Access: RO Format: MBZ
	12:0	**PreCSC Medium Offset** Access: Double Buffered This value is used to give an offset to the medium color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).

<table>
<tr><th colspan="3">PLANE_INPUT_CSC_PREOFF</th></tr>
<tr><td rowspan="2">2</td><td>31:13</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td>12:0</td><td>PreCSC Low Offset<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This value is used to give an offset to the low color channel as it enters CSC logic. The value is a 2's complement fraction allowing offsets between -1 and +1 (exclusive).</td></tr>
</table>

PLANE_KEYMAX

PLANE_KEYMAX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	704A0h-704A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_A
Reset:	soft
Address:	705A0h-705A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_A
Reset:	soft
Address:	714A0h-714A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_B
Reset:	soft
Address:	715A0h-715A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_B
Reset:	soft
Address:	724A0h-724A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_C
Reset:	soft
Address:	725A0h-725A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_C
Reset:	soft
Address:	734A0h-734A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_4_D
Reset:	soft
Address:	735A0h-735A3h

PLANE_KEYMAX	
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_5_D
Reset:	soft
Address:	701A0h-701A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_A
Reset:	soft
Address:	702A0h-702A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_A
Reset:	soft
Address:	703A0h-703A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_A
Reset:	soft
Address:	711A0h-711A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_B
Reset:	soft
Address:	712A0h-712A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_B
Reset:	soft
Address:	713A0h-713A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_B
Reset:	soft
Address:	721A0h-721A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_C
Reset:	soft
Address:	722A0h-722A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_C
Reset:	soft
Address:	723A0h-723A3h

PLANE_KEYMAX

Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_C
Reset:	soft

Address:	731A0h-731A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_1_D
Reset:	soft

Address:	732A0h-732A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_2_D
Reset:	soft

Address:	733A0h-733A3h
Name:	Plane Key Color Max
ShortName:	PLANE_KEYMAX_3_D
Reset:	soft

When plane source is YUV, this register specifies the maximum YUV key value to be used together with the minimum YUV key value and the channel enables to determine if the plane matches the key.When plane source is RGB, this register is not used.

DWord	Bit	Description
0	31:24	**Plane Alpha Value** Access: Double Buffered Specifies the plane alpha value when plane alpha is enabled in PLANE_KEYMSK register.
	23:16	**V Key Max Value** Access: Double Buffered Specifies the maximum key value for the V channel.
	15:8	**Y Key Max Value** Access: Double Buffered Specifies the maximum key value for the Y channel.
	7:0	**U Key Max Value** Access: Double Buffered Specifies the maximum key value for the U channel.

PLANE_KEYMSK

PLANE_KEYMSK	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70498h-7049Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_A
Reset:	soft
Address:	70598h-7059Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_A
Reset:	soft
Address:	71498h-7149Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_B
Reset:	soft
Address:	71598h-7159Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_B
Reset:	soft
Address:	72498h-7249Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_C
Reset:	soft
Address:	72598h-7259Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_C
Reset:	soft
Address:	73498h-7349Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_4_D
Reset:	soft
Address:	73598h-7359Bh

PLANE_KEYMSK	
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_5_D
Reset:	soft
Address:	70198h-7019Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_A
Reset:	soft
Address:	70298h-7029Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_A
Reset:	soft
Address:	70398h-7039Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_A
Reset:	soft
Address:	71198h-7119Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_B
Reset:	soft
Address:	71298h-7129Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_B
Reset:	soft
Address:	71398h-7139Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_B
Reset:	soft
Address:	72198h-7219Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_C
Reset:	soft
Address:	72298h-7229Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_C
Reset:	soft
Address:	72398h-7239Bh

PLANE_KEYMSK

Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_C
Reset:	soft

Address:	73198h-7319Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_1_D
Reset:	soft

Address:	73298h-7329Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_2_D
Reset:	soft

Address:	73398h-7339Bh
Name:	Plane Key Mask
ShortName:	PLANE_KEYMSK_3_D
Reset:	soft

DWord	Bit	Description
0	31	**Plane Alpha Enable** Access: Double Buffered Enables the plane alpha. Color channels will be pre-multiplied by hardware with the plane alpha value from PLANE_KEYMAX register. Per-pixel alpha is defined in the PLANE_COLOR_CTL register. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:27	**Reserved** Access: RO Format: MBZ
	26	**V or R Key Channel Enable** Access: Double Buffered Enables the V/Red channel for key comparison. A disabled channel will be ignored when determining a key match. Value: 0b — Name: Disable Value: 1b — Name: Enable
	25	**Y or G Key Channel Enable** Access: Double Buffered Enables the Y/Green channel for key comparison. A disabled channel will be ignored when determining a key match.

PLANE_KEYMSK

Value	Name
0b	Disable
1b	Enable

24 U or B Key Channel Enable

Access:	Double Buffered

Enables the U/Blue channel for key comparison. A disabled channel will be ignored when determining a key match.

Value	Name
0b	Disable
1b	Enable

23:16 R Key Mask Value

Access:	Double Buffered

Specifies the key mask for the Red channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.

15:8 G Key Mask Value

Access:	Double Buffered

Specifies the key mask for the Green channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.

7:0 B Key Mask Value

Access:	Double Buffered

Specifies the key mask for the Blue channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.

PLANE_KEYVAL

PLANE_KEYVAL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	70494h-70497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_A
Reset:	soft
Address:	70594h-70597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_A
Reset:	soft
Address:	71494h-71497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_B
Reset:	soft
Address:	71594h-71597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_B
Reset:	soft
Address:	72494h-72497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_C
Reset:	soft
Address:	72594h-72597h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_C
Reset:	soft
Address:	73494h-73497h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_4_D
Reset:	soft
Address:	73594h-73597h

PLANE_KEYVAL	
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_5_D
Reset:	soft
Address:	70194h-70197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_A
Reset:	soft
Address:	70294h-70297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_A
Reset:	soft
Address:	70394h-70397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_A
Reset:	soft
Address:	71194h-71197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_B
Reset:	soft
Address:	71294h-71297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_B
Reset:	soft
Address:	71394h-71397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_B
Reset:	soft
Address:	72194h-72197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_C
Reset:	soft
Address:	72294h-72297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_C
Reset:	soft
Address:	72394h-72397h

PLANE_KEYVAL

Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_C
Reset:	soft

Address:	73194h-73197h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_1_D
Reset:	soft

Address:	73294h-73297h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_2_D
Reset:	soft

Address:	73394h-73397h
Name:	Plane Key Color
ShortName:	PLANE_KEYVAL_3_D
Reset:	soft

When plane source is YUV, this register specifies the minimum YUV key value to be used together with the maximum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register specifies the RGB key value to be used together with the channel masks to determine if the plane matches the key. RGB key matches can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match. MSB bits are used for comparison.

Restriction : Keying is not supported in HDR mode.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**V Min or R Key Value** Access: Double Buffered Specifies the minimum key value for the V channel or the compare value for Red channel.
	15:8	**Y Min or G Key Value** Access: Double Buffered Specifies the minimum key value for the Y channel or the compare value for Green channel.
	7:0	**U Min or B Key Value** Access: Double Buffered Specifies the minimum key value for the U channel or the compare value for Blue channel.

PLANE_LEFT_SURF

PLANE_LEFT_SURF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of left or right eye vertical blank (selectable), pipe not enabled. or plane not enabled; after armed
Address:	704B0h-704B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_A
Reset:	soft
Address:	705B0h-705B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_A
Reset:	soft
Address:	714B0h-714B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_B
Reset:	soft
Address:	715B0h-715B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_B
Reset:	soft
Address:	724B0h-724B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_C
Reset:	soft
Address:	725B0h-725B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_C
Reset:	soft
Address:	734B0h-734B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_4_D
Reset:	soft

PLANE_LEFT_SURF	
Address:	735B0h-735B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_5_D
Reset:	soft
Address:	701B0h-701B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_A
Reset:	soft
Address:	702B0h-702B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_A
Reset:	soft
Address:	703B0h-703B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_A
Reset:	soft
Address:	711B0h-711B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_B
Reset:	soft
Address:	712B0h-712B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_B
Reset:	soft
Address:	713B0h-713B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_B
Reset:	soft
Address:	721B0h-721B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_C
Reset:	soft
Address:	722B0h-722B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_C
Reset:	soft

PLANE_LEFT_SURF

Address:	723B0h-723B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_C
Reset:	soft

Address:	731B0h-731B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_1_D
Reset:	soft

Address:	732B0h-732B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_2_D
Reset:	soft

Address:	733B0h-733B3h
Name:	Plane Left Surface Base Address
ShortName:	PLANE_LEFT_SURF_3_D
Reset:	soft

Restriction

This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.

DWord	Bit	Description
0	31:12	**Left Surface Base Address** Access: Double Buffered Format: GraphicsAddress[31:12] This address specifies the stereo 3D left eye surface base address bits 31:12. **Restriction** This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.
	11:0	**Reserved** Access: RO Format: MBZ

PLANE_OFFSET

PLANE_OFFSET	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, pipe not enabled, or plane not enabled
Address:	704A4h-704A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_A
Reset:	soft
Address:	705A4h-705A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_A
Reset:	soft
Address:	714A4h-714A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_B
Reset:	soft
Address:	715A4h-715A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_B
Reset:	soft
Address:	724A4h-724A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_C
Reset:	soft
Address:	725A4h-725A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_C
Reset:	soft
Address:	734A4h-734A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_4_D
Reset:	soft
Address:	735A4h-735A7h

PLANE_OFFSET	
Name:	Plane Offset
ShortName:	PLANE_OFFSET_5_D
Reset:	soft
Address:	701A4h-701A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_A
Reset:	soft
Address:	702A4h-702A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_A
Reset:	soft
Address:	703A4h-703A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_A
Reset:	soft
Address:	711A4h-711A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_B
Reset:	soft
Address:	712A4h-712A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_B
Reset:	soft
Address:	713A4h-713A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_B
Reset:	soft
Address:	721A4h-721A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_C
Reset:	soft
Address:	722A4h-722A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_C
Reset:	soft
Address:	723A4h-723A7h

PLANE_OFFSET	
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_C
Reset:	soft
Address:	731A4h-731A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_1_D
Reset:	soft
Address:	732A4h-732A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_2_D
Reset:	soft
Address:	733A4h-733A7h
Name:	Plane Offset
ShortName:	PLANE_OFFSET_3_D
Reset:	soft
Address:	7089Ch-7089Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_1_A
Reset:	soft
Address:	708BCh-708BFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_2_A
Reset:	soft
Address:	708DCh-708DFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_3_A
Reset:	soft
Address:	708FCh-708FFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_4_A
Reset:	soft
Address:	7092Ch-7092Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_5_A
Reset:	soft
Address:	7189Ch-7189Fh

PLANE_OFFSET	
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_1_B
Reset:	soft
Address:	718BCh-718BFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_2_B
Reset:	soft
Address:	718DCh-718DFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_3_B
Reset:	soft
Address:	718FCh-718FFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_4_B
Reset:	soft
Address:	7192Ch-7192Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_5_B
Reset:	soft
Address:	7289Ch-7289Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_1_C
Reset:	soft
Address:	728BCh-728BFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_2_C
Reset:	soft
Address:	728DCh-728DFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_3_C
Reset:	soft
Address:	728FCh-728FFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_4_C
Reset:	soft
Address:	7292Ch-7292Fh

PLANE_OFFSET

Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_5_C
Reset:	soft

Address:	7389Ch-7389Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_1_D
Reset:	soft

Address:	738BCh-738BFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_2_D
Reset:	soft

Address:	738DCh-738DFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_3_D
Reset:	soft

Address:	738FCh-738FFh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_4_D
Reset:	soft

Address:	7392Ch-7392Fh
Name:	Selective Fetch Plane Offset
ShortName:	SEL_FETCH_PLANE_OFFSET_5_D
Reset:	soft

This register specifies the panning for the plane surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image.

Programming Notes

For 8bpp formats, the maximum offset that can be programmed is 64K-1.

Restriction

Plane Size + Plane Offset should not exceed the surface <stride/width> (in pixels)
X and Y offset restrictions are specified in the following table. For formats not specified in the table, both odd and even offsets are supported.

PixelFormat	Rotate	Start X Position	Start Y Position
YUV 420 Planar - NV12	All	Even	Even
YUV 420 Planar - P01x	All	Even	Even
YUV 422	All	Even	Even

DWord	Bit	Description
0	31:16	**Start Y Position** Access: Double Buffered The Start Y Position or the Y Offset is the vertical offset in lines of the beginning of the active display plane relative to the display surface.
	15:0	**Start X Position** Access: Double Buffered The Start X Position or the X Offset is the horizontal offset in pixels of the beginning of the active display plane relative to the display surface.

PLANE_PIXEL_NORMALIZE

PLANE_PIXEL_NORMALIZE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	701A8h-701ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_A
Reset:	soft
Address:	702A8h-702ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_A
Reset:	soft
Address:	703A8h-703ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_A
Reset:	soft
Address:	711A8h-711ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_B
Reset:	soft
Address:	712A8h-712ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_B
Reset:	soft
Address:	713A8h-713ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_B
Reset:	soft
Address:	721A8h-721ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_C
Reset:	soft
Address:	722A8h-722ABh

PLANE_PIXEL_NORMALIZE

Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_C
Reset:	soft

Address:	723A8h-723ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_C
Reset:	soft

Address:	731A8h-731ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_1_D
Reset:	soft

Address:	732A8h-732ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_2_D
Reset:	soft

Address:	733A8h-733ABh
Name:	Plane Pixel Normalize
ShortName:	PLANE_PIXEL_NORMALIZE_3_D
Reset:	soft

DWord	Bit	Description
0	31	**Enable** Access: Double Buffered This field enables the normalization of FP16 pixels with the specified normalization factor.
	30:16	**Reserved** Access: RO Format: MBZ
	15:0	**Normalization Factor** Access: Double Buffered **Description** This field specifies the normalization factor in the FP16 format. This programmed value is multipled with the input pixel value and normalized to range -4.0 to 4.0, exclusive. Out of bound values get clamped to be within the range from -4.0 to 4.0, exclusive. The programmed half float value must be a positive and not de-normalized, zero or NAN.

PLANE_POS

PLANE_POS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	7048Ch-7048Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_A
Reset:	soft
Address:	7058Ch-7058Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_A
Reset:	soft
Address:	7148Ch-7148Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_B
Reset:	soft
Address:	7158Ch-7158Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_B
Reset:	soft
Address:	7248Ch-7248Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_C
Reset:	soft
Address:	7258Ch-7258Fh
Name:	Plane Position
ShortName:	PLANE_POS_5_C
Reset:	soft
Address:	7348Ch-7348Fh
Name:	Plane Position
ShortName:	PLANE_POS_4_D
Reset:	soft
Address:	7358Ch-7358Fh

PLANE_POS	
Name:	Plane Position
ShortName:	PLANE_POS_5_D
Reset:	soft
Address:	7018Ch-7018Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_A
Reset:	soft
Address:	7028Ch-7028Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_A
Reset:	soft
Address:	7038Ch-7038Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_A
Reset:	soft
Address:	7118Ch-7118Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_B
Reset:	soft
Address:	7128Ch-7128Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_B
Reset:	soft
Address:	7138Ch-7138Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_B
Reset:	soft
Address:	7218Ch-7218Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_C
Reset:	soft
Address:	7228Ch-7228Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_C
Reset:	soft
Address:	7238Ch-7238Fh

PLANE_POS	
Name:	Plane Position
ShortName:	PLANE_POS_3_C
Reset:	soft
Address:	7318Ch-7318Fh
Name:	Plane Position
ShortName:	PLANE_POS_1_D
Reset:	soft
Address:	7328Ch-7328Fh
Name:	Plane Position
ShortName:	PLANE_POS_2_D
Reset:	soft
Address:	7338Ch-7338Fh
Name:	Plane Position
ShortName:	PLANE_POS_3_D
Reset:	soft
Address:	70894h-70897h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_1_A
Reset:	soft
Address:	708B4h-708B7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_2_A
Reset:	soft
Address:	708D4h-708D7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_3_A
Reset:	soft
Address:	708F4h-708F7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_4_A
Reset:	soft
Address:	70924h-70927h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_5_A
Reset:	soft
Address:	71894h-71897h

PLANE_POS	
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_1_B
Reset:	soft
Address:	718B4h-718B7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_2_B
Reset:	soft
Address:	718D4h-718D7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_3_B
Reset:	soft
Address:	718F4h-718F7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_4_B
Reset:	soft
Address:	71924h-71927h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_5_B
Reset:	soft
Address:	72894h-72897h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_1_C
Reset:	soft
Address:	728B4h-728B7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_2_C
Reset:	soft
Address:	728D4h-728D7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_3_C
Reset:	soft
Address:	728F4h-728F7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_4_C
Reset:	soft
Address:	72924h-72927h

PLANE_POS

Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_5_C
Reset:	soft

Address:	73894h-73897h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_1_D
Reset:	soft

Address:	738B4h-738B7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_2_D
Reset:	soft

Address:	738D4h-738D7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_3_D
Reset:	soft

Address:	738F4h-738F7h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_4_D
Reset:	soft

Address:	73924h-73927h
Name:	Selective Fetch Plane Position
ShortName:	SEL_FETCH_PLANE_POS_5_D
Reset:	soft

This register specifies the screen position of the plane. The origin of the plane position is always the upper left corner of the display pipe source image area. When plane scaling is not enabled on this plane, this is the position of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window position is the position of the plane when blended with other planes on this pipe. When performing rotation, the plane image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.

Restriction

When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size. When plane scaling is enabled on this plane, the X and Y positions must be programmed to 0.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ

<table>
<tr><th colspan="3">PLANE_POS</th></tr>
<tr><td></td><td>28:16</td><td>Y Position<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This specifies the vertical position of the plane upper left corner in lines.</td></tr>
<tr><td></td><td>15:13</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>12:0</td><td>X Position<table><tr><td>Access:</td><td>Double Buffered</td></tr></table>This specifies the horizontal position of the plane upper left corner in pixels.</td></tr>
</table>

PLANE_POST_CSC_GAMC_DATA

PLANE_POST_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704DCh-704DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_A
Reset:	soft
Address:	705DCh-705DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_A
Reset:	soft
Address:	714DCh-714DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_B
Reset:	soft
Address:	715DCh-715DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_B
Reset:	soft
Address:	724DCh-724DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_C
Reset:	soft
Address:	725DCh-725DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_C
Reset:	soft
Address:	734DCh-734DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_4_D
Reset:	soft
Address:	735DCh-735DFh

PLANE_POST_CSC_GAMC_DATA

Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_5_D
Reset:	soft

PLANE_POST_CSC_GAMC_INDEX and PLANE_POST_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data after plane Color Space Conversion.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and16 fractional. The 33rd, 34th and 35th entries are stored as19 bits per color in an unsigned 3.16 format with 3 integer and16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Plane Post-CSC Gamma correction gets enabled or disabled based on the 'Plane Gamma Disable' bit in the 'PLANE_COLOR_CTL' register. The same set of values is used for gamma correction of the red, blue and green channels.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing in Direct mode. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description	
0	31:19	**Reserved**	
		Access:	RO
		Format:	MBZ
	18:0	**Gamma Value**	
		Default Value:	00000000000000000b
		Access:	Double Buffered
		Format:	U3.16

PLANE_POST_CSC_GAMC_DATA_ENH

PLANE_POST_CSC_GAMC_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	701DCh-701DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_A
Reset:	soft
Address:	702DCh-702DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_A
Reset:	soft
Address:	703DCh-703DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_A
Reset:	soft
Address:	711DCh-711DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_B
Reset:	soft
Address:	712DCh-712DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_B
Reset:	soft
Address:	713DCh-713DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_B
Reset:	soft
Address:	721DCh-721DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_C
Reset:	soft
Address:	722DCh-722DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_C

PLANE_POST_CSC_GAMC_DATA_ENH

Reset:	soft
Address:	723DCh-723DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_C
Reset:	soft
Address:	731DCh-731DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_1_D
Reset:	soft
Address:	732DCh-732DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_2_D
Reset:	soft
Address:	733DCh-733DFh
Name:	Plane Post CSC Gamma Data
ShortName:	PLANE_POST_CSC_GAMC_DATA_ENH_3_D
Reset:	soft

PLANE_POST_CSC_GAMC_INDEX and PLANE_POST_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional. The 33rd, 34th and 35th entries are stored as27 bits per color in an unsigned 3.24 format with 3 integer and 24 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Pipe CSC Enable" bit in the plane control register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.
To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the

PLANE_POST_CSC_GAMC_DATA_ENH

34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.
For HDR tone mapping usages, only the first 33 entries gets used. The entries are used either in an unsigned 0.24 format or unsigned 8.16 format based on PLANE_COLOR_CTL->Plane Gamma Multiplier Precision programming.

Restriction
The gamma curve must be flat or increasing, never decreasing when used in the direct lookup mode. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ
	26:0	**Gamma Value** Default Value: 00000000000000000000000000b Access: R/W Format: U3.24

PLANE_POST_CSC_GAMC_INDEX

PLANE_POST_CSC_GAMC_INDEX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704D8h-704DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_A
Reset:	soft
Address:	705D8h-705DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_A
Reset:	soft
Address:	714D8h-714DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_B
Reset:	soft
Address:	715D8h-715DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_B
Reset:	soft
Address:	724D8h-724DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_C
Reset:	soft
Address:	725D8h-725DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_5_C
Reset:	soft
Address:	734D8h-734DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_4_D
Reset:	soft
Address:	735D8h-735DBh

PLANE_POST_CSC_GAMC_INDEX

Name: Plane Post CSC Gamma Index
ShortName: PLANE_POST_CSC_GAMC_INDEX_5_D
Reset: soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: Double Buffered This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:6	**Reserved** Access: RO Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. Value: [0,34] – Name:

PLANE_POST_CSC_GAMC_INDEX_ENH

PLANE_POST_CSC_GAMC_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	701D8h-701DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_A
Reset:	soft
Address:	702D8h-702DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_A
Reset:	soft
Address:	703D8h-703DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_A
Reset:	soft
Address:	711D8h-711DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_B
Reset:	soft
Address:	712D8h-712DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_B
Reset:	soft
Address:	713D8h-713DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_B
Reset:	soft
Address:	721D8h-721DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_C
Reset:	soft
Address:	722D8h-722DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_C

PLANE_POST_CSC_GAMC_INDEX_ENH

Reset:	soft
Address:	723D8h-723DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_C
Reset:	soft
Address:	731D8h-731DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_1_D
Reset:	soft
Address:	732D8h-732DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_2_D
Reset:	soft
Address:	733D8h-733DBh
Name:	Plane Post CSC Gamma Index
ShortName:	PLANE_POST_CSC_GAMC_INDEX_ENH_3_D
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: R/W This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:6	**Reserved** Access: RO Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read

PLANE_POST_CSC_GAMC_INDEX_ENH		
		here, and the index will roll over to 0 after reaching the end of the allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.

Value	Name
[0,34]	

PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH

PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	70178h-7017Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_1_A
Reset:	soft
Address:	70278h-7027Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_2_A
Reset:	soft
Address:	70378h-7037Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_3_A
Reset:	soft
Address:	71178h-7117Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_1_B
Reset:	soft
Address:	71278h-7127Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_2_B
Reset:	soft
Address:	71378h-7137Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_3_B
Reset:	soft
Address:	72178h-7217Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_1_C
Reset:	soft
Address:	72278h-7227Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_2_C

PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH

Reset:	soft

Address:	72378h-7237Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_3_C
Reset:	soft

Address:	73178h-7317Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_1_D
Reset:	soft

Address:	73278h-7327Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_2_D
Reset:	soft

Address:	73378h-7337Bh
Name:	Plane Post CSC Gamma Luma Coefficients
ShortName:	PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH_3_D
Reset:	soft

This register contains the coefficients to calculate the luminance of incoming pixels which is used to address into the gamma LUT. The pixel luminance is calculated using the following formula:
luma = (Kr * red) + (Kg * green) + (Kb * blue)
All coefficients have a precision of 0.9. Multiply the desired coefficient by 2^9 to get programming value

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:20	**Red Coefficient** Access: Double Buffered This field contains the red coefficient (Kr) Value: 87h — Name: **[Default]** — Description: 0.2627
	19	**Reserved** Access: RO Format: MBZ
	18:10	**Green Coefficient** Access: Double Buffered This field contains the green coefficient (Kg)

PLANE_POST_CSC_GAMC_LUMA_COEFF_ENH

		Value / **Name** / **Description** 15bh / **[Default]** / 0.6780
	9	**Reserved** Access: RO Format: MBZ
	8:0	**Blue Coefficient** Access: Double Buffered This field contains the blue coefficient (Kb) **Value** / **Name** / **Description** 1eh / **[Default]** / 0.0593

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70164h-70167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_A
Reset:	soft
Address:	70264h-70267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_A
Reset:	soft
Address:	70364h-70367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_A
Reset:	soft
Address:	71164h-71167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_B
Reset:	soft
Address:	71264h-71267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_B
Reset:	soft
Address:	71364h-71367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_B
Reset:	soft
Address:	72164h-72167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_C
Reset:	soft
Address:	72264h-72267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_C

PLANE_POST_CSC_GAMC_SEG0_DATA_ENH

Reset:	soft
Address:	72364h-72367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_C
Reset:	soft
Address:	73164h-73167h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_1_D
Reset:	soft
Address:	73264h-73267h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_2_D
Reset:	soft
Address:	73364h-73367h
Name:	Plane Post CSC Gamma Segment0 Data
ShortName:	PLANE_POST_CSC_GAMC_SEG0_DATA_ENH_3_D
Reset:	soft

PLANE_POST_CSC_GAMC_SEG0_INDEX and PLANE_POST_CSC_GAMC_SEG0_DATA registers are used to program the segment 0 values of the HDR tone mapping curve.
The entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**Gamma Value** Default Value: 000000000000000000000000b Access: R/W Format: U0.24

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	70160h-70163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_A
Reset:	soft
Address:	70260h-70263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_A
Reset:	soft
Address:	70360h-70363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_A
Reset:	soft
Address:	71160h-71163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_B
Reset:	soft
Address:	71260h-71263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_B
Reset:	soft
Address:	71360h-71363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_B
Reset:	soft
Address:	72160h-72163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_C
Reset:	soft
Address:	72260h-72263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_C

PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH

Reset:	soft

Address:	72360h-72363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_C
Reset:	soft

Address:	73160h-73163h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_1_D
Reset:	soft

Address:	73260h-73263h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_2_D
Reset:	soft

Address:	73360h-73363h
Name:	Plane Post CSC Gamma Segment0 Index
ShortName:	PLANE_POST_CSC_GAMC_SEG0_INDEX_ENH_3_D
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: R/W This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:4	**Reserved** Access: RO Format: MBZ
	3:0	**Index Value** Access: Write/Read Status This index controls access to the segment 0of plane postcolor space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read

here, and the index will roll over to 0 after reaching the end of the allowed range.
While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value.

Value	Name
[0,8]	

PLANE_PRE_CSC_GAMC_DATA

PLANE_PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704D4h-704D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_A
Reset:	soft
Address:	705D4h-705D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_A
Reset:	soft
Address:	714D4h-714D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_B
Reset:	soft
Address:	715D4h-715D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_B
Reset:	soft
Address:	724D4h-724D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_C
Reset:	soft
Address:	725D4h-725D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_C
Reset:	soft
Address:	734D4h-734D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_4_D
Reset:	soft
Address:	735D4h-735D7h

PLANE_PRE_CSC_GAMC_DATA

Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_5_D
Reset:	soft

PLANE_PRE_CSC_GAMC_INDEX and PLANE_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 33 gamma entries to create the result value. The first 32 entries are stored as16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 33rd, 34th and 35th entries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 33rd and 34th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 34th and 35th gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Plane Pre-CSC Gamma correction gets enabled or disabled based on the 'Plane Pre CSC Gamma Enable'bit in the 'PLANE_COLOR_CTL'register. The same set of values is used for gamma correction of the red, blue and green channels.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 32 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 34th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 35th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:0	**Gamma Value** Default Value: 00000000000000000b Access: Double Buffered Format: U3.16

PLANE_PRE_CSC_GAMC_DATA_ENH

PLANE_PRE_CSC_GAMC_DATA_ENH	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	701D4h-701D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_A
Reset:	soft
Address:	702D4h-702D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_A
Reset:	soft
Address:	703D4h-703D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_A
Reset:	soft
Address:	711D4h-711D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_B
Reset:	soft
Address:	712D4h-712D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_B
Reset:	soft
Address:	713D4h-713D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_B
Reset:	soft
Address:	721D4h-721D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_C
Reset:	soft
Address:	722D4h-722D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_C

PLANE_PRE_CSC_GAMC_DATA_ENH

Reset:	soft
Address:	723D4h-723D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_C
Reset:	soft
Address:	731D4h-731D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_1_D
Reset:	soft
Address:	732D4h-732D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_2_D
Reset:	soft
Address:	733D4h-733D7h
Name:	Plane Pre CSC Gamma Data
ShortName:	PLANE_PRE_CSC_GAMC_DATA_ENH_3_D
Reset:	soft

PLANE_PRE_CSC_GAMC_INDEX and PLANE_PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the plane pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 129 gamma entries to create the result value. The first 128 entries are stored as 24 bits per color in an unsigned 0.24 format with 0 integer and 24 fractional. The 129th, 130th and 131th entries are stored as 27 bits per color in an unsigned 3.24 format with 3 integer and 24 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 129th and 130th gamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 130th and 131st gamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre-CSC Gamma correction gets enabled or disabled based on the "Plane Pre CSC Gamma Enable" bit in the plane color control register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.

PLANE_PRE_CSC_GAMC_DATA_ENH

Programming Notes
To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 128 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 129th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 130th gamma entry.

Restriction
The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ
	26:0	**Gamma Value** Default Value: 00000000000000000000000000b Access: Double Buffered Format: U3.24

PLANE_PRE_CSC_GAMC_INDEX

PLANE_PRE_CSC_GAMC_INDEX	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	704D0h-704D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_A
Reset:	soft
Address:	705D0h-705D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_A
Reset:	soft
Address:	714D0h-714D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_B
Reset:	soft
Address:	715D0h-715D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_B
Reset:	soft
Address:	724D0h-724D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_C
Reset:	soft
Address:	725D0h-725D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_5_C
Reset:	soft
Address:	734D0h-734D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_4_D
Reset:	soft
Address:	735D0h-735D3h

PLANE_PRE_CSC_GAMC_INDEX

Name: Plane Pre CSC Gamma Index
ShortName: PLANE_PRE_CSC_GAMC_INDEX_5_D
Reset: soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: Double Buffered This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:6	**Reserved** Access: RO Format: MBZ
	5:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. Value: [0,34]

PLANE_PRE_CSC_GAMC_INDEX_ENH

PLANE_PRE_CSC_GAMC_INDEX_ENH	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
Address:	701D0h-701D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_A
Reset:	soft
Address:	702D0h-702D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_A
Reset:	soft
Address:	703D0h-703D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_A
Reset:	soft
Address:	711D0h-711D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_B
Reset:	soft
Address:	712D0h-712D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_B
Reset:	soft
Address:	713D0h-713D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_B
Reset:	soft
Address:	721D0h-721D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_C
Reset:	soft
Address:	722D0h-722D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_C

PLANE_PRE_CSC_GAMC_INDEX_ENH

Reset:	soft

Address:	723D0h-723D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_C
Reset:	soft

Address:	731D0h-731D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_1_D
Reset:	soft

Address:	732D0h-732D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_2_D
Reset:	soft

Address:	733D0h-733D3h
Name:	Plane Pre CSC Gamma Index
ShortName:	PLANE_PRE_CSC_GAMC_INDEX_ENH_3_D
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: Double Buffered This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:8	**Reserved** Access: RO Format: MBZ
	7:0	**Index Value** Access: Write/Read Status This index controls access to the array of plane pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire

PLANE_PRE_CSC_GAMC_INDEX_ENH		
		allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. **Value** / **Name** [0,130] /

PLANE_SIZE

PLANE_SIZE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70490h-70493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_A
Reset:	soft
Address:	70590h-70593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_A
Reset:	soft
Address:	71490h-71493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_B
Reset:	soft
Address:	71590h-71593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_B
Reset:	soft
Address:	72490h-72493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_C
Reset:	soft
Address:	72590h-72593h
Name:	Plane Size
ShortName:	PLANE_SIZE_5_C
Reset:	soft
Address:	73490h-73493h
Name:	Plane Size
ShortName:	PLANE_SIZE_4_D
Reset:	soft
Address:	73590h-73593h

PLANE_SIZE	
Name:	Plane Size
ShortName:	PLANE_SIZE_5_D
Reset:	soft
Address:	70190h-70193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_A
Reset:	soft
Address:	70290h-70293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_A
Reset:	soft
Address:	70390h-70393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_A
Reset:	soft
Address:	71190h-71193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_B
Reset:	soft
Address:	71290h-71293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_B
Reset:	soft
Address:	71390h-71393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_B
Reset:	soft
Address:	72190h-72193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_C
Reset:	soft
Address:	72290h-72293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_C
Reset:	soft
Address:	72390h-72393h

PLANE_SIZE	
Name:	Plane Size
ShortName:	PLANE_SIZE_3_C
Reset:	soft
Address:	73190h-73193h
Name:	Plane Size
ShortName:	PLANE_SIZE_1_D
Reset:	soft
Address:	73290h-73293h
Name:	Plane Size
ShortName:	PLANE_SIZE_2_D
Reset:	soft
Address:	73390h-73393h
Name:	Plane Size
ShortName:	PLANE_SIZE_3_D
Reset:	soft
Address:	70898h-7089Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_1_A
Reset:	soft
Address:	708B8h-708BBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_2_A
Reset:	soft
Address:	708D8h-708DBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_3_A
Reset:	soft
Address:	708F8h-708FBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_4_A
Reset:	soft
Address:	70928h-7092Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_5_A
Reset:	soft
Address:	71898h-7189Bh

PLANE_SIZE	
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_1_B
Reset:	soft
Address:	718B8h-718BBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_2_B
Reset:	soft
Address:	718D8h-718DBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_3_B
Reset:	soft
Address:	718F8h-718FBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_4_B
Reset:	soft
Address:	71928h-7192Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_5_B
Reset:	soft
Address:	72898h-7289Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_1_C
Reset:	soft
Address:	728B8h-728BBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_2_C
Reset:	soft
Address:	728D8h-728DBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_3_C
Reset:	soft
Address:	728F8h-728FBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_4_C
Reset:	soft
Address:	72928h-7292Bh

PLANE_SIZE

Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_5_C
Reset:	soft

Address:	73898h-7389Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_1_D
Reset:	soft

Address:	738B8h-738BBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_2_D
Reset:	soft

Address:	738D8h-738DBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_3_D
Reset:	soft

Address:	738F8h-738FBh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_4_D
Reset:	soft

Address:	73928h-7392Bh
Name:	Selective Fetch Plane Size
ShortName:	SEL_FETCH_PLANE_SIZE_5_D
Reset:	soft

This register specifies the plane source size, the size of the image fetched from the frame buffer. When plane scaling is not enabled on this plane, this is the size of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window size is the size of the plane when blended with other planes on this pipe.

Restriction

When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.

For OLED compensation plane size restrictions, refer to PIPE_MISC->OLED Compensation (bit[12]).

Height and Width restrictions are specified in the following table. For formats not specified in the table, both odd and even sizes are supported.

PixelFormat	Rotate	Width	Height
YUV 420 Planar - NV12	All	Even	Even
YUV 420 Planar - P01x	All	Even	Even
YUV 422	All	Even	Even

PLANE_SIZE

RGB565	90, 270	Even	Even

If Plane Scaling or using the Chroma Up-Sampler (CUS) for this plane, please refer to **PS_CTRL** or **PLANE_CUS_CTL** respectively, for further size restrictions.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Height** Access: Double Buffered This specifies the height of the plane in lines. The value in the register is the height minus one. **Restriction** The height must be at least one line when non-interlaced, two lines when interlaced. The height is limited to maximum of 4320 lines. Refer to size restrictions within PS_CTRL when plane scaling is enabled.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Width** Access: Double Buffered This specifies the width of the plane in pixels. The value in the register is the width minus one. **Restriction** The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. For YUV4:2:0 (NV12), the UV plane must be greater than or equal to 8 and the Y plane must be greater than or equal to 16. The width must be greater than or equal to 4 for 32bpp, YUV212 and YUV216 formats, greater than or equal to 8 for 16bpp formats, and greater than or equal to 16 for 8bpp formats. The width must be greater than or equal to 2 for 64bpp formats. The width must be greater than or equal to 8 for P010, P012 and P016 formats. The width should be less than or equal to the stride in pixels. For planar YUV 420 formats, refer to chroma upsampler size restrictions in PLANE_CUS_CTL register. **Tiling format** / **Bytes per pixel** / **Max Width supported in pixels** Linear, X Tiling / 1,2,4,8 / 5120 Y Tiling / 1,2,4,8 / 5120

PLANE_STRIDE

PLANE_STRIDE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70488h-7048Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_A
Reset:	soft
Address:	70588h-7058Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_A
Reset:	soft
Address:	71488h-7148Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_B
Reset:	soft
Address:	71588h-7158Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_B
Reset:	soft
Address:	72488h-7248Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_C
Reset:	soft
Address:	72588h-7258Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_C
Reset:	soft
Address:	73488h-7348Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_4_D
Reset:	soft
Address:	73588h-7358Bh

PLANE_STRIDE	
Name:	Plane Stride
ShortName:	PLANE_STRIDE_5_D
Reset:	soft
Address:	70188h-7018Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_A
Reset:	soft
Address:	70288h-7028Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_A
Reset:	soft
Address:	70388h-7038Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_A
Reset:	soft
Address:	71188h-7118Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_B
Reset:	soft
Address:	71288h-7128Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_B
Reset:	soft
Address:	71388h-7138Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_B
Reset:	soft
Address:	72188h-7218Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_C
Reset:	soft
Address:	72288h-7228Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_C
Reset:	soft
Address:	72388h-7238Bh

PLANE_STRIDE

Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_C
Reset:	soft

Address:	73188h-7318Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_1_D
Reset:	soft

Address:	73288h-7328Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_2_D
Reset:	soft

Address:	73388h-7338Bh
Name:	Plane Stride
ShortName:	PLANE_STRIDE_3_D
Reset:	soft

This register may be updated through MMIO writes or through command streamer initiated synchronous flips.

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17:12	**Reserved** Access: RO Format: MBZ
	11:0	**Stride** Access: Double Buffered This field specifies the stride for the plane. The field is used to determine the line-to-line increment for the plane. For Linear memory, this field specifies the stride in chunks of 64 bytes (1 cache line). If the programmed value is 100, the actual stride = 100 * 64 = 6400 bytes. For X-Tiled & Tile 4memory, this field specifies the stride in number of tiles. For Tile X, if the programmed value is 10, the actual stride = 10 * 512 (X tile width) = 5120 bytes. For Tile 4, if the programmed value is 10, the actual stride = 10 * 128 (tile 4 width) = 1280 bytes. Tile Format / Width in bytes: Tile X: 512 Tile 4: 128

PLANE_STRIDE

Restriction:
For YUV planar (NV12 or P0xx) plane pixel formats, the stride calculated in bytes should be equal for the Y and UV surfaces.
The stride in bytes must not exceed the of the size of 128K bytes. For pixel formats of 64bpp, the maximum stride in tiles as listed below, will allow for a 16K pixel surface. For pixel formats less than 64bpp, adjustment of PLANE_OFFSET will allow for display of portions of a 128K Byte surface. For 8bpp formats, PLANE_SURF may need an adjustment as well.

Tile Format	Maximum Stride in tiles
Linear	2048
X Tiling	256
Tile 4	1024

PLANE_SURF

PLANE_SURF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of left or right eye vertical blank (selectable), pipe not enabled, or plane not enabled
Address:	7049Ch-7049Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_A
Reset:	soft
Address:	7059Ch-7059Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_A
Reset:	soft
Address:	7149Ch-7149Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_B
Reset:	soft
Address:	7159Ch-7159Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_B
Reset:	soft
Address:	7249Ch-7249Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_C
Reset:	soft
Address:	7259Ch-7259Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_C
Reset:	soft
Address:	7349Ch-7349Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_4_D
Reset:	soft
Address:	7359Ch-7359Fh

PLANE_SURF	
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_5_D
Reset:	soft
Address:	7019Ch-7019Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_A
Reset:	soft
Address:	7029Ch-7029Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_A
Reset:	soft
Address:	7039Ch-7039Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_A
Reset:	soft
Address:	7119Ch-7119Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_B
Reset:	soft
Address:	7129Ch-7129Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_B
Reset:	soft
Address:	7139Ch-7139Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_B
Reset:	soft
Address:	7219Ch-7219Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_C
Reset:	soft
Address:	7229Ch-7229Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_C
Reset:	soft
Address:	7239Ch-7239Fh

PLANE_SURF

Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_C
Reset:	soft

Address:	7319Ch-7319Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_1_D
Reset:	soft

Address:	7329Ch-7329Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_2_D
Reset:	soft

Address:	7339Ch-7339Fh
Name:	Plane Surface Base Address
ShortName:	PLANE_SURF_3_D
Reset:	soft

Writes to this register arm primary registers for this pipe. A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer-initiated flips. Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank. Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank. Stereo 3D synchronous updates (stereo 3D command streamer flips or synchronous MMIO writes while stereo 3D is enabled) will update at the start of either the left or right eye vertical blank, selectable by the plane control register stereo surface vblank mask.

Double buffering control does not apply to PLANE_SURF updates that occur when the plane is disabled. An interrupt event is generated immediately when the PLANE_SURF is written. If the interrupt is unmasked, the interrupt is logged in the IIR.

Asynchronous flip completion time depends greatly on how much data has been prefetched for power savings, and can take up to 1 full frame to complete. For faster flip completion, disable FBC and render compression and allocate a small amount of data buffer for the plane.

DWord	Bit	Description
0	31:12	**Surface Base Address** Access: Double Buffered Format: GraphicsAddress[31:12]
	11	**Reserved** Access: Double Buffered
	10:7	**Reserved** Access: RO Format: MBZ

PLANE_SURF

	6:4	**Reserved** Access: Double Buffered
	3	**Ring Flip Source** Access: Double Buffered This bit indicates if the source of the last ring flip was CS or BCS. This will determine where the flip done response is sent. Value: 0b — Name: CS Value: 1b — Name: BCS
	2	**Reserved** Access: Double Buffered
	1:0	**Reserved** Access: RO Format: MBZ

PLANE_SURFLIVE

PLANE_SURFLIVE	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	704ACh-704AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_A
Reset:	soft
Address:	704BCh-704BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_A
Reset:	soft
Address:	705ACh-705AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_A
Reset:	soft
Address:	705BCh-705BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_A
Reset:	soft
Address:	714ACh-714AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_B
Reset:	soft
Address:	714BCh-714BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_B
Reset:	soft
Address:	715ACh-715AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_B
Reset:	soft
Address:	715BCh-715BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_B
Reset:	soft

PLANE_SURFLIVE	
Address:	724ACh-724AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_C
Reset:	soft
Address:	724BCh-724BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_C
Reset:	soft
Address:	725ACh-725AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_C
Reset:	soft
Address:	725BCh-725BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_C
Reset:	soft
Address:	734ACh-734AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_4_D
Reset:	soft
Address:	734BCh-734BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_4_D
Reset:	soft
Address:	735ACh-735AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_5_D
Reset:	soft
Address:	735BCh-735BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_5_D
Reset:	soft
Address:	701ACh-701AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_A
Reset:	soft

PLANE_SURFLIVE	
Address:	701BCh-701BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_A
Reset:	soft
Address:	702ACh-702AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_A
Reset:	soft
Address:	702BCh-702BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_A
Reset:	soft
Address:	703ACh-703AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_A
Reset:	soft
Address:	703BCh-703BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_A
Reset:	soft
Address:	711ACh-711AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_B
Reset:	soft
Address:	711BCh-711BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_B
Reset:	soft
Address:	712ACh-712AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_B
Reset:	soft
Address:	712BCh-712BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_B
Reset:	soft

PLANE_SURFLIVE	
Address:	713ACh-713AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_B
Reset:	soft
Address:	713BCh-713BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_B
Reset:	soft
Address:	721ACh-721AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_C
Reset:	soft
Address:	721BCh-721BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_C
Reset:	soft
Address:	722ACh-722AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_C
Reset:	soft
Address:	722BCh-722BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_C
Reset:	soft
Address:	723ACh-723AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_C
Reset:	soft
Address:	723BCh-723BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_C
Reset:	soft
Address:	731ACh-731AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_1_D
Reset:	soft

PLANE_SURFLIVE

Address:	731BCh-731BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_1_D
Reset:	soft

Address:	732ACh-732AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_2_D
Reset:	soft

Address:	732BCh-732BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_2_D
Reset:	soft

Address:	733ACh-733AFh
Name:	Plane Live Surface Base Address
ShortName:	PLANE_SURFLIVE_3_D
Reset:	soft

Address:	733BCh-733BFh
Name:	Plane Live Left Surface Base Address
ShortName:	PLANE_LEFT_SURFLIVE_3_D
Reset:	soft

There is one instance of this register for each plane.

DWord	Bit	Description
0	31:12	**Live Surface Base Address** Access: RO This gives the live value of the surface base address as being currently used for the plane.
	11	**Reserved** Access: RO Format: MBZ
	10:9	**Reserved**
	8:0	**Reserved** Access: RO Format: MBZ

PLANE_VFID

PLANE_VFID	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70570h-70573h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_4_A
Reset:	soft
Address:	70670h-70673h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_5_A
Reset:	soft
Address:	71570h-71573h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_4_B
Reset:	soft
Address:	71670h-71673h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_5_B
Reset:	soft
Address:	72570h-72573h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_4_C
Reset:	soft
Address:	72670h-72673h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_5_C
Reset:	soft
Address:	73570h-73573h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_4_D
Reset:	soft
Address:	73670h-73673h

PLANE_VFID	
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_5_D
Reset:	soft
Address:	70270h-70273h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_1_A
Reset:	soft
Address:	70370h-70373h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_2_A
Reset:	soft
Address:	70470h-70473h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_3_A
Reset:	soft
Address:	71270h-71273h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_1_B
Reset:	soft
Address:	71370h-71373h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_2_B
Reset:	soft
Address:	71470h-71473h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_3_B
Reset:	soft
Address:	72270h-72273h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_1_C
Reset:	soft
Address:	72370h-72373h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_2_C
Reset:	soft
Address:	72470h-72473h

PLANE_VFID

Name:	Plane Virtual Function
ShortName:	PLANE_VFID_3_C
Reset:	soft

Address:	73270h-73273h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_1_D
Reset:	soft

Address:	73370h-73373h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_2_D
Reset:	soft

Address:	73470h-73473h
Name:	Plane Virtual Function
ShortName:	PLANE_VFID_3_D
Reset:	soft

This register is programmed with the Virtual Function ID or PASID assigned to this plane.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**VFID** Access: Double Buffered The Virtual Function ID or PASID assigned to this plane. **Restriction** This value must be set to 0 if LMTT is not enabled.

PLANE_WM

PLANE_WM	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF/CUR_BASE or plane/cursor not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank, plane not enabled, or pipe not enabled
Address:	70140h-70143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_A
Reset:	soft
Address:	70144h-70147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_A
Reset:	soft
Address:	70148h-7014Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_A
Reset:	soft
Address:	7014Ch-7014Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_A
Reset:	soft
Address:	70150h-70153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_A
Reset:	soft
Address:	70154h-70157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_A
Reset:	soft
Address:	70158h-7015Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_A
Reset:	soft
Address:	7015Ch-7015Fh

PLANE_WM	
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_A
Reset:	soft
Address:	70168h-7016Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_A
Reset:	soft
Address:	71140h-71143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_B
Reset:	soft
Address:	71144h-71147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_B
Reset:	soft
Address:	71148h-7114Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_B
Reset:	soft
Address:	7114Ch-7114Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_B
Reset:	soft
Address:	71150h-71153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_B
Reset:	soft
Address:	71154h-71157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_B
Reset:	soft
Address:	71158h-7115Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_B
Reset:	soft
Address:	7115Ch-7115Fh

PLANE_WM	
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_B
Reset:	soft
Address:	71168h-7116Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_B
Reset:	soft
Address:	72140h-72143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_C
Reset:	soft
Address:	72144h-72147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_C
Reset:	soft
Address:	72148h-7214Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_C
Reset:	soft
Address:	7214Ch-7214Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_C
Reset:	soft
Address:	72150h-72153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_C
Reset:	soft
Address:	72154h-72157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_C
Reset:	soft
Address:	72158h-7215Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_C
Reset:	soft
Address:	7215Ch-7215Fh

PLANE_WM	
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_C
Reset:	soft
Address:	72168h-7216Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_C
Reset:	soft
Address:	73140h-73143h
Name:	Cursor Watermarks
ShortName:	CUR_WM_0_D
Reset:	soft
Address:	73144h-73147h
Name:	Cursor Watermarks
ShortName:	CUR_WM_1_D
Reset:	soft
Address:	73148h-7314Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_2_D
Reset:	soft
Address:	7314Ch-7314Fh
Name:	Cursor Watermarks
ShortName:	CUR_WM_3_D
Reset:	soft
Address:	73150h-73153h
Name:	Cursor Watermarks
ShortName:	CUR_WM_4_D
Reset:	soft
Address:	73154h-73157h
Name:	Cursor Watermarks
ShortName:	CUR_WM_5_D
Reset:	soft
Address:	73158h-7315Bh
Name:	Cursor Watermarks
ShortName:	CUR_WM_6_D
Reset:	soft
Address:	7315Ch-7315Fh

PLANE_WM	
Name:	Cursor Watermarks
ShortName:	CUR_WM_7_D
Reset:	soft
Address:	73168h-7316Bh
Name:	Cursor Transition Watermark
ShortName:	CUR_WM_TRANS_D
Reset:	soft
Address:	70540h-70543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_A
Reset:	soft
Address:	70544h-70547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_A
Reset:	soft
Address:	70548h-7054Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_A
Reset:	soft
Address:	7054Ch-7054Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_A
Reset:	soft
Address:	70550h-70553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_A
Reset:	soft
Address:	70554h-70557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_A
Reset:	soft
Address:	70558h-7055Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_A
Reset:	soft
Address:	7055Ch-7055Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_A
Reset:	soft
Address:	70568h-7056Bh
Name:	Plane Transition Watermark
ShortName:	PLANE_WM_TRANS_4_A
Reset:	soft
Address:	70640h-70643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_A
Reset:	soft
Address:	70644h-70647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_A
Reset:	soft
Address:	70648h-7064Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_A
Reset:	soft
Address:	7064Ch-7064Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_A
Reset:	soft
Address:	70650h-70653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_A
Reset:	soft
Address:	70654h-70657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_A
Reset:	soft
Address:	70658h-7065Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_A
Reset:	soft
Address:	7065Ch-7065Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_A
Reset:	soft
Address:	70668h-7066Bh
Name:	Plane Transition Watermark
ShortName:	PLANE_WM_TRANS_5_A
Reset:	soft
Address:	71540h-71543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_B
Reset:	soft
Address:	71544h-71547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_B
Reset:	soft
Address:	71548h-7154Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_B
Reset:	soft
Address:	7154Ch-7154Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_B
Reset:	soft
Address:	71550h-71553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_B
Reset:	soft
Address:	71554h-71557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_B
Reset:	soft
Address:	71558h-7155Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_B
Reset:	soft
Address:	7155Ch-7155Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_B
Reset:	soft
Address:	71568h-7156Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_B
Reset:	soft
Address:	71640h-71643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_B
Reset:	soft
Address:	71644h-71647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_B
Reset:	soft
Address:	71648h-7164Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_B
Reset:	soft
Address:	7164Ch-7164Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_B
Reset:	soft
Address:	71650h-71653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_B
Reset:	soft
Address:	71654h-71657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_B
Reset:	soft
Address:	71658h-7165Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_B
Reset:	soft
Address:	7165Ch-7165Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_B
Reset:	soft
Address:	71668h-7166Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_B
Reset:	soft
Address:	72540h-72543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_C
Reset:	soft
Address:	72544h-72547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_C
Reset:	soft
Address:	72548h-7254Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_C
Reset:	soft
Address:	7254Ch-7254Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_C
Reset:	soft
Address:	72550h-72553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_C
Reset:	soft
Address:	72554h-72557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_C
Reset:	soft
Address:	72558h-7255Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_C
Reset:	soft
Address:	7255Ch-7255Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_C
Reset:	soft
Address:	72568h-7256Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_C
Reset:	soft
Address:	72640h-72643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_C
Reset:	soft
Address:	72644h-72647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_C
Reset:	soft
Address:	72648h-7264Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_C
Reset:	soft
Address:	7264Ch-7264Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_C
Reset:	soft
Address:	72650h-72653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_C
Reset:	soft
Address:	72654h-72657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_C
Reset:	soft
Address:	72658h-7265Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_C
Reset:	soft
Address:	7265Ch-7265Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_C
Reset:	soft
Address:	72668h-7266Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_C
Reset:	soft
Address:	73540h-73543h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_4_D
Reset:	soft
Address:	73544h-73547h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_4_D
Reset:	soft
Address:	73548h-7354Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_4_D
Reset:	soft
Address:	7354Ch-7354Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_4_D
Reset:	soft
Address:	73550h-73553h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_4_D
Reset:	soft
Address:	73554h-73557h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_4_D
Reset:	soft
Address:	73558h-7355Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_4_D
Reset:	soft
Address:	7355Ch-7355Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_4_D
Reset:	soft
Address:	73568h-7356Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_4_D
Reset:	soft
Address:	73640h-73643h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_5_D
Reset:	soft
Address:	73644h-73647h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_5_D
Reset:	soft
Address:	73648h-7364Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_5_D
Reset:	soft
Address:	7364Ch-7364Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_5_D
Reset:	soft
Address:	73650h-73653h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_5_D
Reset:	soft
Address:	73654h-73657h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_5_D
Reset:	soft
Address:	73658h-7365Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_5_D
Reset:	soft
Address:	7365Ch-7365Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_5_D
Reset:	soft
Address:	73668h-7366Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_5_D
Reset:	soft
Address:	70240h-70243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_A
Reset:	soft
Address:	70244h-70247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_A
Reset:	soft
Address:	70248h-7024Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_A
Reset:	soft
Address:	7024Ch-7024Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_A
Reset:	soft
Address:	70250h-70253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_A
Reset:	soft
Address:	70254h-70257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_A
Reset:	soft
Address:	70258h-7025Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_A
Reset:	soft
Address:	7025Ch-7025Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_A
Reset:	soft
Address:	70268h-7026Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_A
Reset:	soft
Address:	70340h-70343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_A
Reset:	soft
Address:	70344h-70347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_A
Reset:	soft
Address:	70348h-7034Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_A
Reset:	soft
Address:	7034Ch-7034Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_A
Reset:	soft
Address:	70350h-70353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_A
Reset:	soft
Address:	70354h-70357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_A
Reset:	soft
Address:	70358h-7035Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_A
Reset:	soft
Address:	7035Ch-7035Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_A
Reset:	soft
Address:	70368h-7036Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_A
Reset:	soft
Address:	70440h-70443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_A
Reset:	soft
Address:	70444h-70447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_A
Reset:	soft
Address:	70448h-7044Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_A
Reset:	soft
Address:	7044Ch-7044Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_A
Reset:	soft
Address:	70450h-70453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_A
Reset:	soft
Address:	70454h-70457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_A
Reset:	soft
Address:	70458h-7045Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_A
Reset:	soft
Address:	7045Ch-7045Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_A
Reset:	soft
Address:	70468h-7046Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_A
Reset:	soft
Address:	71240h-71243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_B
Reset:	soft
Address:	71244h-71247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_B
Reset:	soft
Address:	71248h-7124Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_B
Reset:	soft
Address:	7124Ch-7124Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_B
Reset:	soft
Address:	71250h-71253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_B
Reset:	soft
Address:	71254h-71257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_B
Reset:	soft
Address:	71258h-7125Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_B
Reset:	soft
Address:	7125Ch-7125Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_B
Reset:	soft
Address:	71268h-7126Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_B
Reset:	soft
Address:	71340h-71343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_B
Reset:	soft
Address:	71344h-71347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_B
Reset:	soft
Address:	71348h-7134Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_B
Reset:	soft
Address:	7134Ch-7134Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_B
Reset:	soft
Address:	71350h-71353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_B
Reset:	soft
Address:	71354h-71357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_B
Reset:	soft
Address:	71358h-7135Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_B
Reset:	soft
Address:	7135Ch-7135Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_B
Reset:	soft
Address:	71368h-7136Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_B
Reset:	soft
Address:	71440h-71443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_B
Reset:	soft
Address:	71444h-71447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_B
Reset:	soft
Address:	71448h-7144Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_B
Reset:	soft
Address:	7144Ch-7144Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_B
Reset:	soft
Address:	71450h-71453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_B
Reset:	soft
Address:	71454h-71457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_B
Reset:	soft
Address:	71458h-7145Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_B
Reset:	soft
Address:	7145Ch-7145Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_B
Reset:	soft
Address:	71468h-7146Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_B
Reset:	soft
Address:	72240h-72243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_C
Reset:	soft
Address:	72244h-72247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_C
Reset:	soft
Address:	72248h-7224Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_C
Reset:	soft
Address:	7224Ch-7224Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_C
Reset:	soft
Address:	72250h-72253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_C
Reset:	soft
Address:	72254h-72257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_C
Reset:	soft
Address:	72258h-7225Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_C
Reset:	soft
Address:	7225Ch-7225Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_C
Reset:	soft
Address:	72268h-7226Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_C
Reset:	soft
Address:	72340h-72343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_C
Reset:	soft
Address:	72344h-72347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_C
Reset:	soft
Address:	72348h-7234Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_C
Reset:	soft
Address:	7234Ch-7234Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_C
Reset:	soft
Address:	72350h-72353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_C
Reset:	soft
Address:	72354h-72357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_C
Reset:	soft
Address:	72358h-7235Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_C
Reset:	soft
Address:	7235Ch-7235Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_C
Reset:	soft
Address:	72368h-7236Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_C
Reset:	soft
Address:	72440h-72443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_C
Reset:	soft
Address:	72444h-72447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_C
Reset:	soft
Address:	72448h-7244Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_C
Reset:	soft
Address:	7244Ch-7244Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_C
Reset:	soft
Address:	72450h-72453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_C
Reset:	soft
Address:	72454h-72457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_C
Reset:	soft
Address:	72458h-7245Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_C
Reset:	soft
Address:	7245Ch-7245Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_C
Reset:	soft
Address:	72468h-7246Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_C
Reset:	soft
Address:	73240h-73243h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_1_D
Reset:	soft
Address:	73244h-73247h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_1_D
Reset:	soft
Address:	73248h-7324Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_1_D
Reset:	soft
Address:	7324Ch-7324Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_1_D
Reset:	soft
Address:	73250h-73253h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_1_D
Reset:	soft
Address:	73254h-73257h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_1_D
Reset:	soft
Address:	73258h-7325Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_1_D
Reset:	soft
Address:	7325Ch-7325Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_1_D
Reset:	soft
Address:	73268h-7326Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_1_D
Reset:	soft
Address:	73340h-73343h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_2_D
Reset:	soft
Address:	73344h-73347h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_2_D
Reset:	soft
Address:	73348h-7334Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_2_D
Reset:	soft
Address:	7334Ch-7334Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_2_D
Reset:	soft
Address:	73350h-73353h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_2_D
Reset:	soft
Address:	73354h-73357h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_2_D
Reset:	soft
Address:	73358h-7335Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_2_D
Reset:	soft
Address:	7335Ch-7335Fh

PLANE_WM	
Name:	Plane Watermarks
ShortName:	PLANE_WM_7_2_D
Reset:	soft
Address:	73368h-7336Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_2_D
Reset:	soft
Address:	73440h-73443h
Name:	Plane Watermarks
ShortName:	PLANE_WM_0_3_D
Reset:	soft
Address:	73444h-73447h
Name:	Plane Watermarks
ShortName:	PLANE_WM_1_3_D
Reset:	soft
Address:	73448h-7344Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_2_3_D
Reset:	soft
Address:	7344Ch-7344Fh
Name:	Plane Watermarks
ShortName:	PLANE_WM_3_3_D
Reset:	soft
Address:	73450h-73453h
Name:	Plane Watermarks
ShortName:	PLANE_WM_4_3_D
Reset:	soft
Address:	73454h-73457h
Name:	Plane Watermarks
ShortName:	PLANE_WM_5_3_D
Reset:	soft
Address:	73458h-7345Bh
Name:	Plane Watermarks
ShortName:	PLANE_WM_6_3_D
Reset:	soft
Address:	7345Ch-7345Fh

PLANE_WM

Name:	Plane Watermarks
ShortName:	PLANE_WM_7_3_D
Reset:	soft

Address:	73468h-7346Bh
Name:	Plane Transition Watermarks
ShortName:	PLANE_WM_TRANS_3_D
Reset:	soft

Programming Notes

There are eight regular watermarks and a transition watermark per plane/cursor. For YUV planar source formats, only the Y surface watermark value should be programmed. Watermark programming instructions are documented separately.

Restriction

For minimum watermark requirements refer to Display Watermark Programming section.

DWord	Bit	Description
0	31	**Enable** Access: Double Buffered This field enables this watermark. All the watermarks at this level for all enabled planes must be enabled before the level will be used. Value: 1b — Name: Enable Value: 0b — Name: Disable
	30	**Reserved** Access: Double Buffered
	29:27	**Reserved** Access: RO Format: MBZ
	26:22	**Reserved** Access: RO Format: MBZ
	21:14	**Lines** Default Value: 01h Access: Double Buffered This field contains the watermark value in lines. Hardware ignores the lines for the transition watermark.

<table>
<tr><th colspan="4">PLANE_WM</th></tr>
<tr><td></td><td>13:12</td><td colspan="2">Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>11</td><td colspan="2">Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>10:0</td><td colspan="2">Blocks<table><tr><td>Default Value:</td><td>007h</td></tr><tr><td>Access:</td><td>Double Buffered</td></tr></table>This field contains the watermark value in blocks of 8 cachelines.</td></tr>
</table>

POISON_DATA_HANDLING_ENABLE

POISON_DATA_HANDLING_ENABLE - POISON_DATA_HANDLING_ENABLE

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 100120h

This register holds the enable for Poison data detection and reporting for Gunit.

DWord	Bit	Description
0	31:2	**Reserved** Access: RO Format: MBZ
	1	**VIRAL POISON ENABLE** Access: R/W _Custom_GTIReset: BUS Controls whether HW will virally poison data sent towards host system if that data may have been corrupted. This could occur if the device previously received poisoned data from the Host, or encountered uncorrectable data from internal data structures or locally attached memory. Host reads to PCI Configuration registers or internal MMIO registers are not affected by the Viral Poison Condition Value: 0b — **[Default]**; 1b
	0	**LOCAL MEMORY POISON ENABLE** Access: R/W _Custom_GTIReset: BUS Enables the detection and reporting of poisoned data on the Local Memory interface, beyond what is required by the PCIe Spec. This bit has no effect on Poison Handling that is required by the PCIe Spec. Value: 0b — **[Default]**; 1b

POISON_DATA_STATUS

POISON_DATA_STATUS - POISON_DATA_STATUS

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 100124h

This register holds the sticky bit which when set will indicate a Poisoned data has been received on IOSF-Primary.

DWord	Bit	Description
0	31:2	**Reserved** Access: RO Format: MBZ
	1	**VIRAL POISON CONDITION** Access: R/W One Clear _Custom_GTIReset: DEV Logs status of the Viral Poison Condition: 0 : HW is not virally poisoning data sent to the Host system 1 : HW is virally poisoning data sent to the Host system Cleared by FLR. Value: 0b **[Default]**; 1b
	0	**ERROR STATUS** Access: R/W One Clear _Custom_GTIReset: DEV Set to 1 when Poisoned data has been received from IOSF-Primary. This sticky bit must survive secondary bus reset/FLR. Value: 0b **[Default]**; 1b

PORT_CL_DW5

PORT_CL_DW5		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	162014h-162017h	
Name:	PORT_CL_DW5	
ShortName:	PORT_CL_DW5_A	
Reset:	global	
Address:	6C014h-6C017h	
Name:	PORT_CL_DW5	
ShortName:	PORT_CL_DW5_B	
Reset:	global	
Address:	160014h-160017h	
Name:	PORT_CL_DW5	
ShortName:	PORT_CL_DW5_C	
Reset:	global	

DWord	Bit	Description
0	31:24	**Force** Default Value: 00010010b Access: R/W
	23	**Reserved** Access: RO Format: MBZ
	22	**Fusevalid Reset** Access: R/W
	21	**Fusevalid Override** Access: R/W
	20	**Fuse Repull** Access: R/W
	19:16	**CRI Clock Count Max** Default Value: 0100b Access: R/W
	15	**Reserved** Access: RO Format: MBZ

PORT_CL_DW5

	14:13	**IOSF PD Count** Access: R/W
	12	**Reserved** Access: RO Format: MBZ
	11:9	**IOSF ClkDiv Sel** Default Value: 010b Access: R/W
	8	**DL Broadcast Enable** Access: R/W This field causes all Tx's to get programmed when writing to a group access offset for a single Tx.
	7	**Reserved** Access: RO Format: MBZ
	6	**Enable Port Staggering** Default Value: 1b Access: R/W
	5	**PG Staggering Control Disable** Default Value: 1b Access: R/W
	4	**CL Power Down Enable** Access: R/W Value: 0b — Name: Disable Value: 1b — Name: Enable
	3	**CRI Clock Select** Default Value: 1b Access: R/W
	2	**Phy Power Ack Override** Access: R/W
	1:0	**SUS Clock Config** Access: R/W

PORT_CL_DW10

PORT_CL_DW10

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162028h-16202Bh
Name:	PORT_CL_DW10
ShortName:	PORT_CL_DW10_A
Reset:	global
Address:	6C028h-6C02Bh
Name:	PORT_CL_DW10
ShortName:	PORT_CL_DW10_B
Reset:	global
Address:	160028h-16002Bh
Name:	PORT_CL_DW10
ShortName:	PORT_CL_DW10_C
Reset:	global

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ
	26:25	**PG Seq Delay Override** Access: R/W PG Sequential Delay Override
	24	**PG Seq Delay Override Enable** Access: R/W PG Sequential Delay Override Enable 0b – Disable 1b – Enable
	23	**ohvpg_ctrl_mipia** Access: R/W MIPI A HVPG Control
	22	**spare 22** Access: R/W Spare 22

PORT_CL_DW10

	21:16	**ospare_cri_ret** Default Value: 000011b Access: R/W ospare_cri_ret[6:0]
	15:12	**Reserved** Access: RO Format: MBZ
	11	**Spare 11** Access: R/W Spare 11
	10	**Spare 10** Access: R/W Spare 10
	9	**Spare 9** Access: R/W Spare 9
	8	**Spare 8** Access: R/W Spare 8
	7:4	**Static Power Down** Access: R/W This field powers down individual lanes for the DDI that is accessed through this instance of the register. To save power, unused lanes should be powered down after link training is complete.

Value	Name	Description
0000b	Power up all lanes	Enable x4
1100b	Power down lanes 3,2	Enable x2
1110b	Power down lanes 3,2,1	Enable x1
0011b	Power down lanes 1,0	Enable x2 Reversed
0111b	Power down lanes 2,1,0	Enable x1 Reversed
1011b	Power down lanes 3,1,0	Enable DSI x1
1010b	Power down lanes 3,1	Enable DSI x2
1000b	Power down lane 3	Enable DSI x3

PORT_CL_DW10

	3	**o_edp4k2k_mode_ovrd_en** Access: R/W eDP power optimized setting **Value** / **Name** 1b: Enable **[Default]** 0b: Disable
	2	**o_edp4k2k_mode_ovrd_val** Access: R/W eDP power optimized setting. Valid only when corresponding enable bit (o_edp4k2k_mode_ovrd_en) is set and specific voltage swing programming is used. **Value** / **Name** 1b: Optimized 0b: Non-optimized
	1	**o_rterm100en_h_ovrd_en** Access: R/W rterm override enable **Value** / **Name** 1b: **[Default]** 0b:
	0	**o_rterm100en_h_ovrd_val** Access: R/W rterm override val valid only when corresponding enable bit (o_rterm100en_h_ovrd_en) is set. **Value** / **Name** 0b: 150 Ohms 1b: 100 Ohms

PORT_CL_DW12

PORT_CL_DW12

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162030h-162033h
Name:	PORT_CL_DW12
ShortName:	PORT_CL_DW12_A
Reset:	global
Address:	6C030h-6C033h
Name:	PORT_CL_DW12
ShortName:	PORT_CL_DW12_B
Reset:	global
Address:	160030h-160033h
Name:	PORT_CL_DW12
ShortName:	PORT_CL_DW12_C
Reset:	global

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**MIPI Lane Enable** Access: R/W 0b: Disable 1b: Enable
	28	**Reserved** Access: RO Format: MBZ
	27	**MIPI Mode Override Enable** Access: R/W 0b: 1b:

PORT_CL_DW12

26	**MIPI Mode Override** Access: R/W Value: 0b — Name: Value: 1b — Name:
25:18	**Reserved** Access: RO Format: MBZ
17:16	**Reserved** Access: RO Format: MBZ
15:12	**Reserved** Access: RO Format: MBZ
11	**Pwr Req Override AUX** Access: R/W Value: 0b — Name: Value: 1b — Name:
10	**Pwr Req Override Enable AUX** Access: R/W Value: 0b — Name: Disable Value: 1b — Name: Enable
9:7	**Reserved** Access: RO Format: MBZ
6	**Phy Status AUX** Access: RO
5	**Reserved** Access: RO Format: MBZ
4	**Power Ack AUX** Access: RO

PORT_CL_DW12

	3:1	**Reserved** Access: RO Format: MBZ
	0	**Lane Enable AUX** Access: R/W Value: 0b — Name: Disable Value: 1b — Name: Enable

PORT_CL_DW15

PORT_CL_DW15

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	16203Ch-16203Fh
Name:	PORT_CL_DW15
ShortName:	PORT_CL_DW15_A
Reset:	global
Address:	6C03Ch-6C03Fh
Name:	PORT_CL_DW15
ShortName:	PORT_CL_DW15_B
Reset:	global
Address:	16003Ch-16003Fh
Name:	PORT_CL_DW15
ShortName:	PORT_CL_DW15_C
Reset:	global

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**HVPG Power Ack** Access: RO Value / Name: 0b; 1b
	28	**HVPG Enable Status** Access: RO Value / Name: 0b; 1b
	27	**Power Ack MIPI** Access: RO

PORT_CL_DW15

		Value: 0b — Name:
		Value: 1b — Name:
	26:22	**Reserved** Access: RO Format: MBZ
	21	**Power Req AUX** Access: RO Value: 0b — Name: Value: 1b — Name:
	20:18	**Reserved** Access: RO Format: MBZ
	17	**Power Ack AUX** Access: RO Value: 0b — Name: Value: 1b — Name:
	16:0	**Reserved** Access: RO Format: MBZ

PORT_CL_DW16

PORT_CL_DW16	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162040h-162043h
Name:	PORT_CL_DW16
ShortName:	PORT_CL_DW16_A
Reset:	global
Address:	6C040h-6C043h
Name:	PORT_CL_DW16
ShortName:	PORT_CL_DW16_B
Reset:	global
Address:	160040h-160043h
Name:	PORT_CL_DW16
ShortName:	PORT_CL_DW16_C
Reset:	global

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**o_hd_ddib_sel_ovrden** Access: R/W DDI B HD Port select override enable
	14	**o_hd_ddib_sel_ovrd** Access: R/W DDI B HD Port select override
	13	**o_hd_ddic_sel_ovrden** Access: R/W DDI C HD Port select override enable
	12	**o_hd_ddic_sel_ovrd** Access: R/W DDI C HD Port select override

PORT_CL_DW16		
	11	**o_hd_ddid_sel_ovrden** Access: R/W DDI D HD Port select override enable
	10	**o_hd_ddid_sel_ovrd** Access: R/W DDI D HD Port select override
	9:8	**Reserved** Access: RO Format: MBZ
	7:4	**ospare_cri[3:0]** Access: R/W reserved
	3	**o_comp_pwrdown_ovrd** Access: R/W Comp Power Down Override
	2	**o_comp_pwrdown_ovrden** Access: R/W Comp Power Down Override Enable
	1	**o_cri_wake_ovrd** Access: R/W CRI Wake Override
	0	**o_cri_wake_ovrden** Access: R/W CRI Wake Override Enable

PORT_COMP_DW0

PORT_COMP_DW0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162100h-162103h
Name:	PORT_COMP_DW0
ShortName:	PORT_COMP_DW0_A
Reset:	global
Address:	6C100h-6C103h
Name:	PORT_COMP_DW0
ShortName:	PORT_COMP_DW0_B
Reset:	global
Address:	160100h-160103h
Name:	PORT_COMP_DW0
ShortName:	PORT_COMP_DW0_C
Reset:	global

DWord	Bit	Description
0	31	**Comp Init** Access: R/W
	30:29	**Tx Slew Ctl** Access: R/W
	28:27	**Tx Drvsw On** Access: R/W
	26	**Tx Drvsw Ctl** Access: R/W
	25:24	**Comp Spare** Access: R/W
	23	**Procmon clock Sel** Access: R/W
	22:20	**Reserved** Access: RO Format: MBZ
	19:8	**Periodic Comp Counter** Access: R/W Periodic comp programmable counter.

PORT_COMP_DW0

		Value	Name	Description
		05Fh	1.25ms **[Default]**	Period of ~ 1.25ms w.r.t sus clock frequency of 19.2MHz.
	7:0	**Reserved**		
		Access:		RO
		Format:		MBZ

PORT_COMP_DW1

PORT_COMP_DW1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162104h-162107h
Name:	PORT_COMP_DW1
ShortName:	PORT_COMP_DW1_A
Reset:	global
Address:	6C104h-6C107h
Name:	PORT_COMP_DW1
ShortName:	PORT_COMP_DW1_B
Reset:	global
Address:	160104h-160107h
Name:	PORT_COMP_DW1
ShortName:	PORT_COMP_DW1_C
Reset:	global

DWord	Bit	Description
0	31	**ldo_bypass** Default Value: 1b Access: R/W
	30	**fcomp_ovrd_en** Access: R/W
	29	**fcomp_capratio** Access: R/W
	28	**fcomp_bias_sel** Access: R/W
	27:26	**fcomp_inputsel_ovrd** Access: R/W
	25	**fcomp_polaritysel** Access: R/W
	24	**rcomp_en** Default Value: 1b Access: R/W

PORT_COMP_DW1		
	23:22	**p_ref_highval[9:8]** Default Value: 01b Access: R/W
	21:20	**p_ref_lowval[9:8]** Access: R/W
	19:18	**n_ref_highval[9:8]** Default Value: 01b Access: R/W
	17:16	**n_ref_lowval[9:8]** Access: R/W
	15:14	**phvt_ref_highval[9:8]** Access: R/W
	13:12	**phvt_ref_lowval[9:8]** Access: R/W
	11:10	**nhvt_ref_highval[9:8]** Default Value: 01h Access: R/W
	9:8	**nhvt_ref_lowval[9:8]** Access: R/W
	7:6	**plvt_ref_highval[9:8]** Default Value: 01b Access: R/W
	5:4	**plvt_ref_lowval[9:8]** Access: R/W
	3:2	**nlvt_ref_highval[9:8]** Default Value: 01b Access: R/W
	1:0	**nlvt_ref_lowval[9:8]** Access: R/W

PORT_COMP_DW3

PORT_COMP_DW3

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32

Address:	16210Ch-16210Fh
Name:	PORT_COMP_DW3
ShortName:	PORT_COMP_DW3_A
Reset:	global

Address:	6C10Ch-6C10Fh
Name:	PORT_COMP_DW3
ShortName:	PORT_COMP_DW3_B
Reset:	global

Address:	16010Ch-16010Fh
Name:	PORT_COMP_DW3
ShortName:	PORT_COMP_DW3_C
Reset:	global

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:26	**Process Info** Access: RO 000b dot-0 001b dot-1 010b dot-4
	25:24	**Voltage Info** Access: RO 00b 0.85V 01b 0.95V 10b 1.05
	23	**PLL DDI Pwr Ack** Access: RO

PORT_COMP_DW3

	22	**First Comp Done** Access: RO
	21	**Procmon Done** Access: RO
	20	**Icomp Code Maxout** Access: RO
	19	**Icomp Code Minout** Access: RO
	18:15	**Reserved** Access: RO Format: MBZ
	14:8	**Icomp Code** Access: RO
	7	**Lpdn Code Maxout** Access: RO
	6	**Lpdn Code Minout** Access: RO
	5:0	**MIPI Lpdn Code** Access: RO

PORT_COMP_DW8

PORT_COMP_DW8

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	162120h-162123h
Name:	PORT_COMP_DW8
ShortName:	PORT_COMP_DW8_A
Reset:	global

Address:	6C120h-6C123h
Name:	PORT_COMP_DW8
ShortName:	PORT_COMP_DW8_B
Reset:	global

Address:	160120h-160123h
Name:	PORT_COMP_DW8
ShortName:	PORT_COMP_DW8_C
Reset:	global

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24	**irefgen** Access: R/W 1b – Enable 0b – Disable
	23:15	**Reserved** Access: RO Format: MBZ
	14	**prdic_icomp_dis** Access: R/W disable periodic icomp 0b – Enable 1b – Disable

PORT_COMP_DW8		
	13:0	**Reserved** Access: RO Format: MBZ

PORT_COMP_DW9

PORT_COMP_DW9	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162124h-162127h
Name:	PORT_COMP_DW9
ShortName:	PORT_COMP_DW9_A
Reset:	global
Address:	6C124h-6C127h
Name:	PORT_COMP_DW9
ShortName:	PORT_COMP_DW9_B
Reset:	global
Address:	160124h-160127h
Name:	PORT_COMP_DW9
ShortName:	PORT_COMP_DW9_C
Reset:	global

DWord	Bit	Description	
0	31:24	**n_ref_lowval[7:0]**	
		Default Value:	11011010b
		Access:	R/W
	23:16	**n_ref_highval[7:0]**	
		Default Value:	10001100b
		Access:	R/W
	15:8	**p_ref_lowval[7:0]**	
		Default Value:	11011100b
		Access:	R/W
	7:0	**p_ref_highval[7:0]**	
		Default Value:	10100101b
		Access:	R/W

PORT_COMP_DW10

PORT_COMP_DW10		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	162128h-16212Bh	
Name:	PORT_COMP_DW10	
ShortName:	PORT_COMP_DW10_A	
Reset:	global	
Address:	6C128h-6C12Bh	
Name:	PORT_COMP_DW10	
ShortName:	PORT_COMP_DW10_B	
Reset:	global	
Address:	160128h-16012Bh	
Name:	PORT_COMP_DW10	
ShortName:	PORT_COMP_DW10_C	
Reset:	global	

DWord	Bit	Description	
0	31:24	**nlvt_ref_lowval[7:0]**	
		Default Value:	10101010b
		Access:	R/W
	23:16	**nlvt_ref_highval[7:0]**	
		Default Value:	00111101b
		Access:	R/W
	15:8	**plvt_ref_lowval[7:0]**	
		Default Value:	10101000b
		Access:	R/W
	7:0	**plvt_ref_highval[7:0]**	
		Default Value:	01010011b
		Access:	R/W

PORT_PCS_DW1

PORT_PCS_DW1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162304h-162307h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_AUX_A
Reset:	global
Address:	162604h-162607h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_GRP_A
Reset:	global
Address:	162804h-162807h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN0_A
Reset:	global
Address:	162904h-162907h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN1_A
Reset:	global
Address:	162A04h-162A07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN2_A
Reset:	global
Address:	162B04h-162B07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN3_A
Reset:	global
Address:	6C304h-6C307h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_AUX_B
Reset:	global
Address:	6C604h-6C607h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_GRP_B

PORT_PCS_DW1	
Reset:	global
Address:	6C804h-6C807h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN0_B
Reset:	global
Address:	6C904h-6C907h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN1_B
Reset:	global
Address:	6CA04h-6CA07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN2_B
Reset:	global
Address:	6CB04h-6CB07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN3_B
Reset:	global
Address:	160304h-160307h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_AUX_C
Reset:	global
Address:	160604h-160607h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_GRP_C
Reset:	global
Address:	160804h-160807h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN0_C
Reset:	global
Address:	160904h-160907h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN1_C
Reset:	global
Address:	160A04h-160A07h
Name:	PORT_PCS_DW1
ShortName:	PORT_PCS_DW1_LN2_C

PORT_PCS_DW1

Reset: global

Address: 160B04h-160B07h
Name: PORT_PCS_DW1
ShortName: PORT_PCS_DW1_LN3_C
Reset: global

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28	**cmnkeeper_enable_in_pg** Access: R/W 1b: enable **[Default]** 0b: disable
	27	**pg_pwrdownen** Access: R/W PG Power Down Enable 1b: enable **[Default]** 0b: disable
	26	**cmnkeeper_enable** Access: R/W Common Keeper Enable 1b: enable **[Default]** 0b: disable
	25:24	**cmnkeep_biasctr** Access: R/W Common Keeper Bias Control
	23:22	**Reserved** Access: RO Format: MBZ
	21:20	**DCC Mode Select** Access: R/W

PORT_PCS_DW1

Value	Name
00b	Run DCC once **[Default]**
01b	Run DCC every 100us
10b	Run DCC every 1ms
11b	Run DCC continuously

19 **reg_dcc_bypass**

Default Value:	0b
Access:	R/W

Setting this bit will bypass the DCC calibration and will also bypass the DFx RX calibration since both are triggered using same signal in PCS

18 **reg_dcc_calib_wake_en**

Default Value:	0b
Access:	R/W

Asserting this bit will run DCC again during DL wake up from powerdown

17 **tx_dcc_calib_enable**

Default Value:	0b
Access:	R/W

Force Tx DCC Calibration Enable (Should be used only after initial boot is done)

16 **Reserved**

Access:	R/W

15:14 **Reserved**

Access:	RO
Format:	MBZ

13:12 **txhigh**

Access:	R/W

11:10 **Reserved**

Access:	RO
Format:	MBZ

9:8 **clkreq**

Access:	R/W

7 **tbc_as_symbclk**

Access:	R/W

Select tbc clock to be used as symbol clock internal to the data lane

PORT_PCS_DW1

	6	**txfifo_rst_main_ovrden** Access: R/W Override enable for Tx main resets
	5	**txfifo_rst_main_ovrd** Access: R/W Reset Main Override for Tx
	4	**txdeemp** Access: R/W Deemphasis Value
	3:2	**latencyoptim** Default Value: 01b Access: R/W Latency Optim
	1	**softreset_enable** Access: R/W Allow soft_reset_n to reset the lanes Value: 1b — Name: enable Value: 0b — Name: disable
	0	**soft_reset_n** Default Value: 1b Access: R/W Active low soft reset override

PORT_PCS_DW9

PORT_PCS_DW9	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162324h-162327h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_AUX_A
Reset:	global
Address:	162624h-162627h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_GRP_A
Reset:	global
Address:	162824h-162827h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN0_A
Reset:	global
Address:	162924h-162927h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN1_A
Reset:	global
Address:	162A24h-162A27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN2_A
Reset:	global
Address:	162B24h-162B27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN3_A
Reset:	global
Address:	6C324h-6C327h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_AUX_B
Reset:	global
Address:	6C624h-6C627h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_GRP_B

PORT_PCS_DW9	
Reset:	global
Address:	6C824h-6C827h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN0_B
Reset:	global
Address:	6C924h-6C927h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN1_B
Reset:	global
Address:	6CA24h-6CA27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN2_B
Reset:	global
Address:	6CB24h-6CB27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN3_B
Reset:	global
Address:	160324h-160327h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_AUX_C
Reset:	global
Address:	160624h-160627h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_GRP_C
Reset:	global
Address:	160824h-160827h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN0_C
Reset:	global
Address:	160924h-160927h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN1_C
Reset:	global
Address:	160A24h-160A27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN2_C

PORT_PCS_DW9

Reset:	global
Address:	160B24h-160B27h
Name:	PORT_PCS_DW9
ShortName:	PORT_PCS_DW9_LN3_C
Reset:	global

DWord	Bit	Description
0	31:28	**Reserved** Access: RO Format: MBZ
	27:16	**Strong CM Count Ovrd** Default Value: 301h Access: R/W
	15:11	**Reserved** Access: RO Format: MBZ
	10:8	**Stagger Mult** Default Value: 001b Access: R/W
	7:6	**Reserved** Access: RO Format: MBZ
	5	**Stagger Override** Access: R/W
	4:0	**Stagger** Access: R/W

PORT_TX_DFLEXDPCSSS

PORT_TX_DFLEXDPCSSS		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**Displayport Phy Mode Status for Type-C Connector 7** Access: R/W Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 7.
	6	**Displayport Phy Mode Status for Type-C Connector 6** Access: R/W Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 6.
	5	**Displayport Phy Mode Status for Type-C Connector 5** Access: R/W Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 5.
	4	**Displayport Phy Mode Status for Type-C Connector 4** Access: R/W Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 4.
	3	**Displayport Phy Mode Status for Type-C Connector 3** Access: R/W Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 3.
	2	**Displayport Phy Mode Status for Type-C Connector 2** Access: R/W Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 2.
	1	**Displayport Phy Mode Status for Type-C Connector 1** Access: R/W Similar to register DFLEXDPCSSS.DPPMSTC0 but this register is for Type-C Connector 1.

PORT_TX_DFLEXDPCSSS

	0	**Displayport Phy Mode Status for Type-C Connector 0** Access: R/W Displayport Phy Mode Status for Type-C Connector 0 (DPPMSTC0): **Value** / **Name** 1b: DP Controller is not in safe state 0b: DP controller is in safe state

PORT_TX_DFLEXDPMLE1

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Reset:	soft

Display Driver writes to these bits to tell FIA hardware which Main Links of the Display Port are enabled on Type-C Connector 0. FIA hardware uses this information for PHY to Controller signal mapping.
For example, in DP Pin Assignment C, the register DFLEXDPSP1.DPX4TXLATC0 tells Display Driver that all the 4 TX Lanes in PHY can be used. However, Display Driver may choose to use only x1, i.e. for ML0. Then Display Driver will program 0001b to this register. For x2 and x4, Display Driver will program 0011b and 1111b, respectively.
Note that display driver should not use its internal lane reversal feature with Type-C ALT connections.
Display Driver is expected to write to this register when the DDI Interface between DP Controller and FIA is in the Safe Mode, e.g. pllen=pwrreq=lane_enable=0. Display Driver writes to this register and then only it brings up the DP Controller, i.e. to bring the DDI interface out from Safe Mode.
A mode set is required to switch the number of DP lanes.
This register is applicable in both Type-C connector's Alternate mode and also DP connector mode.

DWord	Bit	Description
0	31:28	**Displayport Main Link Enable for Type-C Connector 7** Access: R/W Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 7. 0001b ML0 0011b ML[1:0] 1100b ML[3:2] This setting should not be used with Type-C ALT connections. 1111b ML[3:0]
	27:24	**Displayport Main Link Enable for Type-C Connector 6** Access: R/W Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 6. 0001b ML0 0011b ML[1:0] 1100b ML[3:2] This setting should not be used with Type-C ALT connections. 1111b ML[3:0]
	23:20	**Displayport Main Link Enable for Type-C Connector 5** Access: R/W Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 5.

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1

Value	Name	Description
0001b	ML0	
0011b	ML[1:0]	
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.
1111b	ML[3:0]	

19:16 **Displayport Main Link Enable for Type-C Connector 4**

Access:	R/W

Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 4.

Value	Name	Description
0001b	ML0	
0011b	ML[1:0]	
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.
1111b	ML[3:0]	

15:12 **Displayport Main Link Enable for Type-C Connector 3**

Access:	R/W

Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 3.

Value	Name	Description
0001b	ML0	
0011b	ML[1:0]	
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.
1111b	ML[3:0]	

11:8 **Displayport Main Link Enable for Type-C Connector 2**

Access:	R/W

Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 2.

Value	Name	Description
0001b	ML0	
0011b	ML[1:0]	
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.
1111b	ML[3:0]	

7:4 **Displayport Main Link Enable for Type-C Connector 1**

Access:	R/W

Similar to register DFLEXDPMLE1.DPMLETC0 but this register is for Type-C Connector 1.

Value	Name	Description
0001b	ML0	
0011b	ML[1:0]	
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.
1111b	ML[3:0]	

PORT_TX_DFLEXDPMLE1 - PORT_TX_DFLEXDPMLE1

	3:0	**Displayport Main Link Enable for Type-C Connector 0**

Access:	R/W

Display Port Main Link Enable for Type-C Connector 0 (DPMLETC0):
4 bits correspond to 4 Main Link in DP Controller. Bit [0] is ML0,bit [1] is ML1 and so on.
The Type-C Connector number is logical number. Its not physical lane numbers. Refer to the SOC block diagram for the mapping of Type-C Connector number to the actual physical lane number of the PHY.
Display Driver writes to these bits to tell FIA hardware which Main Links of the Display Port are enabled on Type-C Connector 0. FIA hardware use this information for PHY to Controller signal mapping.
For example, in DP Pin Assignment C, the register DFLEXDPSP1.DPX4TXLATC0 tells Display Driver that all the 4 TX Lane in PHY can be used. However, Display Driver may choose to use only x1, i.e. for ML0. Then Display Driver will program 0001b to this register. For x2 and x4, Display Driver will program 0011b and 1111b, respectively.

Value	Name	Description
0001b	ML0	
0011b	ML[1:0]	
1100b	ML[3:2]	This setting should not be used with Type-C ALT connections.
1111b	ML[3:0]	

PORT_TX_DFLEXDPPMS

PORT_TX_DFLEXDPPMS - PORT_TX_DFLEXDPPMS

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32
Reset: soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Display Port PHY Mode status for Type-C connector 15** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 15.
	14	**Display Port PHY Mode status for Type-C connector 14** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 14.
	13	**Display Port PHY Mode status for Type-C connector 13** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 13.
	12	**Display Port PHY Mode status for Type-C connector 12** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 12.
	11	**Display Port PHY Mode status for Type-C connector 11** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 11.
	10	**Display Port PHY Mode status for Type-C connector 10** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 10.
	9	**Display Port PHY Mode status for Type-C connector 9** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 9.

PORT_TX_DFLEXDPPMS - PORT_TX_DFLEXDPPMS

	8	**Display Port PHY Mode status for Type-C connector 8** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 8.
	7	**Display Port PHY Mode status for Type-C connector 7** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 7.
	6	**Display Port PHY Mode status for Type-C connector 6** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 6.
	5	**Display Port PHY Mode status for Type-C connector 5** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 5.
	4	**Display Port PHY Mode status for Type-C connector 4** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 4.
	3	**Display Port PHY Mode status for Type-C connector 3** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 3.
	2	**Display Port PHY Mode status for Type-C connector 2** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 2.
	1	**Display Port PHY Mode status for Type-C connector 1** Access: R/W Similar to register DFLEXDPPMS.DPPMSTC0 but this register is for Type-C Connector 1.
	0	**Display Port PHY Mode status for Type-C connector 0** Access: R/W DFLEXDPPMS.DPPMSTC0 PD FW writes 1 to this bit to tell DP Driver that PHY is ready. PD FW writes '0' to this bit to tell DP Driver that PHY is not ready.

Value	Name
0b	Not Completed
1b	Completed

PORT_TX_DFLEXDPSP

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32
Reset: soft

Dynamic FlexIO DP Scratch Pad (Type-C)

See the TypeC Programming section for information on how the connector number here maps to the port instance.

DWord	Bit	Description
0	31:29	**TC3 Live State** Access: R/W Value / Name / Description: 000b / No HPD / No HPD connect for TypeC (DP alternate) or TBT 001b / TypeC HPD / HPD connect for TypeC (DP alternate) 010b / TBT HPD / HPD connect for TBT 011b / Invalid / Invalid
	28	**Reserved** Access: RO Format: MBZ
	27:24	**Display Port x4 TX Lane Assignment for Type-C Connector 3** Access: R/W Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 3. Value / Name: 0001b / PHY TX[0] 0010b / PHY TX[1] 0011b / PHY TX[1:0] 0100b / PHY TX[2] 0101b / PHY TX[2] TX[0] 1000b / PHY TX[3] 1100b / PHY TX[3:2] 1111b / PHY TX[3:0]
	23:21	**TC2 Live State** Access: R/W

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP

Value	Name	Description
000b	No HPD	No HPD connect for TypeC (DP alternate) or TBT
001b	TypeC HPD	HPD connect for TypeC (DP alternate)
010b	TBT HPD	HPD connect for TBT
011b	Invalid	Invalid

20 **Reserved**

Access:	RO
Format:	MBZ

19:16 **Display Port x4 TX Lane Assignment for Type-C Connector 2**

Access:	R/W

Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 2.

Value	Name
0001b	PHY TX[0]
0010b	PHY TX[1]
0011b	PHY TX[1:0]
0100b	PHY TX[2]
0101b	PHY TX[2] TX[0]
1000b	PHY TX[3]
1100b	PHY TX[3:2]
1111b	PHY TX[3:0]

15:13 **TC1 Live State**

Access:	R/W

Value	Name	Description
000b	No HPD	No HPD connect for TypeC (DP alternate) or TBT
001b	TypeC HPD	HPD connect for TypeC (DP alternate)
010b	TBT HPD	HPD connect for TBT
011b	Invalid	Invalid

12 **IOM FW version**

Access:	R/W

This field identifies the IOM firmware that is used.

Value	Name
0b	old IOM FW
1b	IOM FW with MFD Gen2 support

11:8 **Display Port x4 TX Lane Assignment for Type-C Connector 1**

Access:	R/W

Same definition as DFLEXDPSP1.DPX4TXLATC0, but this register is for Type-C Connector 1.

PORT_TX_DFLEXDPSP - PORT_TX_DFLEXDPSP

Value	Name
0001b	PHY TX[0]
0010b	PHY TX[1]
0011b	PHY TX[1:0]
0100b	PHY TX[2]
0101b	PHY TX[2] TX[0]
1000b	PHY TX[3]
1100b	PHY TX[3:2]
1111b	PHY TX[3:0]

7:5 **TC0 Live state**

Access:	R/W

Value	Name	Description
000b	No HPD	No HPD connect for TypeC (DP alternate) or TBT
001b	TypeC HPD	HPD connect for TypeC (DP alternate)
010b	TBT HPD	HPD connect for TBT
011b	Invalid	Invalid

4 **Modular FIA (MF)**

Access:	R/W

Description
This bit is set by IOM FW and read by Display Driver. It tells the Display Driver if Modular FIA is used in the SOC. If Modular FIA is used in the SOC, then Display Driver will access the additional instances of FIA based on pre-assigned offset in GTTMADDR space. Each Modular FIA instance houses only 2 Type-C Ports. If Modular FIA is not used in the SOC, then a single monolithic FIA is used to house all the Type-C Ports which has only one IOSF Sideband Port ID.
Modular FIA is always used. IOM FW will program the MF bit in all FIA instances.

Value	Name
0b	Monolithic FIA
1b	Modular FIA

3:0 **Display Port x4 TX Lane Assignment for Type-C Connector 0**

Access:	R/W

DPX4TXLATC0
SOC FW writes to these bits to tell display software the Lane Assignment, which it generates based on the DP Pin Assignment and the Connector Orientation. Display software uses this value to determine the number of lanes that can be enabled, and along with other registers, to

determine the DP mode programming. See the Typec PHY DDI Buffer page for DP mode programming.
The 4 bits correspond to 4 TX, i.e. TX[3:0] Lane in PHY.
Lower 2 bits correspond to the 2 lower TX lane on the PHY of Type-C connector.
Upper 2 bits correspond to the upper 2 TX lane on the PHY of Type-C connector.
For example, in DP Pin Assignment D (Multi function) and Flip case, the x2 TX lane are on the upper TypeC Lane, hence the value written into this register will be 1100b.
Another example, in DP Pin Assignment B (Multi function) Active Gen2 cable and Flip case, the x1 TX lane is on the 1st TX of upper TypeC Lane, hence the value written into this register will be 0100b.

Value	Name
0001b	PHY TX[0]
0010b	PHY TX[1]
0011b	PHY TX[1:0]
0100b	PHY TX[2]
0101b	PHY TX[2] TX[0]
1000b	PHY TX[3]
1100b	PHY TX[3:2]
1111b	PHY TX[3:0]

PORT_TX_DFLEXNPCPMS

PORT_TX_DFLEXNPCPMS - PORT_TX_DFLEXNPCPMS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Reset:	soft

SW writes to these bits to control the Combo Ports mode. This register governs the Phy status tracking handling that could be different for different controllers.

DWord	Bit	Description
0	31:28	**Combo Port 7 Next Phy Combo Port Mode Select (CP7NPCPMS):** Access: R/W Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 7.
	27:24	**Combo Port 6 Next Phy Combo Port Mode Select (CP6NPCPMS):** Access: R/W Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 6.
	23:20	**Combo Port 5 Next Phy Combo Port Mode Select (CP5NPCPMS):** Access: R/W Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 5.
	19:16	**Combo Port 4 Next Phy Combo Port Mode Select (CP4NPCPMS):** Access: R/W Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 4.
	15:12	**Combo Port 3 Next Phy Combo Port Mode Select (CP3NPCPMS):** Access: R/W Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 3.
	11:8	**Combo Port 2 Next Phy Combo Port Mode Select (CP2NPCPMS):** Access: R/W Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 2.
	7:4	**Combo Port 1 Next Phy Combo Port Mode Select (CP1NPCPMS):** Access: R/W Similar to register DFLEXNPCPMS1.CP0NPCPMS but this register is for Combo Port 1.
	3:0	**Combo Port 0 Next Phy Combo Port Mode Select (CP0NPCPMS):** Access: R/W The Combo Port number is logical. Its not physical lane numbers.

PORT_TX_DFLEXNPCPMS - PORT_TX_DFLEXNPCPMS		
		0h: Port Mode is NoOwner_USB3. FIA will keep the Lane in Reset state. PhyMode=USB3 1h: Port Mode is Owner 1 (default owner) 2h: Port Mode is Owner 2 3h: Port Mode is Owner 3 4h: Port Mode is Owner 4 5h: Port Mode is Owner 5 6h-Fh: Reserved Others: Reserved SW mode: SW writes to these bits to control the Combo Ports mode. This register governs the Phy status tracking handling that could be different for different controller. HW mode: These bits have no impact to HW when written. The reset default is dependent on the internal HW mux select bits though its being indicated as soft-straps. The mux selects bits retain their context across Sx and will be reloaded back into this field.

PORT_TX_DFLEXPA2

PORT_TX_DFLEXPA2 - PORT_TX_DFLEXPA2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Reset:	soft

FIA has per Connector register to govern the Pin Assignment of each Type-C Connector. For example, DFLEXPA1.DPPATC0 is used to govern the Pin Assignment of Type-C Connector 0.The Type-C Connector number (e.g. 0 in register DPPATC0) is logical number.

DWord	Bit	Description
0	31:28	**Displayport Pin Assignment for Type-C Connector 15** Access: R/W Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 15.
	27:24	**Displayport Pin Assignment for Type-C Connector 14** Access: R/W Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 14.
	23:20	**Displayport Pin Assignment for Type-C Connector 13** Access: R/W Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 13.
	19:16	**Displayport Pin Assignment for Type-C Connector 12** Access: R/W Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 12.
	15:12	**Displayport Pin Assignment for Type-C Connector 11** Access: R/W Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 11.
	11:8	**Displayport Pin Assignment for Type-C Connector 10** Access: R/W Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 10.
	7:4	**Displayport Pin Assignment for Type-C Connector 9** Access: R/W Similar to register DFLEXPA2.DPPATC8 but this register is for Type-C Connector 9.

PORT_TX_DFLEXPA2 - PORT_TX_DFLEXPA2		
	3:0	**Displayport Pin Assignment for Type-C Connector 8** Access: R/W Display Port Pin Assignment for Type-C Connector 8 (DPPATC8): 0000 : No Pin Assignment (For Non Type-C DP) 0001 : Pin Assignment A 0010 : Pin Assignment B 0011 : Pin Assignment C 0100 : Pin Assignment D 0101 : Pin Assignment E 0110 : Pin Assignment F 0111-1111 : Reserved

PORT_TX_DW0

PORT_TX_DW0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162380h-162383h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_AUX_A
Reset:	global
Address:	162680h-162683h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_GRP_A
Reset:	global
Address:	162880h-162883h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN0_A
Reset:	global
Address:	162980h-162983h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN1_A
Reset:	global
Address:	162A80h-162A83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN2_A
Reset:	global
Address:	162B80h-162B83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN3_A
Reset:	global
Address:	6C380h-6C383h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_AUX_B
Reset:	global
Address:	6C680h-6C683h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_GRP_B

PORT_TX_DW0	
Reset:	global
Address:	6C880h-6C883h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN0_B
Reset:	global
Address:	6C980h-6C983h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN1_B
Reset:	global
Address:	6CA80h-6CA83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN2_B
Reset:	global
Address:	6CB80h-6CB83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN3_B
Reset:	global
Address:	160380h-160383h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_AUX_C
Reset:	global
Address:	160680h-160683h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_GRP_C
Reset:	global
Address:	160880h-160883h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN0_C
Reset:	global
Address:	160980h-160983h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN1_C
Reset:	global
Address:	160A80h-160A83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN2_C

PORT_TX_DW0

Reset:	global

Address:	160B80h-160B83h
Name:	PORT_TX_DW0
ShortName:	PORT_TX_DW0_LN3_C
Reset:	global

This register controls Tx Equalization within the Combo-PHY's AFE.

Restriction : Do not change the default Cursor Coefficient values within this register since that will change the equalization being applied by the PHY

DWord	Bit	Description
0	31	**MIPI EQ Select** Access: R/W This bit controls the Tx Equalization level of the PHY This bit is equivalent to the **TxEqLevelHS** PPI pin, but it is only used by the PHY when both the MIPI EQ Override Enable and MIPI EQ Enable bits are set. 0b – Low Level Equalization (3.5 dB) 1b – High Level Equalization (7 dB)
	30	**MIPI EQ Enable** Access: R/W This bit represents the Tx Equalization active state (i.e., enable) This bit is equivalent to the **TxEqActiveHS** PPI pin, but it is only used by the PHY when the MIPI EQ Override Enable is set 0b – Tx Equalization Disabled 1b – Tx Equalization Enabled
	29:24	**Post Cursor Coeff 0** Default Value: bh Default post cursor coeff Access: R/W Restriction : Do not change the default value
	23	**MIPI EQ Override Enable** Access: R/W This bit controls whether the PPI Tx Equalization pins are driving the equalization logic, or the override bits from this register 0b – PPI inputs drive EQ logic 1b – This register drives EQ logic

<table>
<tr><th colspan="3">PORT_TX_DW0</th></tr>
<tr><td></td><td>22:6</td><td>Reserved<table><tr><td>Access:</td><td>RO</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table></td></tr>
<tr><td></td><td>5:0</td><td>Cursor Coeff 0<table><tr><td>Default Value:</td><td>34h Default cursor coeff</td></tr><tr><td>Access:</td><td>R/W</td></tr></table>Restriction: Do not change the default value</td></tr>
</table>

PORT_TX_DW1

PORT_TX_DW1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162384h-162387h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_AUX_A
Reset:	global
Address:	162684h-162687h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_GRP_A
Reset:	global
Address:	162884h-162887h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN0_A
Reset:	global
Address:	162984h-162987h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN1_A
Reset:	global
Address:	162A84h-162A87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN2_A
Reset:	global
Address:	162B84h-162B87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN3_A
Reset:	global
Address:	6C384h-6C387h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_AUX_B
Reset:	global
Address:	6C684h-6C687h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_GRP_B

PORT_TX_DW1	
Reset:	global
Address:	6C884h-6C887h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN0_B
Reset:	global
Address:	6C984h-6C987h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN1_B
Reset:	global
Address:	6CA84h-6CA87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN2_B
Reset:	global
Address:	6CB84h-6CB87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN3_B
Reset:	global
Address:	160384h-160387h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_AUX_C
Reset:	global
Address:	160684h-160687h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_GRP_C
Reset:	global
Address:	160884h-160887h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN0_C
Reset:	global
Address:	160984h-160987h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN1_C
Reset:	global
Address:	160A84h-160A87h
Name:	PORT_TX_DW1
ShortName:	PORT_TX_DW1_LN2_C

PORT_TX_DW1

Reset: global

Address: 160B84h-160B87h
Name: PORT_TX_DW1
ShortName: PORT_TX_DW1_LN3_C
Reset: global

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**o_iref_config** Access: R/W ICOMP Config bit from COMP routed to Txana
	6:5	**o_iref_ctrl** Access: R/W control to change the ratio of tx iboost
	4:3	**o_tx_slew_ctrl** Access: R/W Used for MIPI HSTX Slew rate control config
	2	**o_vref_low_en** Access: R/W LDO Feedback path enable for low vref
	1	**o_vref_hi_en** Access: R/W LDO Feedback path enable for hi vref
	0	**o_vref_nom_en** Access: R/W LDO Feedback path enable for nominal vref

PORT_TX_DW2

PORT_TX_DW2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162388h-16238Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_AUX_A
Reset:	global
Address:	162688h-16268Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_GRP_A
Reset:	global
Address:	162888h-16288Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN0_A
Reset:	global
Address:	162988h-16298Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN1_A
Reset:	global
Address:	162A88h-162A8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN2_A
Reset:	global
Address:	162B88h-162B8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN3_A
Reset:	global
Address:	6C388h-6C38Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_AUX_B
Reset:	global
Address:	6C688h-6C68Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_GRP_B

PORT_TX_DW2	
Reset:	global
Address:	6C888h-6C88Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN0_B
Reset:	global
Address:	6C988h-6C98Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN1_B
Reset:	global
Address:	6CA88h-6CA8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN2_B
Reset:	global
Address:	6CB88h-6CB8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN3_B
Reset:	global
Address:	160388h-16038Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_AUX_C
Reset:	global
Address:	160688h-16068Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_GRP_C
Reset:	global
Address:	160888h-16088Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN0_C
Reset:	global
Address:	160988h-16098Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN1_C
Reset:	global
Address:	160A88h-160A8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN2_C

PORT_TX_DW2

Reset:	global

Address:	160B88h-160B8Bh
Name:	PORT_TX_DW2
ShortName:	PORT_TX_DW2_LN3_C
Reset:	global

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**swing_sel upper** Access: R/W Swing_sel bit 3
	14	**cmnmode_sel** Access: R/W Select one of the weak common modes.
	13:11	**swing_sel lower** Default Value: 010b Access: R/W Select the voltage swing level. Note that this field has swing_sel bits 2:0 and bit 3 is in swing_sel upper, which is not adjacent.
	10:8	**frclatencyoptim** Access: R/W Enables forcing the latency optimized value for the FIFO.
	7:0	**Rcomp scalar** Default Value: 10011000b Access: R/W Also called Swing Scalar. Scalar to be applied to comp code to get required termination.

PORT_TX_DW4

PORT_TX_DW4	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162390h-162393h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_AUX_A
Reset:	global
Address:	162690h-162693h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_GRP_A
Reset:	global
Address:	162890h-162893h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN0_A
Reset:	global
Address:	162990h-162993h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN1_A
Reset:	global
Address:	162A90h-162A93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN2_A
Reset:	global
Address:	162B90h-162B93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN3_A
Reset:	global
Address:	6C390h-6C393h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_AUX_B
Reset:	global
Address:	6C690h-6C693h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_GRP_B

PORT_TX_DW4	
Reset:	global
Address:	6C890h-6C893h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN0_B
Reset:	global
Address:	6C990h-6C993h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN1_B
Reset:	global
Address:	6CA90h-6CA93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN2_B
Reset:	global
Address:	6CB90h-6CB93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN3_B
Reset:	global
Address:	160390h-160393h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_AUX_C
Reset:	global
Address:	160690h-160693h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_GRP_C
Reset:	global
Address:	160890h-160893h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN0_C
Reset:	global
Address:	160990h-160993h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN1_C
Reset:	global
Address:	160A90h-160A93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN2_C

PORT_TX_DW4

Reset:	global
Address:	160B90h-160B93h
Name:	PORT_TX_DW4
ShortName:	PORT_TX_DW4_LN3_C
Reset:	global

DWord	Bit	Description
0	31	**Loadgen Select** Access: R/W
	30:24	**Spare** Access: R/W
	23	**BS Comp Ovrd** Access: R/W
	22:18	**Rterm Limit** Default Value: 10000b Access: R/W
	17:12	**Post Cursor 1** Access: R/W o_txscaling_coeff[17:12]
	11:6	**Post Cursor 2** Access: R/W o_txscaling_coeff[11:6]
	5:0	**Cursor Coeff** Default Value: 011000b Access: R/W o_txscaling_coeff[5:0]

PORT_TX_DW5

PORT_TX_DW5	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162394h-162397h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_AUX_A
Reset:	global
Address:	162694h-162697h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_GRP_A
Reset:	global
Address:	162894h-162897h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN0_A
Reset:	global
Address:	162994h-162997h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN1_A
Reset:	global
Address:	162A94h-162A97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN2_A
Reset:	global
Address:	162B94h-162B97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN3_A
Reset:	global
Address:	6C394h-6C397h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_AUX_B
Reset:	global
Address:	6C694h-6C697h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_GRP_B

PORT_TX_DW5	
Reset:	global
Address:	6C894h-6C897h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN0_B
Reset:	global
Address:	6C994h-6C997h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN1_B
Reset:	global
Address:	6CA94h-6CA97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN2_B
Reset:	global
Address:	6CB94h-6CB97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN3_B
Reset:	global
Address:	160394h-160397h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_AUX_C
Reset:	global
Address:	160694h-160697h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_GRP_C
Reset:	global
Address:	160894h-160897h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN0_C
Reset:	global
Address:	160994h-160997h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN1_C
Reset:	global
Address:	160A94h-160A97h
Name:	PORT_TX_DW5
ShortName:	PORT_TX_DW5_LN2_C

PORT_TX_DW5

Reset: global

Address: 160B94h-160B97h
Name: PORT_TX_DW5
ShortName: PORT_TX_DW5_LN3_C
Reset: global

DWord	Bit	Description
0	31	**TX Training Enable** Access: R/W Value: 1b — enable; 0b — disable
	30	**Disable 2tap** Access: R/W ospare2[5] Value: 0b — Enable; 1b — Disable
	29	**Disable 3tap** Access: R/W ospare2[5] Value: 0b — Enable; 1b — Disable
	28:27	**Spare 28 27** Access: R/W ospare2[4:3]
	26	**Cursor Program** Access: R/W ospare2[2] Value: 0b — Enable; 1b — Disable
	25	**Coeff Polarity** Access: R/W ospare2[1]

PORT_TX_DW5

		Value / **Name** 0b — Enable 1b — Disable
	24	**Spare 24** Access: R/W ospare2[0]
	23:21	**Reserved** Access: RO Format: MBZ
	20:18	**Scaling Mode Sel** Default Value: 010b Access: R/W
	17:16	**Decode Timer Sel** Default Value: 01b Access: R/W
	15:11	**CR Scaling Coef** Access: R/W
	10:6	**Spare 10 6** Access: R/W o_tx_vswing[10:6]
	5:3	**Rterm Select** Access: R/W o_tx_vswing[5:3]
	2:0	**Spare 2 0** Access: R/W o_tx_vswing[2:0]

PORT_TX_DW6

PORT_TX_DW6 - PORT_TX_DW6	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	162398h-16239Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_AUX_A
Reset:	global
Address:	162698h-16269Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_GRP_A
Reset:	global
Address:	162898h-16289Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN0_A
Reset:	global
Address:	162998h-16299Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN1_A
Reset:	global
Address:	162A98h-162A9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN2_A
Reset:	global
Address:	162B98h-162B9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN3_A
Reset:	global
Address:	6C398h-6C39Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_AUX_B
Reset:	global
Address:	6C698h-6C69Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_GRP_B

PORT_TX_DW6 - PORT_TX_DW6	
Reset:	global
Address:	6C898h-6C89Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN0_B
Reset:	global
Address:	6C998h-6C99Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN1_B
Reset:	global
Address:	6CA98h-6CA9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN2_B
Reset:	global
Address:	6CB98h-6CB9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN3_B
Reset:	global
Address:	160398h-16039Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_AUX_C
Reset:	global
Address:	160698h-16069Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_GRP_C
Reset:	global
Address:	160898h-16089Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN0_C
Reset:	global
Address:	160998h-16099Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN1_C
Reset:	global
Address:	160A98h-160A9Bh
Name:	PORT_TX_DW6
ShortName:	PORT_TX_DW6_LN2_C

PORT_TX_DW6 - PORT_TX_DW6

Reset: global

Address: 160B98h-160B9Bh
Name: PORT_TX_DW6
ShortName: PORT_TX_DW6_LN3_C
Reset: global

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**o_func_ovrd_en** Access: R/W ovrd enable signal
	6:1	**o_ldo_ref_sel_cri** Access: R/W ovrd for ldo_ref_sel
	0	**o_ldo_bypass_cri** Access: R/W ovrd for ldo bypass

PORT_TX_DW7

PORT_TX_DW7	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	16239Ch-16239Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_AUX_A
Reset:	global
Address:	16269Ch-16269Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_GRP_A
Reset:	global
Address:	16289Ch-16289Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN0_A
Reset:	global
Address:	16299Ch-16299Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN1_A
Reset:	global
Address:	162A9Ch-162A9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN2_A
Reset:	global
Address:	162B9Ch-162B9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN3_A
Reset:	global
Address:	6C39Ch-6C39Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_AUX_B
Reset:	global
Address:	6C69Ch-6C69Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_GRP_B

PORT_TX_DW7	
Reset:	global
Address:	6C89Ch-6C89Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN0_B
Reset:	global
Address:	6C99Ch-6C99Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN1_B
Reset:	global
Address:	6CA9Ch-6CA9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN2_B
Reset:	global
Address:	6CB9Ch-6CB9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN3_B
Reset:	global
Address:	16039Ch-16039Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_AUX_C
Reset:	global
Address:	16069Ch-16069Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_GRP_C
Reset:	global
Address:	16089Ch-16089Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN0_C
Reset:	global
Address:	16099Ch-16099Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN1_C
Reset:	global
Address:	160A9Ch-160A9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN2_C

PORT_TX_DW7

Reset:	global
Address:	160B9Ch-160B9Fh
Name:	PORT_TX_DW7
ShortName:	PORT_TX_DW7_LN3_C
Reset:	global

DWord	Bit	Description
0	31	**Spare 31** Access: R/W
	30:24	**N Scalar** Default Value: 7Fh Access: R/W
	23:0	**Spare 23 0** Access: R/W

PORT_TX_DW8

PORT_TX_DW8	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1623A0h-1623A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_AUX_A
Reset:	global
Address:	1626A0h-1626A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_GRP_A
Reset:	global
Address:	1628A0h-1628A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN0_A
Reset:	global
Address:	1629A0h-1629A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN1_A
Reset:	global
Address:	162AA0h-162AA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN2_A
Reset:	global
Address:	162BA0h-162BA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN3_A
Reset:	global
Address:	6C3A0h-6C3A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_AUX_B
Reset:	global
Address:	6C6A0h-6C6A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_GRP_B

PORT_TX_DW8	
Reset:	global
Address:	6C8A0h-6C8A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN0_B
Reset:	global
Address:	6C9A0h-6C9A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN1_B
Reset:	global
Address:	6CAA0h-6CAA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN2_B
Reset:	global
Address:	6CBA0h-6CBA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN3_B
Reset:	global
Address:	1603A0h-1603A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_AUX_C
Reset:	global
Address:	1606A0h-1606A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_GRP_C
Reset:	global
Address:	1608A0h-1608A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN0_C
Reset:	global
Address:	1609A0h-1609A3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN1_C
Reset:	global
Address:	160AA0h-160AA3h
Name:	PORT_TX_DW8
ShortName:	PORT_TX_DW8_LN2_C

PORT_TX_DW8

Reset: global

Address: 160BA0h-160BA3h
Name: PORT_TX_DW8
ShortName: PORT_TX_DW8_LN3_C
Reset: global

DWord	Bit	Description
0	31	**odcc_clksel** Default Value: 0b Access: R/W DCC clock select
	30:29	**odcc_clk_div_sel** Access: R/W Value / Name: 00b,01b: div2 10b: div4 **[Default]** 11b: div8
	28:24	**odcc_code_ovrd** Default Value: 10000b Access: R/W
	23	**odcc_code_ovrd_en** Access: R/W
	22	**odccfuse_en** Access: R/W
	21	**Reserved** Access: R/W
	20:16	**odcc_lower_limit** Default Value: 00011b Access: R/W
	15	**Reserved** Access: R/W
	14:13	**idcc_code_therm_4_3** Default Value: 10b Access: R/W

PORT_TX_DW8		
	12:8	**idcc_code** Default Value: 10000b Access: R/W
	7:5	**idcc_code_therm_2_0** Access: R/W
	4:0	**odcc_upper_limit** Default Value: 11100b Access: R/W

POST_CSC_CC2_DATA

POST_CSC_CC2_DATA

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A50Ch-4A50Fh
Name:	Pipe Post CSC CC2 Data
ShortName:	POST_CSC_CC2_DATA_A
Reset:	soft
Address:	4AD0Ch-4AD0Fh
Name:	Pipe Post CSC CC2 Data
ShortName:	POST_CSC_CC2_DATA_B
Reset:	soft

These are the precision palette entries used for the 10 bpc and 12 bpc gamma. The Precision Palette Index Value indicates the precision palette location to be accessed through this register.

Programming Notes

For 10 bpc, program with the color 10 bit palette entry fraction value. For 12 bpc gamma odd indexes, program with the upper 10 bits of the color palette entry fraction value. For 12 bpc gamma even indexes, program the MSbs with the lower 6 bits of the color palette entry fraction value, then program all 0s in the LSbs.

For 12 bit Logarithmic Gamma Mode, the first 510 gamma entries are stored in the precision palette with 16 bits per color in a 0.16 format with 0 integer and 16 fractional bits (upper 10 bits in odd indexes, lower 6 bits in even indexes)

Restriction

This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:20	**Red Precision Palette Entry** Default Value: UUUUUUUUUUb Access: R/W Red precision palette entry value.
	19:10	**Green Precision Palette Entry** Default Value: UUUUUUUUUUb Access: R/W Green precision palette entry value.

POST_CSC_CC2_DATA		
	9:0	**Blue Precision Palette Entry** Default Value: UUUUUUUUUUb Access: R/W Blue precision palette entry value.

POST_CSC_CC2_INDEX

POST_CSC_CC2_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A508h-4A50Bh
Name:	Pipe Post CSC CC2 Index
ShortName:	POST_CSC_CC2_INDEX_A
Reset:	soft
Address:	4AD08h-4AD0Bh
Name:	Pipe Post CSC CC2 Index
ShortName:	POST_CSC_CC2_INDEX_B
Reset:	soft

This index controls access to the array of CSC CC2 data values.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**Index Auto Increment** Access: R/W This field enables the index auto increment. Value / Name / Description: 0b / No Increment / Do not automatically increment the index value. 1b / Auto Increment / Increment the index value with each read or write to the data register.
	14:10	**Reserved** Access: RO Format: MBZ
	9:0	**Index Value** Access: R/W This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. Value / Name: [0,1023] /

Power Clock State Register

PWR_CLK_STATE - Power Clock State Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	020C8h-020CBh
Name:	PWR_CLK_STATE
ShortName:	PWR_CLK_STATE_RCSUNIT_BE_COMPUTE
Address:	1A0C8h-1A0CBh
Name:	PWR_CLK_STATE
ShortName:	PWR_CLK_STATE_CCSUNIT_BE_COMPUTE0
Address:	1C0C8h-1C0CBh
Name:	PWR_CLK_STATE
ShortName:	PWR_CLK_STATE_CCSUNIT_BE_COMPUTE1
Address:	1E0C8h-1E0CBh
Name:	PWR_CLK_STATE
ShortName:	PWR_CLK_STATE_CCSUNIT_BE_COMPUTE2
Address:	260C8h-260CBh
Name:	PWR_CLK_STATE
ShortName:	PWR_CLK_STATE_CCSUNIT_BE_COMPUTE3

This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.

Programming Notes
This register is only functional for RenderCS. This register must not be exercised in VideoCS, BlitterCS and VideoEnhancementCS.
This register must not be programmed directly through CPU MMIO cycle. **Exec-List Scheduling Mode:** Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer.

DWord	Bit	Description
0	31:0	**Reserved** Access: R/W Format: PBC

Power Down Delay

POWER_DOWN_DELAY - Power Down Delay		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	0A040h	
DWord	**Bit**	**Description**
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Delay** Default Value: 0 Access: R/W Lock _Custom_GTIReset: BUS Number of cuclk to wait after GPM has received Block ack from MGSR and before GPM does Message Channel Flush. Default: 0000h (0 clk) Applies to GT C6 entry, Render Power down & Media Power Down. Notes: MGSR can send posted cycle into GT. To make sure cycle reaches the streamers and BUSY message reaches to GPM , this register can be programmed to add delay to GT/Render/Media Power down flows. Lock bit for this register is in : A180[31]

Power Management Capabilities

PMCAP_0_2_0_PCI - Power Management Capabilities

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	000D2h

This register provides information on the capabilities of the function related to power management.

DWord	Bit	Description
0	15:11	**PME Support** Default Value: 00000b Access: RO _Custom_GTIReset: BUS This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
	10	**D2 Support** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 to indicate the D2 power management state is not supported.
	9	**D1 Support** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 to indicate that the D1 power management state is not supported.
	8:6	**Reserved** Access: RO Format: MBZ
	5	**Device Specific Initialization** Default Value: 1b Access: RO _Custom_GTIReset: BUS Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.

PMCAP_0_2_0_PCI - Power Management Capabilities

4 — Reserved

Access:	RO
Format:	MBZ

3 — PME Clock

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 0 to indicate IGD does not support PME# generation.

2:0 — Version

Access:	RO
_Custom_GTIReset:	BUS

Description
Hardwired to 011b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.2 of the PCI Power Management Interface Specification.

Value	Name
011b	**[Default]**

Power Management Capabilities ID

PMCAPID_0_2_0_PCI - Power Management Capabilities ID

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	000D0h

This register contains the PCI Power Management Capability ID and the next capability pointer.

DWord	Bit	Description
0	15:8	**Next Capability Pointer** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list.
	7:0	**Capability Identifier** Default Value: 00000001b Access: RO _Custom_GTIReset: BUS Hardwired to 01h for power management.

Power Management Control and Status

PMCS_0_2_0_PCI - Power Management Control and Status

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	000D4h

DWord	Bit	Description
0	15	**PME Status** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit is hardwired to 0 to indicate that IGD does not support PME# generation from D3 (cold).
	14:13	**Data Scale** Default Value: 00b Access: RO _Custom_GTIReset: BUS This field is hardwired to 00 to indicate IGD does not support data register.
	12:9	**Data Select** Default Value: 0000b Access: RO _Custom_GTIReset: BUS This field is hardwired to 0h to indicate IGD does not support data register.
	8	**PME Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit is hardwired to 0 to indicate that PME# assertion from D3 (cold) is disabled.
	7:4	**Reserved** Access: RO Format: MBZ
	3	**No Soft Reset** Default Value: 1 Access: RO When set (1), this bit indicates that devices transitioning from D3hot to D0 because of

PMCS_0_2_0_PCI - Power Management Control and Status

		PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
	2	**Reserved** Access: RO Format: MBZ
	1:0	**Power State** Default Value: 00b Access: R/W Variant _Custom_GTIReset: BUS This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec. Bits[1:0]Power state00:D0Default01:D1Not Supported10:D2Not Supported11:D3

PP_CONTROL

PP_CONTROL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	C7204h-C7207h
Name:	Panel Power Control
ShortName:	PP_CONTROL
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: R/W
	15:9	**Reserved** Access: RO Format: MBZ
	8:4	**Power Cycle Delay** Access: R/W This field provides the delay for the eDP T12 time; the shortest time from panel power disable to power enable. If panel power power state target is set to on during this delay, the power on sequence will not commence until the delay is complete. The value should be programmed to (desired delay / 100 milliseconds) + 1. Writing a value of 0 selects no delay or is used to abort the delay if it is active. Value: 00000b — Name: No delay Value: 00101b — Name: 400 mS Restriction: A correct value must be programmed before enabling panel power.
	3	**VDD Override** Access: R/W This bit is used to force on VDD for the embedded DisplayPort panel so AUX transactions can occur without enabling the panel power sequence. This is intended for panels that require VDD to be asserted before accessing AUX port on the receiver. Value: 0b — Name: Not Force Value: 1b — Name: Force Restriction: When software clears this bit from '1' to '0' (disable VDD override) it must ensure that T4 power

PP_CONTROL

		cycle delay is met before setting this bit to '1' again.
	2	**Backlight Enable** Access: R/W This field enables the backlight when hardware is in the correct panel power sequence state. **Value** / **Name** 0b – Disable 1b – Enable
	1	**Power Down on Reset** Access: R/W This field selects whether the panel will run the power down sequence when a reset is detected **Value** / **Name** 0b – Do not run power down on reset 1b – Run power down on reset **Programming Notes** Setting power down on reset is recommended for panel protection.
	0	**Power State Target** Access: R/W This field sets the panel power state target. It can be written at any time and takes effect at the completion of any current power cycle. **Value** / **Name** / **Description** 0b / Off / If panel power is currently on, the power off sequence starts immediately. If a power on sequence is currently in progress, the power off sequence starts after the power on state is reached, which may include a power cycle delay. 1b / On / If panel power is currently off, the power on sequence starts immediately. If a power off sequence is currently in progress, the power on sequence starts after the power off state is reached and the power cycle delay is met. **Restriction** A correct Power Cycle Delay value must be programmed before enabling panel power.

PP_OFF_DELAYS

PP_OFF_DELAYS	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	C720Ch-C720Fh
Name:	Panel Power Off Sequencing Delays
ShortName:	PP_OFF_DELAYS
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Power Down delay** Access: R/W This fields provides the delay during power down. Software programs this field with the time delay for the eDP T10 time value; the time from source ending valid video data to source disabling panel power. Software controls the source valid video data output. The time unit is 100us.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Backlight Off to Power Down** Access: R/W This field provides the backlight off to power down delay. Software programs this field with the time delay for the eDP T9 time value; the time from backlight disable to source ending valid video data. Software controls the backlight disable and source valid video data output. The time unit is 100us.

PP_ON_DELAYS

PP_ON_DELAYS		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	C7208h-C720Bh	
Name:	Panel Power On Sequencing Delays	
ShortName:	PP_ON_DELAYS	
Reset:	soft	

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Power Up Delay** Access: R/W This field provides the delay during panel power up. Software programs this field with the delay for eDP T3; the time from enabling panel power to when the sink HPD and AUX channel should be ready. Software controls when AUX channel transactions start. The time unit is 100us.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Power On to Backlight On** Access: R/W This field provides the power on to backlight enable delay. Software controls the source valid video data output and can enable backlight after this delay has been met. Hardware will not allow the backlight to enable until after the power up delay (eDP T3) and this delay have passed. The time unit is 100us.

PP_STATUS

PP_STATUS

Register Space: MMIO: 0/2/0
Access: RO
Size (in bits): 32

Address: C7200h-C7203h
Name: Panel Power Status
ShortName: PP_STATUS
Reset: soft

DWord	Bit	Description
0	31	**Panel Power On Status** Access: RO Value / Name / Description: 0b / Off / Panel power down has completed. A power cycle delay may be currently active. 1b / On / Panel is currently powered up or is currently in the power down sequence. **Programming Notes** Software is responsible for enabling the embedded panel display only at the correct point as defined in the mode set sequence.
	30	**Reserved** Access: RO Format: MBZ
	29:28	**Power Sequence Progress** Access: RO Value / Name / Description: 00b / None / Panel is not in a power sequence 01b / Power Up / Panel is in a power up sequence (may include power cycle delay) 10b / Power Down / Panel is in a power down sequence 11b / Reserved / Reserved
	27	**Power Cycle Delay Active** Access: RO Power cycle delays occur after a panel power down sequence or after a hardware reset. Value / Name: 0b / Not Active **[Default]** 1b / Active

PP_STATUS		
	26:4	**Reserved** Access: RO Format: MBZ
	3:0	**Reserved** Access: RO

PPPR

PPPR - PPPR	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	124824h

GT uses this register to post pending page requests to software, such as x86 page faults.
A write to this register triggers an MSI per the registers PRESTS, PRECTL, PREDATA, PREADR, and PREUADR.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**POST PENDING PAGE REQUEST** Default Value: 0h Access: WO _Custom_GTIReset: BUS Post Pending Page Request

PPRO

PPRO - PPRO		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	124820h	
GT uses this register to post Page Request Queue overflow faults		
DWord	**Bit**	**Description**
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**POST PAGE REQUEST OVERFLOW FAULT** Default Value: 0h Access: WO _Custom_GTIReset: BUS Post Page Request overflow fault

PRE_CSC_CC2_GAMC_DATA

PRE_CSC_CC2_GAMC_DATA

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A504h-4A507h
Name:	Pipe Pre CSC CC2 Gamma Data
ShortName:	PRE_CSC_CC2_GAMC_DATA_A
Reset:	soft
Address:	4AD04h-4AD07h
Name:	Pipe Pre CSC CC2 Gamma Data
ShortName:	PRE_CSC_CC2_GAMC_DATA_B
Reset:	soft

Description

PRE_CSC_CC2_GAMC_INDEX and PRE_CSC_CC2_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the pipe pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion, if needed.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the 129 gamma entries to create the result value. The first 128 entries are stored as 12 bits per color in an unsigned 0.12 format with 0 integer and 12 fractional. The 129th entry is stored as 13 bits per color in a signed 1.12 format with 1 integer and 12 fractional bits.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.
Pre CSC CC2 Gamma correction gets enabled or disabled based on the "Pipe Pre CSC CC2 Gamma Enable" bit in the GAMMA_MODE register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 1.0. For inputs of 0 to 1.0, multiply the input value by 128 to find the gamma entry number, then store the desired gamma result in that entry.
Recommended sRGB degamma programming:

Index	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Values	0	3	6	8	B	D	10	13	16	1A	1E	21	25	2A	2F	35	3B	41	48	4F	56	5E	66	6F	78	82	8C	96	A1	AC	B8	C4

PRE_CSC_CC2_GAMC_DATA

Index	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
Values	D0	DD	EB	F9	107	116	126	136	146	157	168	17A	18C	19F	1B3	1C7	1DB	1F0	206	21C	232	249	261	279	292	2AB	2C5	2E0	2FB	316	333	34F

Index	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
Values	36D	38B	3A9	3C8	3E8	408	429	44B	46D	48F	4B3	4D7	4FB	520	546	56C	593	5BB	5E3	60C	636	660	68B	6B7	6E3	710	73D	76B	79A	7CA	7FA	82B

Index	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112>	113>	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
Values	85C	88E	8C1	8F5	929	95E	994	9CA	A01	A39	A71	AAA	AE4	B1E	B5A	B96	BD2	C10	C4E	C8D	CCC	D0C	D4D	D8F	DD2	E15	E59	E8D	ED3	F19	F60	FA8	1000

Restriction

Restriction : The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO Format: MBZ
	24:13	**Reserved** Access: RO Format: MBZ
	12:0	**Gamma Value** Default Value: 0000000000000b Access: R/W Format: U1.12

PRE_CSC_CC2_GAMC_INDEX

PRE_CSC_CC2_GAMC_INDEX

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	4A500h-4A503h
Name:	Pipe Pre CSC CC2 Gamma Index
ShortName:	PRE_CSC_CC2_GAMC_INDEX_A
Reset:	soft
Address:	4AD00h-4AD03h
Name:	Pipe Pre CSC CC2 Gamma Index
ShortName:	PRE_CSC_CC2_GAMC_INDEX_B
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:8	**Reserved** Access: RO Format: MBZ
	7:0	**Index Value** Access: Write/Read Status This index controls access to the array of pipe pre color space conversion CC2 gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. Value: [0,128]

PRE_CSC_GAMC_DATA

PRE_CSC_GAMC_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A488h-4A48Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_A
Reset:	soft
Address:	4AC88h-4AC8Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_B
Reset:	soft
Address:	4B488h-4B48Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_C
Reset:	soft
Address:	4BC88h-4BC8Bh
Name:	Pipe Pre CSC Gamma Data
ShortName:	PRE_CSC_GAMC_DATA_D
Reset:	soft

Description

PRE_CSC_GAMC_INDEX and PRE_CSC_GAMC_DATA registers are used to program the values that determine the characteristics of the gamma correction for the pipe pixel data before Color Space Conversion. Additional gamma correction can be done after the Color Space Conversion Gamma if desired.
The gamma correction curve is represented by specifying a set of gamma entry reference points spaced equally along the curve for values between -1 and 1. For extended values there are extended gamma entry reference points. All input values are clamped to the greater than -7.0 and less than 7.0 range before the gamma calculation.
For input values greater than or equal to 0 and less than 1.0, the input value is used to linearly interpolate between two adjacent points of the first 129 gamma entries to create the result value. The first 128 entries are stored as 16 bits per color in an unsigned 0.16 format with 0 integer and 16 fractional. The 129th, 130thand 131thentries are stored as 19 bits per color in an unsigned 3.16 format with 3 integer and 16 fractional bits.
For input values greater than or equal to 1.0 and less than 3.0, the input value is used to linearly interpolate between the 129th and 130thgamma entries to create the result value.
For input values greater than or equal to 3.0 and less than 7.0, the input value is used to linearly interpolate between the 130thand 131stgamma entries to create the result value.
For negative input values, gamma is mirrored along the X-axis, giving the same result as positive input values, except for a negative sign. When gamma input may be negative, the first gamma point should be programmed to a value of 0.0 in order to have a symmetric mirroring.

PRE_CSC_GAMC_DATA

Pre-CSC Gamma correction gets enabled or disabled based on the "Pipe CSC Enable" bit in the PLANE_COLOR_CTL register. The same set of values is used for gamma correction of the red, blue and green channels.
See Pipe Gamma for an example gamma curve diagram.

Programming Notes

To program the gamma correction entries, calculate the desired gamma curve for inputs from 0 to 7.0. For inputs of 0 to 1.0, multiply the input value by 128 to find the gamma entry number, then store the desired gamma result in that entry. For inputs greater than 1.0 and less than or equal to 3.0, store the result for an input of 3.0 in the 129th gamma entry. For inputs greater than 3.0 and less than or equal to 7.0, store the result for an input of 7.0 in the 130th gamma entry.

Restriction

The gamma curve must be flat or increasing, never decreasing. The gamma correction registers should only be updated when the plane is off, otherwise screen artifacts may show temporarily.

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ
	26:19	**Reserved** Access: RO Format: MBZ
	18:0	**Gamma Value** Default Value: 0000000000000000000b Access: R/W Format: U3.16

PRE_CSC_GAMC_INDEX

PRE_CSC_GAMC_INDEX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4A484h-4A487h
Name:	Pipe Pre CSC Gamma Index
ShortName:	PRE_CSC_GAMC_INDEX_A
Reset:	soft
Address:	4AC84h-4AC87h
Name:	Pipe Pre CSC Gamma Index
ShortName:	PRE_CSC_GAMC_INDEX_B
Reset:	soft
Address:	4B484h-4B487h
Name:	Pipe Pre CSC Gamma Index
ShortName:	PRE_CSC_GAMC_INDEX_C
Reset:	soft
Address:	4BC84h-4BC87h
Name:	Pipe Pre CSC Gamma Index
ShortName:	PRE_CSC_GAMC_INDEX_D
Reset:	soft

DWord	Bit	Description
0	31:11	**Reserved** Access: RO Format: MBZ
	10	**Index Auto Increment** Access: R/W This field enables the index auto increment. 0b – No Increment – Do not automatically increment the index value. 1b – Auto Increment **[Default]** – Increment the index value with each read or write to the data register.
	9:8	**Reserved** Access: RO Format: MBZ

PRE_CSC_GAMC_INDEX

	7:0	**Index Value** Access: Write/Read Status This index controls access to the array of pipe pre color space conversion gamma values. This value can be automatically incremented by a read or a write to the data register if the index auto increment bit is set. When automatically incrementing, the index will roll over to 0 after writing or reading the entire allowed range. While in auto increment mode, after performing reads or writes to only part of the range, the auto increment bit must be cleared before resetting the index value. **Value** / **Name** [0,130]

Predicate Rendering Data Result

MI_PREDICATE_RESULT - Predicate Rendering Data Result		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
DWord	**Bit**	**Description**
0	31:1	**Reserved** Access: R/W Format: PBC
	0	**MI_PREDICATE_RESULT** Access: R/W This bit is the result of the last MI_PREDICATE.

Predicate Rendering Data Result 1

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0241Ch-0241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_RCSUNIT_CTX
Address:	2241Ch-2241Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_BCSUNIT_CTX
Address:	1C041Ch-1C041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT0_CTX
Address:	1C441Ch-1C441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT1_CTX
Address:	1C841Ch-1C841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT0_CTX
Address:	1D041Ch-1D041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT2_CTX
Address:	1D441Ch-1D441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT3_CTX
Address:	1D841Ch-1D841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT1_CTX
Address:	1E041Ch-1E041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT4_CTX
Address:	1E441Ch-1E441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT5_CTX

MI_PREDICATE_RESULT_1 - Predicate Rendering Data Result 1

Address:	1E841Ch-1E841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT2_CTX

Address:	1F041Ch-1F041Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT6_CTX

Address:	1F441Ch-1F441Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VCSUNIT7_CTX

Address:	1F841Ch-1F841Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_VECSUNIT3_CTX

Address:	1A41Ch-1A41Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_CCSUNIT0_CTX

Address:	1C41Ch-1C41Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_CCSUNIT1_CTX

Address:	1E41Ch-1E41Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_CCSUNIT2_CTX

Address:	2641Ch-2641Fh
Name:	Predicate Rendering Data Result 1
ShortName:	MI_PREDICATE_RESULT_1_CCSUNIT3_CTX

DWord	Bit	Description
0	31:1	**Reserved** Access: R/W Format: PBC
	0	**MI_PREDICATE_RESULT_1** Access: R/W

Predicate Rendering Data Result 2

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	023BCh-023BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_RCSUNIT
Address:	223BCh-223BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_BCSUNIT
Address:	1C03BCh-1C03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT0
Address:	1C43BCh-1C43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT1
Address:	1C83BCh-1C83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT0
Address:	1D03BCh-1D03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT2
Address:	1D43BCh-1D43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT3
Address:	1D83BCh-1D83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT1
Address:	1E03BCh-1E03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT4
Address:	1E43BCh-1E43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT5

MI_PREDICATE_RESULT_2 - Predicate Rendering Data Result 2

Address:	1E83BCh-1E83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT2

Address:	1F03BCh-1F03BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT6

Address:	1F43BCh-1F43BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VCSUNIT7

Address:	1F83BCh-1F83BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_VECSUNIT3

Address:	1A3BCh-1A3BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_CCSUNIT0

Address:	1C3BCh-1C3BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_CCSUNIT1

Address:	1E3BCh-1E3BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_CCSUNIT2

Address:	263BCh-263BFh
Name:	Predicate Rendering Data Result 2
ShortName:	MI_PREDICATE_RESULT_2_CCSUNIT3

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**MI_PREDICATE_RESULT_2** Access: R/W This bit must be loaded with by SW based on GT mode of operation. This register must be loaded appropriately before using MI_SET_PREDICATE command. 0h **[Default]** Indicates GT2 mode and lower slice is disabled. 1h Indicates GT3 mode and lower slice is enabled.

Predicate Rendering Data Storage

MI_PREDICATE_DATA - Predicate Rendering Data Storage

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

DWord	Bit	Description
0	63:32	**MI_PREDICATE_DATA_UDW** Access: R/W This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.
	31:0	**MI_PREDICATE_DATA_LDW** Access: R/W This register is used either as computed value based off the MI_PREDICATE_SRC0 and MI_PREDICATE_SRC1 or a temporary register. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register0

MI_PREDICATE_SRC0 - Predicate Rendering Temporary Register0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC0** Access: R/W This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predicate Rendering Temporary Register1

MI_PREDICATE_SRC1 - Predicate Rendering Temporary Register1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

DWord	Bit	Description
0	63:0	**MI_PREDICATE_SRC1** Access: R/W This register is a temporary register for Predicate Rendering. See Predicate Rendering section for more details.

Predication Mask Register

PREDICATION_MASK - Predication Mask Register	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	021FCh-021FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_RCSUNIT_CTX
Address:	221FCh-221FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_BCSUNIT_CTX
Address:	1C01FCh-1C01FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VCSUNIT0_CTX
Address:	1C41FCh-1C41FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VCSUNIT1_CTX
Address:	1C81FCh-1C81FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VECSUNIT0_CTX
Address:	1D01FCh-1D01FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VCSUNIT2_CTX
Address:	1D41FCh-1D41FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VCSUNIT3_CTX
Address:	1D81FCh-1D81FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VECSUNIT1_CTX
Address:	1E01FCh-1E01FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VCSUNIT4_CTX
Address:	1E41FCh-1E41FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VCSUNIT5_CTX
Address:	1E81FCh-1E81FFh

PREDICATION_MASK - Predication Mask Register

Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VECSUNIT2_CTX
Address:	1F01FCh-1F01FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VCSUNIT6_CTX
Address:	1F41FCh-1F41FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VCSUNIT7_CTX
Address:	1F81FCh-1F81FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_VECSUNIT3_CTX
Address:	1A1FCh-1A1FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_CCSUNIT0_CTX
Address:	1C1FCh-1C1FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_CCSUNIT1_CTX
Address:	1E1FCh-1E1FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_CCSUNIT2_CTX
Address:	261FCh-261FFh
Name:	Predication Mask Register
ShortName:	PREDICATION_MASK_CCSUNIT3_CTX

Value programmed in this register is used in computation of predication status on executing MI_SET_PREDICATE command.
This is a non-privileged registers and context save/restored on a context switch.

DWord	Bit	Description
0	31:0	**Predication Mask Value** Default Value: 00000000h Access: R/W

Preemption Status

PREEMPTION_STATUS - Preemption Status	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	025ACh-025AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_RCSUNIT_CTX
Address:	225ACh-225AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_BCSUNIT_CTX
Address:	1C05ACh-1C05AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT0_CTX
Address:	1C45ACh-1C45AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT1_CTX
Address:	1C85ACh-1C85AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VECSUNIT0_CTX
Address:	1D05ACh-1D05AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT2_CTX
Address:	1D45ACh-1D45AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT3_CTX
Address:	1D85ACh-1D85AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VECSUNIT1_CTX
Address:	1E05ACh-1E05AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT4_CTX
Address:	1E45ACh-1E45AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT5_CTX

PREEMPTION_STATUS - Preemption Status

Address:	1E85ACh-1E85AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VECSUNIT2_CTX

Address:	1F05ACh-1F05AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT6_CTX

Address:	1F45ACh-1F45AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VCSUNIT7_CTX

Address:	1F85ACh-1F85AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_VECSUNIT3_CTX

Address:	1A5ACh-1A5AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_CCSUNIT0_CTX

Address:	1C5ACh-1C5AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_CCSUNIT1_CTX

Address:	1E5ACh-1E5AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_CCSUNIT2_CTX

Address:	265ACh-265AFh
Name:	PREEMPTION_STATUS
ShortName:	PREEMPTION_STATUS_CCSUNIT3_CTX

This register captures the context switch status on a context switch and gets saved as part of the context image. This register doesn't get restored on a context restore. For all functional purpose this register must be red or sampled form the context image in memory and must not be sampled live from reading to this register.
This register is for HW internal purpose and must not be programmed by SW.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:13	**CS Engine ID** Access: RO This field holds the EngineID of the command streamer on which the context got recently executed.

PREEMPTION_STATUS - Preemption Status

12:7 CS Instance ID

Access:	RO

This field holds the InstanceID of the command streamer on which the context got recently executed.

6:4 Reserved

Access:	RO
Format:	MBZ

3:2 Context Switch Status

Access:	RO

This field indicates the preemption boundary and must be inferred based on the value in "Pipeline Selection" field.

Value	Name	Description	Exists If
0h		**Command Boundary:** Context switched out on a clean command boundary with no work pending from the commands executed.	
1h		**Thread Group Boundary:** Context got switched out in middle of workload (Media/GPGPU Walker) execution in Media or GPGPU mode of operation. Workload got preempted on a thread group boundary. HW will resume from the point it got preempted on resubmission of the context.	//PipelineSelection != 0
1h		**Object Boundary:** Context got switch out in middle of workload (3DPRIMTIVE) execution in 3D mode of operation. Workload got preempted on an object level boundary. HW will resume from the point it got preempted on resubmission of the context.	//PipelineSelection == 0
2h		**Mid Thread Boundary:**Context got switched out in middle of workload (Media/GPGPU Walker) execution in Media or GPGPU mode of operation. Workload got preempted in middle of thread execution (mid-thread boundary). HW will resume from the point it got preempted on resubmission of the context.	//PipelineSelection != 0
3h	Reserved		

1:0 Pipeline Selection

Access:	RO
Format:	U2

This bit indicates the pipeline select mode (PIPELINE_SELECT) at the time of context switch.

Value	Name	Description
0h		3D mode of operation.
1h		Media mode of operation.

PREEMPTION_STATUS - Preemption Status				
		2h		GPGPU mode of operation.
		3h	Reserved	

PRERESETMessagingRegister

MSG_RESET_PRE_GCP - PRERESETMessagingRegister

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 0866Ch

PRE RESET Messaging Register for Clocking Unit

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**Request to Prepare for GSC Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cgscrst_b Domain Reset (GSC).
	28:21	**Reserved** Access: RO Format: MBZ
	20	**Request to Prepare for VEBox3 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cvrst_b Domain Reset (vecs3unit).
	19	**Request to Prepare for VEBox2 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cvrst_b Domain Reset (vecs2unit).
	18	**Request to Prepare for VEBox1 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cvrst_b Domain Reset (vecs1unit).
	17	**Request to Prepare for VEBox0 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cvrst_b Domain Reset (vecs0unit).

MSG_RESET_PRE_GCP - PRERESETMessagingRegister

	16	**Request to Prepare for SFC3 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for csfcrst_b Domain Reset (vecs0unit).
	15	**Request to Prepare for SFC2 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for csfcrst_b Domain Reset (vecs0unit).
	14	**Request to Prepare for SFC1 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for csfcrst_b Domain Reset (vecs0unit).
	13	**Request to Prepare for SFC0 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for csfcrst_b Domain Reset (vecs0unit).
	12	**Request to Prepare for Media7 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cmrst_b Domain Reset (vcs7unit).
	11	**Request to Prepare for Media6 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cmrst_b Domain Reset (vcs6unit).
	10	**Request to Prepare for Media5 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cmrst_b Domain Reset (vcs5unit).
	9	**Request to Prepare for Media4 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cmrst_b Domain Reset (vcs4unit).

MSG_RESET_PRE_GCP - PRERESETMessagingRegister

	8	**Request to Prepare for Media3 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cmrst_b Domain Reset (vcs3unit).
	7	**Request to Prepare for Media2 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cmrst_b Domain Reset (vcs2unit).
	6	**Request to Prepare for Media1 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cmrst_b Domain Reset (vcs1unit).
	5	**Request to Prepare for Media0 Reset** Access: R/W _Custom_GTIReset: BUS Prepare for cmrst_b Domain Reset (vcs0unit).
	4	**Request to Prepare for Render Reset** Access: R/W _Custom_GTIReset: BUS Prepare for crrst_b Domain Reset (csunit).
	3	**Reserved**
	2	**Request to Prepare for Blitter Reset** Access: R/W _Custom_GTIReset: BUS Prepare for crblitrst_b Domain Reset (bcsunit).
	1	**Request to Prepare for Full Reset** Access: R/W _Custom_GTIReset: BUS Prepare for all the soft Domain Reset (csunit).

MSG_RESET_PRE_GCP - PRERESETMessagingRegister		
	0	**Request to Prepare for FLR** Access: R/W _Custom_GTIReset: BUS Prepare for devrst_b Domain Reset (FLR) Note: All resets except busrst_b are asserted for an FLR.

PRIMARY_SPI_ADDRESS

PRIMARY_SPI_ADDRESS - PRIMARY_SPI_ADDRESS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	102080h

Programming Notes

This register is used by software running on the CPU die. This register contains the SPI address offset from the SPI region base ID.

DWord	Bit	Description
0	31:0	**PrimarySPIAddress** Access: R/W _Custom_GTIReset: BUS This register contains the SPI address offset from the SPI region base ID.

PRIMARY_SPI_ERASE

PRIMARY_SPI_ERASE - PRIMARY_SPI_ERASE

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	102088h

Programming Notes

A write to this register will trigger a SPI Flash controller erase command. The triggered erase command will use the supplied data for Region ID and Erase size.
A read will return the data value of the last write. The read does not trigger a SPI access.

DWord	Bit	Description
0	31:24	**ERASEREGIONID** Default Value: 01h Access: RO Variant _Custom_GTIReset: BUS This byte is the Erase RegionID for an erase command.
	23:16	**SPARE** Default Value: 00h Access: RO _Custom_GTIReset: BUS This byte is a R/W spare register.
	15:0	**EraseSize** Default Value: 0000h Access: RO Variant _Custom_GTIReset: BUS Erase size value used for Primary initiated accesses targeting SPI Flash controller.

PRIMARY_SPI_REGIONID

PRIMARY_SPI_REGIONID - PRIMARY_SPI_REGIONID

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	102084h

Programming Notes

This register is used by software running on the CPU die. This register contains the SPI RegionID targeted.

DWord	Bit	Description
0	31:8	**Spare** Access: R/W _Custom_GTIReset: BUS This register contains spare R/W bits
	7:0	**PrimaryRegionID** Default Value: 01h Access: R/W _Custom_GTIReset: BUS Primary Region ID value used for Primary initiated accesses targeting SPI Flash controller.

PRIMARY_SPI_TRIGGER

PRIMARY_SPI_TRIGGER - PRIMARY_SPI_TRIGGER

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	102040h

Programming Notes

This register is used by software running on the CPU die. A register write will trigger a write to the SPI Flash Controller. A register read will trigger a read to the SPI Flash controller.

DWord	Bit	Description
0	31:0	**SPItrigger** Access: RO _Custom_GTIReset: BUS This register offset is used to trigger SPI R/W accesses from the primary host interface.

PRIMARY_SPI_TRIGGER2

PRIMARY_SPI_TRIGGER2 - PRIMARY_SPI_TRIGGER2

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	102044h

Programming Notes

This register is reserved as part of the SPI Flash trigger mechanism, given that a 64 bit access can occur.

DWord	Bit	Description
0	31:0	**SPItrigger** Access: RO _Custom_GTIReset: BUS This register is reserved as part of the SPI trigger mechanism, given that a 64 bit access can occur.

Primitives Generated By VF

IA_PRIMITIVES_COUNT - Primitives Generated By VF	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02318h-0231Fh
Name:	Primitives Generated By VF
ShortName:	IA_PRIMITIVES_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18318h-1831Fh
Name:	Primitives Generated By VF
ShortName:	IA_PRIMITIVES_COUNT_POCSUNIT_BE_GEOMETRY

This register stores the count of primitives generated by VF. This register is part of the context save and restore. More details about the precise event counted by this register are located in **Statistics Gathering.**

DWord	Bit	Description
0	63:32	**IA Primitives Count Report UDW** Access: R/W Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)
	31:0	**IA Primitives Count Report LDW** Access: R/W Total number of primitives output by the Vertex Fetch (IA) stage. This count is updated for every primitive output by the VF stage, as long as Statistics Enable is set in VF_STATE (see the Vertex Fetch Chapter in the 3D Volume.)

PRMRR_BASE_LSB

PRMRR_BASE_LSB - PRMRR_BASE_LSB

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	04CD8h

The PMRR range is used to protect Xucode memory from unauthorized reads and writes.
This register controls the location of the PRMRR range by indicating its starting address. It functions in tandem with the PRMRR mask register.
This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:12	**RANGE_BASE** Default Value: 00000h Access: R/W _Custom_GTIReset: BUS This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.
	11:4	**Reserved** Access: RO Format: MBZ
	3	**CONFIGURED** Default Value: 0h Access: R/W _Custom_GTIReset: BUS This bitfield is required to enable the PRMRR range
	2:0	**Reserved** Access: RO Format: MBZ

PRMRR_BASE_MSB

PRMRR_BASE_MSB - PRMRR_BASE_MSB	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	04CDCh

The PMRR range is used to protect Xucode memory from unauthorized reads and writes.
This register controls the location of the PRMRR range by indicating its starting address. It functions in tandem with the PRMRR mask register.
This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:0	**RANGE_BASE** Default Value: 00h Access: R/W _Custom_GTIReset: BUS This field corresponds to bits 63:32 of the base address memory range which is allocated to EMRR memory.

PRMRR_MASK_LSB

PRMRR_MASK_LSB - PRMRR_MASK_LSB

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	04CE0h

This register controls the size of the PRMRR range by indicating which address bits must match the PRMRR base register value.
This register is a LOCAL CR register and not an MMIO register

DWord	Bit	Description
0	31:12	**RANGE_MASK** Default Value: 00000h Access: R/W _Custom_GTIReset: BUS This field indicates which address bits must match PRMRR base in order to qualify as an PRMRR access.
	11	**RANGE_EN** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Indicates whether the EMRR range is enabled and valid.
	10	**SPARE** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This was lock bit.
	9	**IWB_EN** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Implicit Writeback enable. Used by the System agent with memory tracing.
	8	**Reserved**
	7:0	**Reserved** Access: RO Format: MBZ

PRMRR_MASK_MSB

PRMRR_MASK_MSB - PRMRR_MASK_MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	04CE4h	
This register controls the size of the PRMRR range by indicating which address bits must match the PRMRR base register value. This register is a LOCAL CR register and not an MMIO register		
DWord	**Bit**	**Description**
0	31:0	**RANGE_MASK** Default Value: 00h Access: R/W _Custom_GTIReset: BUS This field indicates which address bits must match PRMRR base in order to qualify as an PRMRR access.

ProgramShadow_2

PROGSHADOW_2 - ProgramShadow_2		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00EE8h-00EEBh	
DWord	**Bit**	**Description**
0	31:26	**Reserved** Access: RO Format: MBZ
	25:0	**Shadow Address** Default Value: 00000h Access: R/W Programmable shadow register address.

ProgramShadow_3

PROGSHADOW_3 - ProgramShadow_3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00EECh-00EEFh	
DWord	**Bit**	**Description**
0	31:26	**Reserved** Access: RO Format: MBZ
	25:0	**Shadow Address** Default Value: 00000h Access: R/W Programmable shadow register address.

PS_ADAPTIVE_CTRL

PS_ADAPTIVE_CTRL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	681A8h-681ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_A
Reset:	soft
Address:	681ACh-681AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_A
Reset:	soft
Address:	682A8h-682ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_A
Reset:	soft
Address:	682ACh-682AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_A
Reset:	soft
Address:	689A8h-689ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_B
Reset:	soft
Address:	689ACh-689AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_B
Reset:	soft
Address:	68AA8h-68AABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_B
Reset:	soft
Address:	68AACh-68AAFh

PS_ADAPTIVE_CTRL

Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_B
Reset:	soft

Address:	691A8h-691ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_C
Reset:	soft

Address:	691ACh-691AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_C
Reset:	soft

Address:	692A8h-692ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_C
Reset:	soft

Address:	692ACh-692AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_C
Reset:	soft

Address:	699A8h-699ABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_1_D
Reset:	soft

Address:	699ACh-699AFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_1_D
Reset:	soft

Address:	69AA8h-69AABh
Name:	PS Adaptive Control Set 0 1
ShortName:	PS_ADAPTIVE_CTRL_SET_0_2_D
Reset:	soft

Address:	69AACh-69AAFh
Name:	PS Adaptive Control Set 1 1
ShortName:	PS_ADAPTIVE_CTRL_SET_1_2_D
Reset:	soft

Programming Notes

PS_ADAPTIVE_CTRL

Recommended threshold programming:
Threshold 1: 1Eh
Threshold 2: 2Dh
Threshold 3: 3Ch

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:16	**Threshold 3** Access: Double Buffered This field specifies the third threshold value used in adaptive filtering.
	15:8	**Threshold 2** Access: Double Buffered This field specifies the second threshold value used in adaptive filtering.
	7:0	**Threshold 1** Access: Double Buffered This field specifies the first threshold value used in adaptive filtering.

PS_COEF_DATA

PS_COEF_DATA	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	6819Ch-6819Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_A
Reset:	soft
Address:	681A4h-681A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_A
Reset:	soft
Address:	6829Ch-6829Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_A
Reset:	soft
Address:	682A4h-682A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_A
Reset:	soft
Address:	6899Ch-6899Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_B
Reset:	soft
Address:	689A4h-689A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_B
Reset:	soft
Address:	68A9Ch-68A9Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_B
Reset:	soft
Address:	68AA4h-68AA7h

PS_COEF_DATA	
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_B
Reset:	soft
Address:	6919Ch-6919Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_C
Reset:	soft
Address:	691A4h-691A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_C
Reset:	soft
Address:	6929Ch-6929Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_C
Reset:	soft
Address:	692A4h-692A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_C
Reset:	soft
Address:	6999Ch-6999Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_1_D
Reset:	soft
Address:	699A4h-699A7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_1_D
Reset:	soft
Address:	69A9Ch-69A9Fh
Name:	PS Coeffecient Set 0 Data 1
ShortName:	PS_COEF_SET_0_DATA_2_D
Reset:	soft
Address:	69AA4h-69AA7h
Name:	PS Coeffecient Set 1 Data 1
ShortName:	PS_COEF_SET_1_DATA_2_D
Reset:	soft
These are the coefficient values for scaler.	

PS_COEF_DATA

The scaler coefficient Index indicates the coefficients array location to be accessed through this register.
The contents of the coefficient array is uninitialized until Software loads the array (i.e. the array is not resetable). Use of the coefficient array or reading from the coefficient array before Software has initialized it will result in non-deterministic behavior or read back data.

Restriction
This register must be written only as a full 32 bit dword. Byte or word writes are not supported.

DWord	Bit	Description
0	31:16	**Coefficient2** Access: Double Buffered Format: **SCALER_COEFFICIENT_FORMAT** Specifies the value for the second coefficient stored in this dword.
	15:0	**Coefficient1** Access: Double Buffered Format: **SCALER_COEFFICIENT_FORMAT** Specifies the value for the first coefficient stored in this dword.

PS_COEF_INDEX

PS_COEF_INDEX	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	68198h-6819Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_A
Reset:	soft
Address:	681A0h-681A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_A
Reset:	soft
Address:	68298h-6829Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_A
Reset:	soft
Address:	682A0h-682A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_A
Reset:	soft
Address:	68998h-6899Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_B
Reset:	soft
Address:	689A0h-689A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_B
Reset:	soft
Address:	68A98h-68A9Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_B
Reset:	soft
Address:	68AA0h-68AA3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_B

PS_COEF_INDEX

Reset:	soft
Address:	69198h-6919Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_C
Reset:	soft
Address:	691A0h-691A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_C
Reset:	soft
Address:	69298h-6929Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_C
Reset:	soft
Address:	692A0h-692A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_C
Reset:	soft
Address:	69998h-6999Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_1_D
Reset:	soft
Address:	699A0h-699A3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_1_D
Reset:	soft
Address:	69A98h-69A9Bh
Name:	PS Coeffecient Set 0 Index 1
ShortName:	PS_COEF_SET_0_INDEX_2_D
Reset:	soft
Address:	69AA0h-69AA3h
Name:	PS Coeffecient Set 1 Index 1
ShortName:	PS_COEF_SET_1_INDEX_2_D
Reset:	soft

DWord	Bit	Description	
0	31:11	**Reserved**	
		Access:	RO

PS_COEF_INDEX

	Format:	MBZ

10 Index Auto Increment

Access:	R/W

This field enables the index auto increment.

Value	Name	Description
0b	No Increment	Do not automatically increment the index value.
1b	Auto Increment **[Default]**	Increment the index value with each read or write to the data register.

9:6 Reserved

Access:	RO
Format:	MBZ

5:0 Index Value

Access:	R/W

This index controls access to the array of scaler coefficient values.

Value	Name
[0,59]	

PS_CTRL

PS_CTRL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68180h-68183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_A
Reset:	soft
Address:	68280h-68283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_A
Reset:	soft
Address:	68980h-68983h
Name:	PS Control 1
ShortName:	PS_CTRL_1_B
Reset:	soft
Address:	68A80h-68A83h
Name:	PS Control 1
ShortName:	PS_CTRL_2_B
Reset:	soft
Address:	69180h-69183h
Name:	PS Control 1
ShortName:	PS_CTRL_1_C
Reset:	soft
Address:	69280h-69283h
Name:	PS Control 1
ShortName:	PS_CTRL_2_C
Reset:	soft
Address:	69980h-69983h
Name:	PS Control 1
ShortName:	PS_CTRL_1_D
Reset:	soft
Address:	69A80h-69A83h

PS_CTRL

Name:	PS Control 1
ShortName:	PS_CTRL_2_D
Reset:	soft

Description

The pipe scalers are used to scale the output of a display pipe or of a display plane. All pipes have two scalers each.
The scaler preserves 8 bits of alpha and 10 bits of each color channel for plane scaling and 12 bits of each color channel for pipe scaling.
The scalers can be assigned to any plane (except cursor) output or the output of the display pipe (after blending and color correction, before dithering and color clamping).
Downscale usages have scale factor restrictions:

- All scaler modes support a downscale factor of less than 3.0 in each direction.
- Pipe YUV 420 encoding for port output supports Y downscale factor of less than 1.5 in each direction.

Beyond the restrictions of the Scaler output fitting within the destination window size, there are effectively no upscale restrictions except for the following:
(Scale Factor) * 2^{15} >= 1.0
Where the Scale Factor = (Source Size) / (Destination Size)

The scalers support horizontal source sizes up to 5120 and vertical source sizes up to 4096.

Programming Notes

The scalers must not be enabled when the horizontal source sizes are greater than 5120 and the vertical sizes greater than 4320.

Driver is responsible for making sure all the plane, pipe, and scaler size registers are programmed appropriately and gets applied atomically to the same frame since hardware does not ensure an atomic update of plane, scaler, and pipe source size registers.

When scaling a pipe, the scaler window size and position must fit within the pipe active size. If there is a seam present (i.e. PIPE_SEAM_EXCESS is non-zero), then the pipe's horizontal active size that the scaler sees is the horizontal active size defined within the TRANS_HTOTAL register plus the amount(s) specified within the PIPE_SEAM_EXCESS.
Pipe Horizontal Active = Horizontal Active + Left Excess Amount + Right Excess Amount

Refer to 'YUV 420 Support' page for scaler restrictions with YUV 420 pipe output.

Restriction

Down scaling (scaler input size is larger than scaler window size) can reduce the maximum supported pixel rate for a pipe as well as increase the watermark and data buffer requirements. Refer to the Display Resolution Support page and Watermark Calculations page for detailed calculations.

Scaler 1 and 2 must not be both scaling the same plane output.
When scaling a pipe, the scaler window size and position must fit within the pipe active size.
When scaling a plane, the plane position must be programmed to 0 and the scaler window size and position must fit within the pipe source size.
When scaling is enabled, the scaler input width should be a minimum of 8 pixels and the height should be minimum of 8 scanlines.

PS_CTRL

When the plane scaling is used with YUV 420 planar formats, the height should be a minimum of 16 scanlines. When using down scaling (scaler input size is larger than scaler output size) the maximum supported pixel rate will be reduced by the down scale amount.

DWord	Bit	Description
0	31	**Enable Scaler** Access: Double Buffered This field enables the scaler. 0b: Disable 1b: Enable
	30	**Reserved** Access: Double Buffered
	29	**Reserved** Access: RO Format: MBZ
	28	**Adaptive Filtering** Access: Double Buffered This field enables the scaler adaptive vertical and horizontal filtering. When adaptive filtering is enabled, the adaptive threshold values must be programmed in the PS_ADAPTIVE_CTRL register and the Filter Set Select bits should be programmed. 0h: Disable 1h: Enable
	27:25	**Scaler Binding** Access: Double Buffered This field selects the where the scaling operation is done. When scaling a pipe, the pipe source size specifies the input size to the scaler. When scaling a plane, the PLANE_SIZE specifies the input size to the scaler. Any border around a scaled plane window will become transparent at the plane blender. 000b: Pipe Scaler 001b: Plane 1 Scaler 010b: Plane 2 Scaler 011b: Plane 3 Scaler 100b: Plane 4 Scaler 101b: Plane 5 Scaler

PS_CTRL

Programming Notes
When plane scaling is enabled on planes 1 through 3, make sure that the *PLANE_CUS_CTL. Plane Scaling Enabled* (bit 30) is programmed correctly.

Restriction
The scaler input size should be at least 8 scanlines. Plane/Pipe scaling is not compatible with interlaced fetch mode. Plane up and down scaling is not compatible with keying. Keying can be enabled with 1:1 plane scaling. Plane scaling is not compatible with the Indexed 8-bit, XR_BIAS, or any pixel values less than 0 or greater than 1.

24:23 **FILTER SELECT**

Access:	Double Buffered

This field selects filter coefficients. The medium coefficients will provide an unfiltered image when the scale factor is 1:1.

In the programmed mode, the filter coefficients must be programmed using the PS_COEF_INDEX and PS_COEF_DATA registers and the Filter Set Select bits should be programmed.

Value	Name
00b	Medium
01b	Programmed
10b	Edge Enhance
11b	Bilinear

22 **ADAPTIVE FILTER SELECT**

Access:	Double Buffered

This field selects the filter coefficients used for adaptive filtering. The field is ignored when adaptive filtering is not enabled.

Value	Name
0b	Medium
1b	Edge Enhance

21 **Pipe Scaler Location**

Access:	Double Buffered

This field selects where the pipe scaling is done in the pipe.

Value	Name	Description
0b	After Output CSC	This is a non-linear tap point
1b	After CSC	This is a linear tap point

PS_CTRL

		Restriction The HDR Mode cannot be enabled for the Pipe(PIPE_MISC[23] = 0), when the Scaler is bound to the linear tap point
	20	**Reserved** Access: Double Buffered
	19	**Reserved** Access: Double Buffered
	18	**Reserved** Access: RO Format: MBZ
	17	**Reserved** Access: Double Buffered
	16	**Reserved** Access: RO Format: MBZ
	15	**Reserved** Access: Double Buffered
	14	**Reserved** Access: RO Format: MBZ
	13:12	**Reserved** Access: Double Buffered
	11:10	**Reserved** Access: RO Format: MBZ
	9	**Allow DB Stall** Access: R/W This field controls whether double buffer updates are allowed to be stalled for this scaler. **Value** / **Name** 0b: Not Allowed 1b: Allowed **[Default]**
	8	**Reserved** Access: Double Buffered
	7:5	**Reserved** Access: RO Format: MBZ

PS_CTRL

	4	**Y Vert Filter Set Sel** Access: Double Buffered This field selects the programmed coefficient set and/or the adaptive threshold set used by the Y component vertical filter when filtering YUV planar formats. This field is ignored with other formats. **Value** / **Name** 0b: Set 0 **[Default]** 1b: Set 1
	3	**Y Horz Filter Set Sel** Access: Double Buffered This field selects the programmed coefficient set and/or the adaptive threshold set used by the Y component horizontal filter when filtering YUV hybrid planar formats. This field is ignored with other formats. **Value** / **Name** 0b: Set 0 **[Default]** 1b: Set 1
	2	**UV Vert Filter Set Sel** Access: Double Buffered This field selects the programmed coefficient set and/or the adaptive threshold set used by the UV component vertical filter when filtering YUV hybrid planar formats. With other formats, this field selects the coefficient set and/or the adaptive threshold set used by the vertical filter. **Value** / **Name** 0b: Set 0 **[Default]** 1b: Set 1
	1	**UV Horz Filter Set Sel** Access: Double Buffered This field selects the programmed coefficient set and/or the adaptive threshold set used by the UV component horizontal filter when filtering YUV hybrid planar formats. With other formats, this field selects the coefficient set and/or the adaptive threshold set used by the horizontal filter. **Value** / **Name** 0b: Set 0 **[Default]** 1b: Set 1
	0	**Reserved** Access: RO Format: MBZ

PS_ECC_STAT

PS_ECC_STAT	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	681D0h-681D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_A
Reset:	soft
Address:	682D0h-682D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_A
Reset:	soft
Address:	689D0h-689D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_B
Reset:	soft
Address:	68AD0h-68AD3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_B
Reset:	soft
Address:	691D0h-691D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_C
Reset:	soft
Address:	692D0h-692D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_C
Reset:	soft
Address:	699D0h-699D3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_1_D
Reset:	soft
Address:	69AD0h-69AD3h
Name:	PS ECC Status 1
ShortName:	PS_ECC_STAT_2_D

PS_ECC_STAT

Reset: soft

Each of these fields is a sticky bit that gives the ECC error status for a particular memory bank. A '1' in a bit indicates that ECC detected an error. A write of '1' to a bit will clear the bit. Single errors are corrected by ECC. Double errors are not correctable.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16	**Double Error Detected** Access: R/WC
	15:1	**Reserved** Access: RO Format: MBZ
	0	**Single Error Detected** Access: R/WC

PS_HPHASE

PS_HPHASE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of horizontal blank after armed
Address:	68194h-68197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_A
Reset:	soft
Address:	68294h-68297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_A
Reset:	soft
Address:	68994h-68997h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_B
Reset:	soft
Address:	68A94h-68A97h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_B
Reset:	soft
Address:	69194h-69197h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_C
Reset:	soft
Address:	69294h-69297h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_2_C
Reset:	soft
Address:	69994h-69997h
Name:	PS Horizontal Phase 1
ShortName:	PS_HPHASE_1_D
Reset:	soft
Address:	69A94h-69A97h

PS_HPHASE

Name: PS Horizontal Phase 1
ShortName: PS_HPHASE_2_D
Reset: soft

Description

This register programs the scaler horizontal filtering initial phase.
The initial phase within the -0.5 to 1.5 range is supported. Refer to PS_VPHASE for programming details.

The programming of this register is ignored by the pipe scaler when the pipe is in the Full Blend YUV420 mode. The scaler hardware is responsible for calculating and applying the appropriate horizontal phase when encoding the YUV420 format.

DWord	Bit	Description
0	31:30	**Y Initial HPhase Int** Access: Double Buffered This field specifies the integer part of the Y horizontal filtering initial phase when the scaler is operating on YUV420 hybrid planar formats. This field is ignored for non-YUV420 pixel formats.
	29:17	**Y Initial HPhase Frac** Access: Double Buffered This field specifies the most significant 13 bits of the fractional part of the Y horizontal filtering initial phase when the scaler is operating onYUV420 hybrid planar formats. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13. This field is ignored for non-YUV420 pixel formats.
	16	**Y Initial HPhase Trip** Access: Double Buffered This field specifies whether the initial trip, that may occur while applying the initial phase, is used in Y horizontal filtering. This field is ignored for non-YUV420 pixel formats. Value: 1b — Name: Enable Value: 0b — Name: Disable
	15:14	**UV or RGB Initial HPhase Int** Access: Double Buffered This field specifies the integer part of the UV or RGB horizontal filtering initial phase.
	13:1	**UV or RGB Initial HPhase Frac** Access: Double Buffered This field specifies the most significant 13 bits of the fractional part of the UV or RGB horizontal filtering initial phase. This field should be programmed with the fractional portion of the initial phase multiplied by 2^13.

PS_HPHASE		
	0	**UV or RGB Initial HPhase Trip** Access: Double Buffered This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB horizontal filtering. **Value** / **Name** 1b – Enable 0b – Disable

PS_HSCALE

PS_HSCALE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	68190h-68193h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_A
Reset:	soft
Address:	68290h-68293h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_A
Reset:	soft
Address:	68990h-68993h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_B
Reset:	soft
Address:	68A90h-68A93h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_B
Reset:	soft
Address:	69190h-69193h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_C
Reset:	soft
Address:	69290h-69293h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_C
Reset:	soft
Address:	69990h-69993h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_1_D
Reset:	soft
Address:	69A90h-69A93h
Name:	PS Horizontal Scale 1
ShortName:	PS_HSCALE_2_D

PS_HSCALE

Reset: soft

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17:15	**HScale Int** Access: RO This field gives the integer part of the horizontal scaling factor divided by the oversampling rate. HSCALE_INT = int(src width/dest width)
	14:0	**HScale Frac** Access: RO This field gives the fractional part of the horizontal scaling factor divided by the oversampling rate. HSCALE_FRAC = int((((src width/dest width)-HSCALE_INT) * 2^^15) + 0.5)

PS_PROG_HSCALE

PS_PROG_HSCALE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68168h-6816Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_A
Reset:	soft
Address:	68268h-6826Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_A
Reset:	soft
Address:	68968h-6896Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_B
Reset:	soft
Address:	68A68h-68A6Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_B
Reset:	soft
Address:	69168h-6916Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_C
Reset:	soft
Address:	69268h-6926Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_2_C
Reset:	soft
Address:	69968h-6996Bh
Name:	PS Programmed Horizontal Scale 1
ShortName:	PS_PROG_HSCALE_1_D
Reset:	soft
Address:	69A68h-69A6Bh

PS_PROG_HSCALE

Name: PS Programmed Horizontal Scale 1

ShortName: PS_PROG_HSCALE_2_D

Reset: soft

This register is used to specify the horizontal scale factor when Programmable Scale Factor is enabled.

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17:15	**HScale Int** Access: Double Buffered This field gives the integer part of the horizontal scaling factor divided by the oversampling rate. HSCALE_INT = int(src width/dest width)
	14:0	**HScale Frac** Access: Double Buffered This field gives the fractional part of the horizontal scaling factor divided by the oversampling rate. HSCALE_FRAC = int(((src width/dest width)-HSCALE_INT)*2^^15)

PS_PROG_VSCALE

PS_PROG_VSCALE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68164h-68167h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_A
Reset:	soft
Address:	68264h-68267h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_A
Reset:	soft
Address:	68964h-68967h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_B
Reset:	soft
Address:	68A64h-68A67h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_B
Reset:	soft
Address:	69164h-69167h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_C
Reset:	soft
Address:	69264h-69267h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_2_C
Reset:	soft
Address:	69964h-69967h
Name:	PS Programmed Vertical Scale 1
ShortName:	PS_PROG_VSCALE_1_D
Reset:	soft
Address:	69A64h-69A67h

PS_PROG_VSCALE

Name: PS Programmed Vertical Scale 1
ShortName: PS_PROG_VSCALE_2_D
Reset: soft

This register is used to specify the vertical scale factor when Programmable Scale Factor is enabled.

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17:15	**VScale Int** Access: Double Buffered This field gives the integer part of the vertical scale factor. VSCALE_INT = int(src height/(interlace x dest height)) Interlace = 1/2 in interlace modes, 1 in progressive modes.
	14:0	**VScale Frac** Access: Double Buffered This field gives the fractional part of the vertical scale factor. VSCALE_FRAC = int((src height/(interlace x dest height)-VSCALE_INT)*2^^15) Interlace = 1/2 in interlace modes, 1 in progressive modes.

PS_PWR_GATE

PS_PWR_GATE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68160h-68163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_A
Reset:	soft
Address:	68260h-68263h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_A
Reset:	soft
Address:	68960h-68963h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_B
Reset:	soft
Address:	68A60h-68A63h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_B
Reset:	soft
Address:	69160h-69163h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_C
Reset:	soft
Address:	69260h-69263h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_2_C
Reset:	soft
Address:	69960h-69963h
Name:	Power Gate Control 1
ShortName:	PS_PWR_GATE_1_D
Reset:	soft
Address:	69A60h-69A63h

PS_PWR_GATE

Name: Power Gate Control 1
ShortName: PS_PWR_GATE_2_D
Reset: soft

DWord	Bit	Description
0	31	**Reserved** Access: Double Buffered
	30	**Reserved** Access: RO Format: MBZ
	29:6	**Reserved** Access: RO Format: MBZ
	5	**Dynamic Pwr Gate Disable** Access: Double Buffered Disables the dynamic power gate of unused EBB's when processing low resolution source images. Value: 0b — Name: Do Not Disable **[Default]** Value: 1b — Name: Disable
	4:3	**Reserved** Access: Double Buffered
	2	**Reserved** Access: RO Format: MBZ
	1:0	**Reserved** Access: Double Buffered

PS_VPHASE

PS_VPHASE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68188h-6818Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_A
Reset:	soft
Address:	68288h-6828Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_A
Reset:	soft
Address:	68988h-6898Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_B
Reset:	soft
Address:	68A88h-68A8Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_B
Reset:	soft
Address:	69188h-6918Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_C
Reset:	soft
Address:	69288h-6928Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_2_C
Reset:	soft
Address:	69988h-6998Bh
Name:	PS Vertical Phase 1
ShortName:	PS_VPHASE_1_D
Reset:	soft
Address:	69A88h-69A8Bh

PS_VPHASE

Name: PS Vertical Phase 1
ShortName: PS_VPHASE_2_D
Reset: soft

Description

This register programs the scaler vertical filtering initial phase. The programming of this register is ignored in the pipe scaler PF/ID fetch mode, and the pipe scaler is responsible for applying the appropriate vertical phase to the proper frame when interlacing.
The initial phase within the -0.5 to 1.5 range is supported.
Programming +ve initial phase:

- Initial Phase Trip = 1b
- Initial Phase Int = Desired Initial Phase Int
- Initial Phase Frac = Desired Initial Phase Frac

Programming -ve initial phase:

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - Desired Initial Phase Frac

For example, -0.25 initial phase should be programmed as

- Initial Phase Trip = 0b
- Initial Phase Int = 00b
- Initial Phase Frac = 1 - 0.25 = 0.75

The following table shows phase programming for frequently used YUV420 to YUV444 chroma upsampling scenarios (chroma being filtered to the center of the pixel).

YUV 420 Chroma Siting	H Phase	V Phase	Programmed H Initial Phase	Programmed H Initial Trip	Programmed V Initial Phase	Programmed V Initial Trip
Top Left	0.25	0.25	0.25	1	0.25	1
Bottom Right (MPEG-1)	-0.25	-0.25	0.75	0	0.75	0
Bottom Center (MPEG-2)	0	-0.25	0	0	0.75	0

The programming of this register is ignored by a pipe scaler when the pipe is in the Full Blend YUV420 mode. The scaler hardware is responsible for calculating and applying the appropriate vertical phase when encoding the YUV420 format.

DWord	Bit	Description
0	31:30	**Y Initial VPhase Int** Access: Double Buffered This field specifies the integer part of the Y vertical filtering initial phase when the scaler is

operating on YUV420 hybrid planar formats. This field is ignored for non-YUV420 pixel formats.

29:17 Y Initial VPhase Frac

Access:	Double Buffered

This field specifies the most significant 13 bits of the fractional part of the Y vertical filtering initial phase when the scaler is operating on YUV420 hybrid planar formats.
This field should be programmed with the fractional portion of the initial phase multiplied by 2^13.
This field is ignored for non-YUV420 pixel formats.

16 Y Initial VPhase Trip

Access:	Double Buffered

This field specifies whether the initial trip, that may occur while applying the initial phase, is used in Y vertical filtering. This field is ignored for non-YUV420 pixel formats.

Value	Name
1b	Used
0b	Not Used

15:14 UV or RGB Initial VPhase Int

Access:	Double Buffered

This field specifies the integer part of the UV or RGB vertical filtering initial phase.

13:1 UV or RGB Initial VPhase Frac

Access:	Double Buffered

This field specifies the most significant 13 bits of the fractional part of the UV or RGB vertical filtering initial phase.
This field should be programmed with the fractional portion of the initial phase multiplied by 2^13.

0 UV or RGB Initial VPhase Trip

Access:	Double Buffered

This field specifies whether the initial trip, that may occur while applying the initial phase, is used in UV or RGB vertical filtering.

Value	Name
1b	Used
0b	Not Used

PS_VSCALE

PS_VSCALE	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	68184h-68187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_A
Reset:	soft
Address:	68284h-68287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_A
Reset:	soft
Address:	68984h-68987h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_B
Reset:	soft
Address:	68A84h-68A87h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_B
Reset:	soft
Address:	69184h-69187h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_C
Reset:	soft
Address:	69284h-69287h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_C
Reset:	soft
Address:	69984h-69987h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_1_D
Reset:	soft
Address:	69A84h-69A87h
Name:	PS Vertical Scale 1
ShortName:	PS_VSCALE_2_D

PS_VSCALE

Reset: soft

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17:15	**VScale Int** Access: RO This field gives the integer part of the vertical scale factor. VSCALE_INT = int(src height/(interlace x dest height)) Interlace = 1/2 in interlace modes, 1 in progressive modes.
	14:0	**VScale Frac** Access: RO This field gives the fractional part of the vertical scale factor. VSCALE_FRAC = int(((src height/(interlace x dest height)-VSCALE_INT) * 2^^15) + 0.5) Interlace = 1/2 in interlace modes, 1 in progressive modes.

PS_WIN_POS

PS_WIN_POS	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PS_WIN_SZ
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank after armed
Address:	68170h-68173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_A
Reset:	soft
Address:	68270h-68273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_A
Reset:	soft
Address:	68970h-68973h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_B
Reset:	soft
Address:	68A70h-68A73h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_B
Reset:	soft
Address:	69170h-69173h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_C
Reset:	soft
Address:	69270h-69273h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_2_C
Reset:	soft
Address:	69970h-69973h
Name:	PS Window Position 1
ShortName:	PS_WIN_POS_1_D
Reset:	soft
Address:	69A70h-69A73h

PS_WIN_POS

Name: PS Window Position 1

ShortName: PS_WIN_POS_2_D

Reset: soft

Coordinates are determined with a value of (0,0) being the upper left corner of the display device (rotation does not affect this).

Restriction

When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**XPOS** Access: Double Buffered This field specifies the horizontal coordinate in pixels of the upper left most pixel of the scaled output window. Restriction : This field must be even when the scaler is delivering YUV420 format for HDMI output.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**YPOS** Access: Double Buffered This field specifies the vertical coordinate in lines of the upper left most pixel of the scaled output window. **Restriction** Bit 0 must be zero for interlaced modes. This field must be even when the scaler is delivering YUV420 format for HDMI output.

PS_WIN_SZ

PS_WIN_SZ	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank
Address:	68174h-68177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_A
Reset:	soft
Address:	68274h-68277h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_A
Reset:	soft
Address:	68974h-68977h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_B
Reset:	soft
Address:	68A74h-68A77h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_B
Reset:	soft
Address:	69174h-69177h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_C
Reset:	soft
Address:	69274h-69277h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_2_C
Reset:	soft
Address:	69974h-69977h
Name:	PS Window Size 1
ShortName:	PS_WIN_SZ_1_D
Reset:	soft
Address:	69A74h-69A77h
Name:	PS Window Size 1

PS_WIN_SZ

ShortName: PS_WIN_SZ_2_D

Reset: soft

This register specifies the size in pixels of the scaled output window. A programmed value of (100, 100) will result in scaled output window of size 100x100 pixels.
Writes to this register arm PS registers on this pipe. After arming, any write to other PS registers will disarm all PS registers. Subsequent write to this register will arm them again.

Restriction

When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**XSIZE** Access: Double Buffered This field specifies the horizontal size in pixels of the scaled output window. Restriction: When the pipe scalar is configured to output YUV 420, the X size must be even.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**YSIZE** Access: Double Buffered This field specifies the vertical size in scan lines of the scaled output window. Restriction : Bit 0 must be zero for interlaced modes. **Restriction** When the pipe scalar is configured to output YUV 420, the Y size must be even.

PS Depth Count

PS_DEPTH_COUNT - PS Depth Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02350h

This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume.
More details about the precise event counted by this register are located **Statistics Gathering.**

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice0

PS_DEPTH_COUNT_SLICE0 - PS Depth Count for Slice0	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	022D8h
Name:	PS Depth Count for Slice0
ShortName:	PS_DEPTH_COUNT_SLICE0

This register stores the value of the count of pixels that have passed the depth test in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the total number of pixels that have passed the depth test in Slice0(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice1

PS_DEPTH_COUNT_SLICE1 - PS Depth Count for Slice1	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	022F8h
Name:	PS Depth Count for Slice1
ShortName:	PS_DEPTH_COUNT_SLICE1

This register stores the value of the count of pixels that have passed the depth test in Slice1. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the total number of pixels that have passed the depth test in Slice1(i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice2

PS_DEPTH_COUNT_SLICE2 - PS Depth Count for Slice2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02450h
Name:	PS Depth Count for Slice2
ShortName:	PS_DEPTH_COUNT_SLICE2

This register stores the value of the count of pixels that have passed the depth test in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the depth test in slice2 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice3

PS_DEPTH_COUNT_SLICE3 - PS Depth Count for Slice3	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02460h
Name:	PS Depth Count for Slice3
ShortName:	PS_DEPTH_COUNT_SLICE3

This register stores the value of the count of pixels that have passed the depth test in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the depth test in slice3 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice4

PS_DEPTH_COUNT_SLICE4 - PS Depth Count for Slice4	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02470h
Name:	PS Depth Count for Slice4
ShortName:	PS_DEPTH_COUNT_SLICE4

This register stores the value of the count of pixels that have passed the depth test in Slice4. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the depth test in slice4 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the depth test in slice4 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice5

PS_DEPTH_COUNT_SLICE5 - PS Depth Count for Slice5	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	024A8h
Name:	PS Depth Count for Slice5
ShortName:	PS_DEPTH_COUNT_SLICE5

This register stores the value of the count of pixels that have passed the depth test in Slice5. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice6

PS_DEPTH_COUNT_SLICE6 - PS Depth Count for Slice6	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	025B0h
Name:	PS Depth Count for Slice6
ShortName:	PS_DEPTH_COUNT_SLICE6

This register stores the value of the count of pixels that have passed the depth test in Slice6. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Depth Count for Slice7

PS_DEPTH_COUNT_SLICE7 - PS Depth Count for Slice7	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	025B8h
Name:	PS Depth Count for Slice7
ShortName:	PS_DEPTH_COUNT_SLICE7

This register stores the value of the count of pixels that have passed the depth test in Slice7. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**Depth Count UDW** Access: R/W This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.
	31:0	**Depth Count LDW** Access: R/W This register reflects the depth test in slice5 (i.e., will be visible). All pixels are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Pixels that pass the depth test but fail the stencil test will not be counted.

PS Invocation Count

PS_INVOCATION_COUNT - PS Invocation Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02348h

More details about the precise event counted by this register are located **Statistics Gathering.**

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice0

PS_INVOCATION_COUNT_SLICE0 - PS Invocation Count for Slice0

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

Address:	022C8h
Name:	PS Invocation Count for Slice0
ShortName:	PS_INVOCATION_COUNT_SLICE0

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice0. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice1

PS_INVOCATION_COUNT_SLICE1 - PS Invocation Count for Slice1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	022F0h
Name:	PS Invocation Count for Slice1
ShortName:	PS_INVOCATION_COUNT_SLICE1

This register stores the value of the count of pixels that get shaded in Slice0. This register is part of the context save and restore. This register should not be programmed by SW. Note: In GT3 mode there are two slices Slice0 (Upper Slice) and Slice1 (Lower slice).

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice1. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice2

PS_INVOCATION_COUNT_SLICE2 - PS Invocation Count for Slice2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02448h
Name:	PS Invocation Count for Slice2
ShortName:	PS_INVOCATION_COUNT_SLICE2

This register stores the value of the count of pixels that get shaded in Slice2. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice2. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice3

PS_INVOCATION_COUNT_SLICE3 - PS Invocation Count for Slice3

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02458h
Name:	PS Invocation Count for Slice3
ShortName:	PS_INVOCATION_COUNT_SLICE3

This register stores the value of the count of pixels that get shaded in Slice3. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice3. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice4

PS_INVOCATION_COUNT_SLICE4 - PS Invocation Count for Slice4

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02468h
Name:	PS Invocation Count for Slice4
ShortName:	PS_INVOCATION_COUNT_SLICE4

This register stores the value of the count of pixels that get shaded in Slice4. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice5

PS_INVOCATION_COUNT_SLICE5 - PS Invocation Count for Slice5

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	024A0h
Name:	PS Invocation Count for Slice5
ShortName:	PS_INVOCATION_COUNT_SLICE5

This register stores the value of the count of pixels that get shaded in Slice5. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice6

PS_INVOCATION_COUNT_SLICE6 - PS Invocation Count for Slice6

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	025D0h
Name:	PS Invocation Count for Slice6
ShortName:	PS_INVOCATION_COUNT_SLICE6

This register stores the value of the count of pixels that get shaded in Slice6. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PS Invocation Count for Slice7

PS_INVOCATION_COUNT_SLICE7 - PS Invocation Count for Slice7	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	025D8h
Name:	PS Invocation Count for Slice7
ShortName:	PS_INVOCATION_COUNT_SLICE7

This register stores the value of the count of pixels that get shaded in Slice7. This register is part of the render context save and restore. This register should not be programmed by SW.

DWord	Bit	Description
0..1	63:32	**PS Invocation Count UDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.
	31:0	**PS Invocation Count LDW** Access: R/W Reflects a count of the total number of pixels (including unlit "helper pixels" within a subspan that need to go through the PS shader to provide 2x2 gradients) that are dispatched to pixel shader invocations while Statistics Enable is set in the Windower in Slice4. See the Windower chapter of the 3D volume for details. This count will generally be much greater than the actual count of PS threads since a single thread may process up to 32 pixels.

PSR_EVENT

PSR_EVENT	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	60848h-6084Bh
Name:	Transcoder PSR Event
ShortName:	PSR_EVENT_A
Reset:	soft
Address:	61848h-6184Bh
Name:	Transcoder PSR Event
ShortName:	PSR_EVENT_B
Reset:	soft
Address:	62848h-6284Bh
Name:	Transcoder PSR Event
ShortName:	PSR_EVENT_C
Reset:	soft
Address:	63848h-6384Bh
Name:	Transcoder PSR Event
ShortName:	PSR_EVENT_D
Reset:	soft

This register captures the event that caused an exit from PSR or PSR2. The exit events will be set by hardware. Software will need to clear these events.

DWord	Bit	Description
0	31:18	**Reserved** Access: RO Format: MBZ
	17	**PSR2 watch dog timer expire** Access: R/WC This is a sticky bit which is set when the PSR2 watch dog timer expires, causing PSR exit. Clear by writing with a 1. Value: 0b — Name: Condition Not Detected Value: 1b — Name: Condition Detected

PSR_EVENT

16 PSR2 Disable

Access:	R/WC

This is a sticky bit which is set when the PSR2 is disabled, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

15 Selective Update Dirty FIFO Underrun

Access:	R/WC

This is a sticky bit which is set when the selective update dirty/clean FIFO Underruns, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

14 Reserved

Access:	RO
Format:	MBZ

13 Reserved

Access:	RO
Format:	MBZ

12 Graphics Reset

Access:	R/WC

This is a sticky bit which is set when a graphics reset causes PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

11 PCH Interrupt

Access:	R/WC

This is a sticky bit which is set when a PCH Interrupt causes PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

10 Memory Up

Access:	R/WC

This is a sticky bit which is set when a PCU memup up event causes PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected

PSR_EVENT

	1b	Condition Detected

9 Front Buffer Modify

Access:	R/WC

This is a sticky bit which is set when a front buffer modify causes PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

8 Watch dog timer expire

Access:	R/WC

This is a sticky bit which is set when the PSR watch dog timer expires, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

7 Reserved

Access:	RO
Format:	MBZ

6 Pipe Registers Update

Access:	R/WC

This is a sticky bit which is set when a display pipe register update causes PSR exit. Clear by writing with a 1.

5 Reserved

Access:	RO
Format:	MBZ

4 Reserved

Access:	R/WC

3 KVMR session enable

Access:	R/WC

This is a sticky bit which is set when a KVMR session is enabled, causing PSR exit. Clear by writing with a 1.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

PSR_EVENT

	2	**VBI enable** Access: R/WC This is a sticky bit which is set when vblank or vsync interrupt is enabled, causing PSR exit. Clear by writing with a 1. Value: 0b — Name: Condition Not Detected Value: 1b — Name: Condition Detected
	1	**Reserved** Access: RO Format: MBZ
	0	**SRD disable** Access: R/WC This is a sticky bit which is set when SRD enable is cleared, causing PSR exit. Clear by writing with a 1. Value: 0b — Name: Condition Not Detected Value: 1b — Name: Condition Detected

PSR_IIR

PSR_IIR	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	60818h-6081Bh
Name:	Transcoder PSR Interrupt Identity
ShortName:	PSR_IIR_A
Reset:	soft
Address:	61818h-6181Bh
Name:	Transcoder PSR Interrupt Identity
ShortName:	PSR_IIR_B
Reset:	soft
Address:	62818h-6281Bh
Name:	Transcoder PSR Interrupt Identity
ShortName:	PSR_IIR_C
Reset:	soft
Address:	63818h-6381Bh
Name:	Transcoder PSR Interrupt Identity
ShortName:	PSR_IIR_D
Reset:	soft

This register holds the persistent values of the PSR interrupt bits which are unmasked by PSR_IMR. Bits set in this register will propagate to the PSR/SRD interrupt in the Display Engine Miscellaneous Interrupts.

DWord	Bit	Description
0	31:4	**Reserved** Access: RO Format: MBZ
	3	**Push Done** Access: R/WC This is a sticky bit which is set after double buffer update or Push done. After this interrupt, Logic is ready to receive another push frame indication. Clear by writing with a 1. 0b – Condition Not Detected 1b – Condition Detected

PSR_IIR

	2	**PSR Aux Error** Access: R/WC This is a sticky bit which is set on the rising edge of the PSR Aux error (receive error or timeout) indication. Clear by writing with a 1. **Value** / **Name** 0b: Condition Not Detected 1b: Condition Detected
	1	**PSR Exit** Access: R/WC This is a sticky bit which is set on the first blank start after PSR exit. Clear by writing with a 1. **Value** / **Name** 0b: Condition Not Detected 1b: Condition Detected
	0	**PSR PreWarn** Access: R/WC This is a sticky bit which is set two display frames prior to entering PSR. Clear by writing with a 1. **Value** / **Name** 0b: Not Detected 1b: Condition Detected

PSR_IMR

PSR_IMR	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60814h-60817h
Name:	Transcoder PSR Interrupt Mask
ShortName:	PSR_IMR_A
Reset:	soft
Address:	61814h-61817h
Name:	Transcoder PSR Interrupt Mask
ShortName:	PSR_IMR_B
Reset:	soft
Address:	62814h-62817h
Name:	Transcoder PSR Interrupt Mask
ShortName:	PSR_IMR_C
Reset:	soft
Address:	63814h-63817h
Name:	Transcoder PSR Interrupt Mask
ShortName:	PSR_IMR_D
Reset:	soft

This register contains a bit mask which selects the PSR events that will be reported in the PSR_IIR.

DWord	Bit	Description
0	31:4	**Reserved** Access: RO Format: MBZ
	3	**Mask Push Done** Access: R/W 0b: Not Masked 1b: Masked **[Default]**
	2	**Mask PSR Aux Error** Access: R/W 0b: Not Masked

PSR_IMR

		1b: Masked **[Default]**
	1	**Mask PSR Exit** Access: R/W 0b: Not Masked 1b: Masked **[Default]**
	0	**Mask PSR PreWarn** Access: R/W 0b: Not Masked 1b: Masked **[Default]**

PSR_MASK

PSR_MASK	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60860h-60863h
Name:	Transcoder PSR Event Mask
ShortName:	PSR_MASK_A
Reset:	soft
Address:	61860h-61863h
Name:	Transcoder PSR Event Mask
ShortName:	PSR_MASK_B
Reset:	soft
Address:	62860h-62863h
Name:	Transcoder PSR Event Mask
ShortName:	PSR_MASK_C
Reset:	soft
Address:	63860h-63863h
Name:	Transcoder PSR Event Mask
ShortName:	PSR_MASK_D
Reset:	soft

Some of the masking is controlled here and some in the PIPE_MISC register.

Restriction
Only bit 30 (Idle Frame Override) can be changed while PSR or PSR2 is enabled. The other fields must not be changed while PSR or PSR2 is enabled.

DWord	Bit	Description
0	31:30	**Idle Frame Override** Access: R/W This field overrides the entry/exit conditions to force PSR or PSR2 Deep Sleep entry/exit. Value / Name / Description: 00b,01b – No Override – Do not override. Use regular entry and exit conditions. 10b – Force Idle Frame – Force Idle Frames to force PSR entry or PSR2 Deep Sleep 11b – Force Non-Idle Frame – Force Non-Idle Frames to force PSR exit or exit from PSR2 Deep Sleep
	29	**Reserved** Access: RO Format: MBZ

PSR_MASK

28 Mask Max Sleep

Access:	R/W

This field controls the mask for the max sleep time event.

Value	Name
0b	Not Masked
1b	Masked

27 Reserved

Access:	RO
Format:	MBZ

26 Mask Memup

Access:	R/W

This field controls the mask for the memory up event.

Value	Name	Description
0b	Not Masked	
1b	Masked **[Default]**	Masked - will not be considered in PSR idleness tracking (default)

25 Mask Hotplug

Access:	R/W

This field controls the mask for the hotplug event .Not used in PSR2 Deep Sleep entry/exit.

Value	Name
0b	Not Masked
1b	Masked

24 Mask FBC Modify

Access:	R/W

This field controls the mask for the FBC front buffer modify event.

Value	Name
0b	Not Masked
1b	Masked

23:16 Reserved

Access:	RO
Format:	MBZ

15 Exit on Pixel Underrun

Access:	R/W

This field controls the mask for exit on pixel underrun.

Value	Name
0b	Not Masked
1b	Masked **[Default]**

PSR_MASK

	14:1	**Reserved** Access: RO Format: MBZ
	0	**Global Mask** Access: R/W This field is no longer used. The global mask function moved to 0x42084 bit 0. 0b – Not Masked 1b – Masked

PSR2_CTL

PSR2_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60900h-60903h
Name:	PSR2 Control
ShortName:	PSR2_CTL_A
Reset:	soft

Programming Notes

To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.

Restriction

PSR needs to be enabled only when at least one plane is enabled.

PSR2 is limited to 30bpp 10:10:10, even when using the manual tracking mode.

Only the PSR2 Enable can be changed while PSR2 is enabled. The other fields must not be changed while PSR2 is enabled. Selective Update Tracking Enable must be set before or along with PSR2 enable

PSR2 is supported for pipe active sizes up to 5120 pixels wide and 3200 lines tall.

DWord	Bit	Description
0	31	**PSR2 Enable** Access: R/W This bit enables Revision 2.0 of the Panel Self Refresh function. Updates will take place at the start of the next vertical blank. The port will send PSR2 VDMs while enabled. **Value** / **Name** 0b – Disable 1b – Enable **Programming Notes** Clear the register field SRD_CTL [TP2 TP3 Select] before enabling this bit. Do not set the register field SRD_CTL [TP2 TP3 Select] while PSR2 is enabled. **Restriction** **PSR2 not supported. Do not enable.** PSR2 must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line. PSR2 must not be enabled together with Interlacing, Black Frame Insertion (BFI), Compression Mode, or S3D.

PSR2_CTL

	Disable FBC when PSR2 is enabled.
30	**Reserved** Access: RO Format: MBZ
29	**Context restore to PSR2 Deep Sleep State** Access: R/W This field restores PSR2 into Deep Sleep State **Value** / **Name** 0b – Disable 1b – Enable **Restriction** This bit should only be used with context save restore.
28	**Block count number** Access: R/W This field selects block count number before SU turn on sequence **Value** / **Name** 0b – 2 blocks OR 8 lines 1b – 3 blocks OR 12 lines
27	**Aux Frame Sync Enable** Access: R/W This field selects whether the frame sync will be sent on Aux channel. **Value** / **Name** 1b – Enable 0b – Disable **Restriction** Must be programmed to match the panel's requirements.
26	**Reserved** Access: RO Format: MBZ
25	**SU SDP scanline indication** Access: R/W **Value** / **Name** / **Description** 0b / same line / Send the PSR2 start and end SDP on the same line as the SU region start and end lines.

PSR2_CTL

1b	prior line	Send the PSR2 start and end SDP one line prior to the SU region start and end lines.

24:20 Max SU Disable Time

Default Value:	00000b Disabled
Access:	R/W

This field is the maximum time to spend in PSR2 Selective update without fetching a full frame. It is programmed in increments of sixty frames. Programming all 1s gives 31x60 frames time.

Restriction
Programming all 0s disable the forced fetch of a full frame in SU.

19 Reserved

Access:	R/W

18 PSR2 RAM power state

Access:	RO

17:16 Reserved

Access:	R/W

15:13 IO buffer Wake

Access:	R/W

This field selects the number of lines before the Selective Update Region to wake the IO Buffers.

Value	Name
000b	5 lines
001b	6 lines
010b	7 lines **[Default]**
011b	8 lines
100b	9 lines
101b	10 lines
110b	11 lines
111b	12 lines

Restriction
To program line 9 to 12, block count number bit [28] must be set.

12:10 Fast Wake

Access:	R/W

This field selects the number of lines before the Selective Update Region to send the Fast Wake.

Value	Name
000b	5 lines
001b	6 lines

		010b: 7 lines **[Default]** 011b: 8 lines 100b: 9 lines 101b: 10 lines 110b: 11 lines 111b: 12 lines **Restriction** To program line 9 to 12, block count number bit [28] must be set.
	9:8	**TP2 Time** Access: R/W This field selects the TP2 time when training the link on exit from PSR2 DeepSleep (waking). 00b: 500us 01b: 100us 10b: 2.5ms 11b: 50us
	7:4	**Frames Before SU Entry** Default Value: 0001b 1 Frames Before SU Entry Access: R/W This field is the number of frames it takes to enter into Selective Update when PSR2 is enabled. Note: HW takes a minimum of 2frames, so'0' and '1' are not valid entries for this field.
	3:0	**Idle Frames** Access: R/W This field is the number of idle frames required before entering PSR2 Deep Sleep. Write to this field doesn't cause a PSR2 exit and frame update. 0000b: Deep Sleep Disabled 0001b: 1 idle frame **[Default]**

PSR2_MAN_TRK_CTL

PSR2_MAN_TRK_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	60910h-60913h
Name:	PSR2 Manual Tracking Control
ShortName:	PSR2_MAN_TRK_CTL_A
Reset:	soft

Address:	62910h-62913h
Name:	PSR2 Manual Tracking Control
ShortName:	PSR2_MAN_TRK_CTL_C
Reset:	soft

Address:	63910h-63913h
Name:	PSR2 Manual Tracking Control
ShortName:	PSR2_MAN_TRK_CTL_D
Reset:	soft

Description

This register instances are also used for configuration of **Panel Replay** feature on all pipes.

Programming Notes

The frame is divided into blocks of four scan lines each. The blocks are addressed starting from 1 for the first block of the frame and ending with ROUNDUP[(TRANS_VTOTAL Vertical Active + 1) / 4]for the last block of the frame.
Software must provide the starting and ending block address of the selective update region.
The SU Region Start Address is programmed to the first block of the selective update region.
The SU Region End Address is programmed to the final block of the selective update region + 1.
There can be only one selective update region in a frame.
To disable selective update, set the selective update region to the full frame by programming SU Region Start Address to the start of the frame and SU Region End Address to the end of the frame.

DWord	Bit	Description
0	31	**SF partial frame enable** Access: R/W This bit enables selective fetch.

Value	Name
0b	Disable
1b	Enable

PSR2_MAN_TRK_CTL

30	**Allow DB Stall** Access: R/W This field controls whether double buffer updates are allowed to be stalled for this register. Value: 0b — Name: Not Allowed **[Default]** Value: 1b — Name: Allowed
29	**Reserved** Access: RO Format: MBZ
28:16	**SU Region Start Address** Access: R/W This field indicates the starting line address of the selective update region.
15	**Reserved** Access: RO Format: MBZ
14	**SF Single full frame** Access: R/W Set This bit will select for a single a full frame fetch and update when Selective Fetch is enabled. It is cleared on vblank. Do not set this bit to 1 if Selective Fetch is not enabled.
13	**SF Continuous full frame** Access: R/W This bit will select for full frame fetches and updates continuously when Selective Fetch is enabled, until disabled by software. Do not set this bit to 1 if Selective Fetch is not enabled.
12:0	**SU Region End Address** Access: R/W This field indicates the ending line address of the selective update region.

PSR2_STATUS

PSR2_STATUS

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	60940h-60943h
Name:	PSR2 Status
ShortName:	PSR2_STATUS_A
Reset:	soft

DWord	Bit	Description
0	31:28	**PSR2 State** Access: RO This field indicates the live state of PSR2

Value	Name	Description
0000b	IDLE	Reset state
0001b	CAPTURE	Send capture frame
0010b	CPTURE_FS	Fast sleep after capture frame is sent
0011b	SLEEP	Selective Update
0100b	BUFON_FW	Turn Buffer on and Send Fast wake
0101b	ML_UP	Turn Main link up and send SR
0110b	SU_STANDBY	Selective update or Standby state
0111b	FAST_SLEEP	Send Fast sleep
1000b	DEEP_SLEEP	Enter Deep sleep
1001b	BUF_ON	Turn ON IO Buffer
1010b	TG_ON	Turn ON Timing Generator
1011b	BUFON_FW_2	Turn Buffer on and Send Fast wake for 3 Block case
Others	Reserved	Reserved

	27:26	**Link Status** Access: RO This field indicates the live status of the link.

Value	Name	Description
00b	Full Off	Link is fully off
01b	Full On	Link is fully on
11b	Reserved	Reserved

	25	**Reserved** Access: RO Format: MBZ

PSR2_STATUS

24:20 Max Sleep Time Counter

Access:	RO

This field provides the live status of the sleep time counter.

19:16 PSR2 Deep Sleep Entry Count

Access:	RO

The value in this register represents the number of times PSR2 Deep Sleep has been entered. The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.

15:12 Reserved

Access:	RO
Format:	MBZ

11:10 Reserved

Access:	RO
Format:	MBZ

9 PSR2 idle frame indication

Access:	RO

This bit gets set when DP link goes to sleep state and gets reset on PSR2 exit.

8 Sending TP2

Access:	RO

Description
This field indicates if TP2 is currently being sent.
Recommendation is to not use this status bit.

Value	Name	Description
0b	Not Sending	Not sending TP2
1b	Sending	Sending TP2

7:6 Reserved

Access:	RO
Format:	MBZ

5 PSR2 deep Sleep Entry Completion

Access:	R/WC

This is a sticky bit which is set on PSR2 deep sleep entry completion. Clear this bit by writing a 1b to it.

Value	Name
0b	Not complete

PSR2_STATUS

		1b: Complete
	4	**PSR2 SU Entry Completion** Access: R/WC This is a sticky bit which is set on PSR2 SU entry completion. Clear this bit by writing a 1b to it. 0b: Not complete 1b: Complete
	3:0	**Idle Frame Counter** Access: RO This field provides the live status of the idle frame counter.

PSR2_SU_STATUS

PSR2_SU_STATUS	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	96
Address:	60914h-6091Fh
Name:	PSR2 Selective Update Status
ShortName:	PSR2_SU_STATUS_A
Reset:	soft

A frame is divided into selective update blocks of four scan lines each. This register provides the count of the number of selective update blocks per frame, for the last eight frames

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:20	**Number of SU blocks in frame N - 2** Access: RO This field indicates the number of selective update blocks in frame N - 1.
	19:10	**Number of SU blocks in frame N - 1** Access: RO This field indicates the number of selective update blocks in frame N - 1.
	9:0	**Number of SU blocks in frame N** Access: RO This field indicates the number of selective update blocks in frame N.
1	31:30	**Reserved** Access: RO Format: MBZ
	29:20	**Number of SU blocks in frame N - 5** Access: RO This field indicates the number of selective update blocks in frame N - 1.
	19:10	**Number of SU blocks in frame N - 4** Access: RO This field indicates the number of selective update blocks in frame N - 1.

PSR2_SU_STATUS		
	9:0	**Number of SU blocks in frame N - 3** Access: RO This field indicates the number of selective update blocks in frame N.
2	31:20	**Reserved** Access: RO Format: MBZ
	19:10	**Number of SU blocks in frame N - 7** Access: RO This field indicates the number of selective update blocks in frame N - 1.
	9:0	**Number of SU blocks in frame N - 6** Access: RO This field indicates the number of selective update blocks in frame N.

PTE SW Fault Repair High

PTESWC_H - PTE SW Fault Repair High		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0CEF0h	
DWord	**Bit**	**Description**
0	31:0	**Repair Address High** Default Value: 00000000h Access: R/W Fixed PTE entry is written by SW here.

PTE SW Fault Repair Low

PTESWC_L - PTE SW Fault Repair Low		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0CEF4h	
DWord	**Bit**	**Description**
0	31:0	**Repair Address Low** Access: R/W Fixed PTE entry is written by SW here.

PWR_WELL_CTL

PWR_WELL_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45400h-45403h
Name:	Power Well Control 1
ShortName:	PWR_WELL_CTL1
Reset:	soft
CrashLogSaved:	true
CrashLogPriority:	2
CrashLogVisibility:	public
ExternalLongName:	DE Power Well Control 1
ExternalDescription:	Display engine power well control
Address:	45404h-45407h
Name:	Power Well Control 2
ShortName:	PWR_WELL_CTL2
Reset:	soft

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL1 is generally used for BIOS to control power.
PWR_WELL_CTL2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

Restriction
The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.
Power wells must be enabled and disabled following the display initialization and mode set sequences.

DWord	Bit	Description
0	31:22	**Reserved** Access: RO Format: MBZ
	21:18	**Reserved** Access: RO Format: MBZ

PWR_WELL_CTL

17	**Power Well D Request** Access: R/W This field requests power well to enable or disable. 0b: Disable 1b: Enable
16	**Power Well D State** Access: RO This field indicates the status of power well. 0b: Disabled 1b: Enabled
15	**Power Well C Request** Access: R/W This field requests power well to enable or disable. 0b: Disable 1b: Enable
14	**Power Well C State** Access: RO This field indicates the status of power well. 0b: Disabled 1b: Enabled
13	**Power Well B Request** Access: R/W This field requests power well to enable or disable. 0b: Disable 1b: Enable
12	**Power Well B State** Access: RO This field indicates the status of power well. 0b: Disabled 1b: Enabled

PWR_WELL_CTL

	11	**Power Well A Request** Access: R/W This field requests power well to enable or disable. 0b: Disable 1b: Enable
	10	**Power Well A State** Access: RO This field indicates the status of power well. 0b: Disabled 1b: Enabled
	9:4	**Reserved** Access: RO Format: MBZ
	3	**Power Well 2 Request** Access: R/W This field requests power well to enable or disable. 0b: Disable 1b: Enable
	2	**Power Well 2 State** Access: RO This field indicates the status of power well. 0b: Disabled 1b: Enabled
	1	**Power Well 1 Request** Access: R/W This field requests power well to enable or disable. 0b: Disable 1b: Enable
	0	**Power Well 1 State** Access: RO This field indicates the status of power well.

PWR_WELL_CTL			
		Value	Name
		0b	Disabled
		1b	Enabled

PWR_WELL_CTL_AUX

PWR_WELL_CTL_AUX

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45440h-45443h
Name:	Power Well Control AUX 1
ShortName:	PWR_WELL_CTL_AUX1
Reset:	soft
Address:	45444h-45447h
Name:	Power Well Control AUX 2
ShortName:	PWR_WELL_CTL_AUX2
Reset:	soft

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL_AUX1 is generally used for BIOS to control power.
PWR_WELL_CTL_AUX2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

Restriction

The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**Reserved** Access: RO Format: MBZ
	15	**AUX D IO Power Request** Access: R/W This field requests power for this Aux IO to enable or disable. Value: 0b — Name: Disable

PWR_WELL_CTL_AUX

	1b	Enable

14 AUX D IO Power State

Access:	RO

This field requests power for this Aux IO to enable or disable.

Value	Name
0b	Disabled
1b	Enabled

13:8 Reserved

Access:	RO
Format:	MBZ

7 USBC1 IO Power Request

Access:	R/W

This field requests power for this USBC Aux IO to enable or disable. This is used for typeC ports that are not in thunderbolt mode.

Value	Name
0b	Disable
1b	Enable

6 USBC1 IO Power State

Access:	RO

This field indicates the status of power for this USBC Aux IO.

Value	Name
0b	Disabled
1b	Enabled

5 AUX C IO Power Request

Access:	R/W

This field requests power for this Aux IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

4 AUX C IO Power State

Access:	RO

This field indicates the status of power for this Aux IO.

Value	Name
0b	Disabled
1b	Enabled

PWR_WELL_CTL_AUX

	3	**AUX B IO Power Request** Access: R/W This field requests power for this Aux IO to enable or disable. **Value** / **Name** 0b: Disable 1b: Enable
	2	**AUX B IO Power State** Access: RO This field requests power for this Aux IO to enable or disable. **Value** / **Name** 0b: Disabled 1b: Enabled
	1	**AUX A IO Power Request** Access: R/W This field requests power for this Aux IO to enable or disable. **Value** / **Name** 0b: Disable 1b: Enable
	0	**AUX A IO Power State** Access: RO This field indicates the status of power for this Aux IO. **Value** / **Name** 0b: Disabled 1b: Enabled

PWR_WELL_CTL_DDI

PWR_WELL_CTL_DDI	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45450h-45453h
Name:	Power Well Control DDI 1
ShortName:	PWR_WELL_CTL_DDI1
Reset:	soft
Address:	45454h-45457h
Name:	Power Well Control DDI 2
ShortName:	PWR_WELL_CTL_DDI2
Reset:	soft

This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power.
PWR_WELL_CTL _DDI1 is generally used for BIOS to control power.
PWR_WELL_CTL_DDI2 is generally used for driver to control power.
The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable.
When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes.
The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in.

Restriction
The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource.

DWord	Bit	Description
0	31:23	**Reserved** Access: RO Format: MBZ
	22:18	**Reserved** Access: RO Format: MBZ
	17:16	**Reserved** Access: RO Format: MBZ

PWR_WELL_CTL_DDI

15	**DDI D IO Power Request** Access: R/W This field requests power for DDI D IO to enable or disable. 0b: Disable 1b: Enable
14	**DDI D IO Power State** Access: RO This field indicates the status of power for DDI D IO. 0b: Disabled 1b: Enabled
13:8	**Reserved** Access: RO Format: MBZ
7	**USBC1 IO Power Request** Access: R/W This field requests power for USBC1 IO to enable or disable. 0b: Disable 1b: Enable
6	**USBC1 IO Power State** Access: RO This field indicates the status of power for USBC1 IO. 0b: Disabled 1b: Enabled
5	**DDI C IO Power Request** Access: R/W This field requests power for DDI C IO to enable or disable. 0b: Disable 1b: Enable
4	**DDI C IO Power State** Access: RO This field indicates the status of power for DDI C IO.

PWR_WELL_CTL_DDI

Value	Name
0b	Disabled
1b	Enabled

3 — DDI B IO Power Request

Access: R/W

This field requests power for DDI B IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

2 — DDI B IO Power State

Access: RO

This field indicates the status of power for DDI B IO.

Value	Name
0b	Disabled
1b	Enabled

1 — DDI A IO Power Request

Access: R/W

This field requests power for DDI A IO to enable or disable.

Value	Name
0b	Disable
1b	Enable

0 — DDI A IO Power State

Access: RO

This field indicates the status of power for DDI A IO.

Value	Name
0b	Disabled
1b	Enabled

PWRCTXSAVE Message Register for Boot Controller Unit

MSG_PWRCTXSAVE_MBC - PWRCTXSAVE Message Register for Boot Controller Unit

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0850Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
To **set** bit0, for example, the data would be 0x0001_0001.
To **clear** bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16.
Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:10	**Reserved** Access: RO Format: MBZ
	9	**Power Context Save Request** Access: R/W _Custom_GTIReset: BUS Power Context Save Request 1'b0: Power context save is not being requested (default). 1'b1: Power context save is being requested. Unit needs to self-clear this bit upon sampling.
	8:0	**QWord Credits for Power Context Save Request** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request. Minimum Credits = 1: Unit may send 1 QWord pair (enough for first LRI at least). Maximum Credits = 511: Unit may send 511 QWord pairs. A QWord pair is defined as a 32-bit register address and the corresponding 32-bitsof register data. Note that the LRI header and END commands are 64-bits each(32-bit command followed by 32-bit NOOP) and consume one QWord credit. Only valid with PWRCTXSAVE_REQ (Bit9).

RAWCLK_FREQ

RAWCLK_FREQ

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	C6204h-C6207h
Name:	Rawclk Frequency
ShortName:	RAWCLK_FREQ
Reset:	soft

38.4 MHz reference frequency: Integer 38 and fraction 2/5. Program Numerator=2, Denominator=4, Divider=37 decimal.

These fields are used to generate a divided down clock for miscellaneous timers in display.

DWord	Bit	Description
0	31	**Reserved** Access: R/W
	30	**Reserved** Access: RO Format: MBZ
	29:26	**Microsecond Counter Fraction Denominator** Access: R/W This field provides the denominator for the fractional part of the microsecond counter divider. Program this field to the denominator of the fractional portion of reference frequency minus one. If the fraction is 0, program to 0. Value / Name / Description: 0100b / 5 **[Default]** / Denominator 5 0000b / 0 / No fraction
	25:16	**Microsecond Counter Divider** Default Value: 0000100101b 38 MHz Access: R/W This field provides the integer part of the microsecond counter divider.
	15:14	**Reserved** Access: RO Format: MBZ
	13:11	**Microsecond Counter Fraction Numerator** Access: R/W This field provides the numerator for the fractional part of the microsecond counter divider. Program this field to the numerator of the fractional portion of reference frequency. If the fraction is 0, program to 0.

RAWCLK_FREQ

Value	Name	Description
000b	0	No fraction
001b	1	Numerator 1
010b	2 **[Default]**	Numerator 2

10:0 **Reserved**

Access:	RO
Format:	MBZ

Ray Tracing Control Register

RT_CTRL - Ray Tracing Control Register

Register Space:	MMIO: GTTMMADR
Size (in bits):	32
Address:	0E530h
Name:	RT_CTRL_ADDR
ShortName:	RT_CTRL_ADDR

Description
This register defines the functional and performance tuning related controls for Ray Tracing subsystem.

DWord	Bit	Description
0	31:16	**Reserved** Access: R/W Format: MBZ
	15:14	**Reserved** Access: R/W Format: MBZ
	13:12	**Memory Backed FIFO Fill Watermark** Access: R/W **Description** WaterMark for Filling from Memory onto local storage, once local storage occupancy reaches this value. Following is the encoding of the sizes 00 ==> 16; 01 ==> 24; 10 ==> 32; 11 : 48;
	11	**Reserved** Access: R/W
	10	**Disabling NULL query for Anyhit Shader** Access: R/W **Description** When this bit is SET, HW does not perform NULL address check for any hit shader before actually dispatching any hit shader. When HW performs the NULL check and finds that any hit shader is NULL, it trivially accepts the hit. When this bit is set, SW must ensure that callstack handler sends a TraceRay message with TraceRay_COMMIT for any hit shader invocation so that it matches with HW behavior of trivially accepting that hit. Value / Name: 0b: Off **[Default]** 1b: On

RT_CTRL - Ray Tracing Control Register

Programming Notes
This bit must be set i.e. Null Query must be disabled and therefore SW must ensure that callstack handler sends a TraceRay message with TraceRay_COMMIT for any hit shader invocation so that it matches with HW behavior of trivially accepting the hit.

9:7 **Compute guardband in terms of ULPs.**

Access:	R/W

Description
This field describes the multiplier in terms of ULPs for conservatism intersection test.
Conservative guardband = 7*ULP
Conservative guardband = 6*ULP
Conservative guardband = 5*ULP
Conservative guardband = 4*ULP
Conservative guardband = 3*ULP
Conservative guardband = 2*ULP
Conservative guardband = 1*ULP
Conservative guardband = 0*ULP

Value	Name
000b	7 **[Default]**
001b	6
010b	5
011b	4
100b	3
101b	2
110b	1
111b	0

6:5 **Controls the number of stackIDs for Ray Tracing subsystem.**

Access:	R/W

Description
This field allows controlling the number stackIDs (i.e. #unique rays in the Ray Tracing subsytem.
Number of stackIDs = 2048
Number of stackIDs = 1024
Number of stackIDs = 512

Value	Name

RT_CTRL - Ray Tracing Control Register

00b	2K **[Default]**
01b	1K
10b	512

Programming Notes
The number of StackID must >= (num_threads_in_tg * SIMD_size). Setting this field to a value less than the required value will result in a hang
For optimal performance, KMD must program this field to 01b i.e. 1024 StackIDs.

4 **Disables message compaction in RTF**

Access:	R/W

Description
When this bit is SET, messages are not compacted in RTFunit.

Value	Name
0b	Off **[Default]**
1b	On

3 **FIFO mode for RTF**

Access:	R/W

Description
When this bit is SET, the RTF will operate on the messages in true FIFO mode. If this bit is RESET, RTF will operate in LIFO mode to the downstream pipeline.

Value	Name
0b	Off **[Default]**
1b	On

2 **Bypass memory backed FIFO for SPAWN Messages**

Access:	R/W

Description
When this bit is SET, HW bypasses the memory backed FIFO for all incoming Spawn messages.

Value	Name
0b	Off **[Default]**
1b	On

RT_CTRL - Ray Tracing Control Register

	1	**Bypass memory backed FIFO for TraceRay(Sync)** Access: R/W **Description** When this bit is SET, HW bypasses the memory backed FIFO for all incoming TraceRay messages with RayQuery bit set. **Value** / **Name** 0b: Off **[Default]** 1b: On **Programming Notes** When this bit is set, it disabled the LIFO mode bug fix.
	0	**Bypass memory backed FIFO for TraceRay(Async)** Access: R/W **Description** When this bit is SET, HW bypasses the memory backed FIFO for all incoming TraceRay messages with RayQuery bit cleared (i.e. 0). **Value** / **Name** 0b: Off **[Default]** 1b: On

RC6 Context Base

RC6CTXBASE - RC6 Context Base		
Register Space:	MMIO: 0/2/0	
Size (in bits):	64	
Address:	00D48h	
RC6 Location		
DWord	**Bit**	**Description**
0	31:12	**RC6 Memory Base Low** Access: R/W Lock _Custom_GTIReset: BUS This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1
	11:1	**Reserved** Access: RO Format: MBZ
	0	**RC6Context Base Register Lock** Access: R/W Lock _Custom_GTIReset: BUS 1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only BIOS must set this bit to prevent further changes
1	31:0	**RC6 Memory Base High** Access: R/W Lock _Custom_GTIReset: BUS This field is used to set the base of memory where the RC6 power context will be saved. This value MUST be above the base and below the top of stolen memory. This High Dword must be written before the low word is written with RC6MEMLOCK of 1. This register is locked (becomes read-only) when RC6MEMLOCK is 1

RC6 Context Base Register 1

GPMRC6CTXBASE1 - RC6 Context Base Register 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	08674h	
DWord	**Bit**	**Description**
0	31:0	**RC6 Memory Base High** Access: R/W Lock _Custom_GTIReset: BUS This field corresponds to bits [63:32] of RC6MEMBASE This register is locked (becomes read-only) when RC6MEMLOCK is 1

RC6 LOCATION

RC6LOCATION - RC6 LOCATION

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00D40h

RC6 Location

DWord	Bit	Description
0	31	**RC6Context Location Lock** Access: R/W Lock _Custom_GTIReset: BUS 1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only
	30:1	**Reserved** Access: RO Format: MBZ
	0	**RC6Context Location** Access: RO _Custom_GTIReset: BUS 1'b1 : Send context data to DRAM location specified in RC6MEMBASE (default) This will be tied to 1 with as there is no option to save context to a SRAM

Register_HCPBitstreamOutputCABACInsertionCount

HCP_CABAC_INSERTION_COUNT - Register_HCPBitstreamOutputCABACInsertionCount

Register Space:	MMIO: GTTMMADR
Source:	VideoCS1
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	BUS

This register stores the count in bytes of **CABAC ZERO_WORD insertion. It is primarily provided for statistical data gathering.**

DWord	Bit	Description
0	31:0	**HCP Cabac Insertion Count** Access: RO Format: U32 Total number of bytes in the bitstream output before for the CABAC zero word insertion. This count is updated each time when the insertion count is incremented.

Register_HCPSFCLOCKRequest

HCP_SFC_LOCK_REQUEST - Register_HCPSFCLOCKRequest

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1C2910h
ShortName:	HCP_SFC_LOCK_REQUEST_VCS0
Description:	For VDBox0
Address:	1C6910h
ShortName:	HCP_SFC_LOCK_REQUEST_VCS1
Description:	For VDBox1
Address:	1D2910h
ShortName:	HCP_SFC_LOCK_REQUEST_VCS2
Description:	For VDBox2
Address:	1D6910h
ShortName:	HCP_SFC_LOCK_REQUEST_VCS3
Description:	For VDBox3
Address:	1E2910h
ShortName:	HCP_SFC_LOCK_REQUEST_VCS4
Description:	For VDBox4
Address:	1E6910h
ShortName:	HCP_SFC_LOCK_REQUEST_VCS5
Description:	For VDBox5
Address:	1F2910h
ShortName:	HCP_SFC_LOCK_REQUEST_VCS6
Description:	For VDBox6
Address:	1F6910h
ShortName:	HCP_SFC_LOCK_REQUEST_VCS7
Description:	For VDBox7

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**HCP_SFC_Forced_Lock** Access: R/W Format: U1

HCP_SFC_LOCK_REQUEST - Register_HCPSFCLOCKRequest		
		This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells HCP that a software reset is going to happen. HCP then issues a forced lock to SFC. If SFC is currently locked to HCP, SFC should not unlock itself from HCP. If SFC is NOT currently locked to HCP, SFC should not accept the lock request from HCP. Driver needs to clear this bit after the software reset sequence is complete.

Register_HCPSFCLOCKStatus

HCP_SFC_LOCK_STATUS - Register_HCPSFCLOCKStatus	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1C2914h
ShortName:	HCP_SFC_LOCK_STATUS_VCS0
Description:	For VDbox0
Address:	1C6914h
ShortName:	HCP_SFC_LOCK_STATUS_VCS1
Description:	For VDbox1
Address:	1D2914h
ShortName:	HCP_SFC_LOCK_STATUS_VCS2
Description:	For VDBox2
Address:	1D6914h
ShortName:	HCP_SFC_LOCK_STATUS_VCS3
Description:	For VDBox3
Address:	1E2914h
ShortName:	HCP_SFC_LOCK_STATUS_VCS4
Description:	For VDBox4
Address:	1E6914h
ShortName:	HCP_SFC_LOCK_STATUS_VCS5
Description:	For VDBox5
Address:	1F2914h
ShortName:	HCP_SFC_LOCK_STATUS_VCS6
Description:	For VDBox6
Address:	1F6914h
ShortName:	HCP_SFC_LOCK_STATUS_VCS7
Description:	For VDBox7

DWord	Bit	Description
0	31:2	**Reserved** Access: RO Format: MBZ
	1	**HCP_SFC_Forced_Act** Access: RO Format: U1

HCP_SFC_LOCK_STATUS - Register_HCPSFCLOCKStatus

		This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that HCP has received HCP_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert HCP_SFC_Forced_Lock as well.
	0	**HCP_SFC_Usage** Access: RO Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to HCP. This bit should be set after SFC accepts the lock request from HCP. This bit should be clear once SFC finishes the workload and unlocked from HCP. In case a reset happens on HCP, this bit must be reset once a new workload is received

Register_MESHPrimitiveCounter

MESH_PRIMITIVE_COUNT - Register_MESHPrimitiveCounter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

Address:	026D8h
Name:	MESH Primitive Counter
ShortName:	MESH_PRIMITIVE_COUNT

The **MESH_PRIMITIVE_COUNT** accumulates API-level MeshShader Primitive created by the pipeline. For each MeshShader ThreadGroup, this register is incremented by the number of primitives created.
SW shall comprehend that a pipeline flush is required to ensure that preceding MeshShader work is included in the register value.

DWord	Bit	Description
0	63:32	**MESH Primitive Count UDW** Access: R/W Number of primitives created by the MESH stage. Updated only when MESH Enable and MESH Statistics Enable are set in 3DSTATE_MESH
	31:0	**MESH Primitive Count LDW** Access: R/W Number of primitives created by the MESH stage. Updated only when MESH Enable and MESH Statistics Enable are set in 3DSTATE_MESH

Register_MESHPrimitiveCounterperSlice

MESH_PRIMITIVE_COUNT_SLICE - Register_MESHPrimitiveCounterperSlice

Register Space:	MMIO: GTTMMADR
Access:	R/W
Size (in bits):	64
_Custom_GTIAccessProtection:	IA
_Custom_GTIReset:	DEV
_Custom_GTIStorage:	FLOP

The **MESH_PRIMITIVE_COUNT** accumulates API-levelMeshShader Primitive created by the pipeline. For each MeshShader ThreadGroup, this register is incremented by the number of primitives created.
SW shall comprehend that a pipeline flush is required to ensure that preceding MeshShader work is included in the register value.

DWord	Bit	Description
0..1	63:32	**MESH Primitive Count UDW in Slice** Access: R/W Number of primitives created by the MESH stage within the slice. Updated only when MESH Enable and MESH Statistics Enable are set in 3DSTATE_MESH
	31:0	**MESH Primitive Count LDW in Slice** Access: R/W Number of primitive created by the MESH stage within the slice. Updated only when MESH Enable and MESH Statistics Enable are set in 3DSTATE_MESH

Register_OAG Aggregate Perf Counter A36UpperDWord

OAG_OAPERF_A36_UPPER - Register_OAG Aggregate Perf Counter A36UpperDWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB24h

This register reflects the count value of the OA Performance counter A36 Upper Dword.
More details about the precise event counted by this register are located in **Statistics Gathering.**

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Register_OAG Aggregate Perf Counter A37UpperDword

OAG_OAPERF_A37_UPPER - Register_OAG Aggregate Perf Counter A37UpperDword

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0DB2Ch

This register reflects the count value of the OA Performance counter A37 Upper Dword.
More details about the precise event counted by this register are located **Statistics Gathering.**

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Register_OAM Aggregate Perf Counter A36 Upper DWord

OAM_OAPERF_A36_UPPER - Register_OAM Aggregate Perf Counter A36 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	130C8h-130CBh
Name:	Aggregate Perf Counter 36 Upper DWord
ShortName:	AGG_PERF_COUNTER_A36_UPPER_MEDIA_SLICE_0_OA
Address:	132C8h-132CBh
Name:	Aggregate Perf Counter 36 Upper DWord
ShortName:	AGG_PERF_COUNTER_A36_UPPER_MEDIA_SLICE_1_OA
Address:	134C8h-134CBh
Name:	Aggregate Perf Counter 36 Upper DWord
ShortName:	AGG_PERF_COUNTER_A36_UPPER_MEDIA_SLICE_2_OA
Address:	136C8h-136CBh
Name:	Aggregate Perf Counter 36 Upper DWord
ShortName:	AGG_PERF_COUNTER_A36_UPPER_MEDIA_SLICE_3_OA

This register reflects the count value of the OA Performance counter A36 Upper DWord.
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Register_OAM Aggregate Perf Counter A37 Upper DWord

OAM_OAPERF_A37_UPPER - Register_OAM Aggregate Perf Counter A37 Upper DWord

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	130D0h-130D3h
Name:	Aggregate Perf Counter 37 Upper DWord
ShortName:	AGG_PERF_COUNTER_A37_UPPER_MEDIA_SLICE_0_OA

Address:	132D0h-132D3h
Name:	Aggregate Perf Counter 37 Upper DWord
ShortName:	AGG_PERF_COUNTER_A37_UPPER_MEDIA_SLICE_1_OA

Address:	134D0h-134D3h
Name:	Aggregate Perf Counter 37 Upper DWord
ShortName:	AGG_PERF_COUNTER_A37_UPPER_MEDIA_SLICE_2_OA

Address:	136D0h-136D3h
Name:	Aggregate Perf Counter 37 Upper DWord
ShortName:	AGG_PERF_COUNTER_A37_UPPER_MEDIA_SLICE_3_OA

This register reflects the count value of the OA Performance counter A37 Upper DWord.
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Upper Value** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 63:32 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Register_OAR Aggregate Perf Counter A35

OAR_OAPERF_A35 - Register_OAR Aggregate Perf Counter A35

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	029B8h

This register reflects the count value of the OA Performance counter A35

DWord	Bit	Description
0	31:0	**Considerations** Access: R/W Format: U32 _Custom_GTIReset: DEV This 32-bit field returns bits 31:0 of the live performance counter value when read. Note that there is no "latch and hold" mechanism for performance counters when they are accessed through MMIO, so the value returned from this register may be different on back-to-back reads.

Remote2Root FLR Ack

REM2RTFLRACK - Remote2Root FLR Ack

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	10180Ch

For a multi-tile configuration, this register will be used by hardware. The remote tile hardware will write the appropriate byte in the root tile to "ack" FLR request/prep completion.
This register is for hardware communication purposes only. This register is not intended to be used by software.

DWord	Bit	Description
0	31:26	**Reserved** Access: RO Format: MBZ
	25	**Reserved** Access: RO Format: MBZ
	24	**REM3ACK** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Remote tile 3 writes this bit to "ack" FLR has completed. 0 : No remote tile 3 "ack" 1 : Remote tile 3 has "ack'ed" FLR flow Root tile hardware will clear this register
	23:18	**Reserved** Access: RO Format: MBZ
	17	**Reserved** Access: RO Format: MBZ
	16	**REM2ACK** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Remote tile 2 writes this bit to "ack" FLR request has completed. 0 : No remote tile 2 "ack" 1 : Remote tile 2 has "ack'ed" FLR flow Root tile hardware will clear this register

REM2RTFLRACK - Remote2Root FLR Ack

	15:10	**Reserved** Access: RO Format: MBZ
	9	**Reserved** Access: RO Format: MBZ
	8	**REM1ACK** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Remote tile 1 writes this bit to "ack" FLR request has completed. 0 : No remote tile 1 "ack" 1 : Remote tile 1 has "ack'ed" FLR flow Root tile hardware will clear this register
	7:1	**SPARE0** Default Value: 00h Access: RO _Custom_GTIReset: BUS Reserved
	0	**Reserved** Access: RO Format: MBZ

Render and Media Context Restore Needed

RENDER_MEDIA_NEED_RESTORE - Render and Media Context Restore Needed		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	080F0h	
DWord	**Bit**	**Description**
0	31:2	**Reserved** Access: RO
	1	**Render Context Restore is needed** Access: RO _Custom_GTIReset: BUS Render Context Restore Needed Flag to support Render Powergating Feature This flag will let PM know if Media context need to be restored on C6 exit 1'b0: Do not proceed if Wait for VCR1 is set (default). 1'b1: Proceed to unblocking FIFO.
	0	**Media Context Restore is needed** Access: RO _Custom_GTIReset: BUS Render Context Restore Needed Flag to support Render Powergating Feature This flag will let PM know if Media context need to be restored on C6 exit 1'b0: Do not proceed if Wait for VCR1 is set (default). 1'b1: Proceed to unblocking FIFO.

Render Control Unit Mode Register

RCU_MODE - Render Control Unit Mode Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	14800h

Mode register for Render Control Unit (RCU).

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:5	**Reserved** Access: R/W Format: PBC
	4:3	**Reserved** Access: R/W Format: PBC
	2	**Reserved** Access: R/W Format: PBC
	1	**Compute Engine Dispatch Mode** Access: R/W This field is only valid when Compute Engine is enabled i.e. bit[0] of this register is set otherwise ignored. This bit selects the how each of all the ComputeCS fill the various compute slices. RenderCS will always run (dispatch threads) on all the compute slices.

Value	Name	Description
0	Load Balance Slice CCS Mode **[Default]**	When only one ComputeCS is active, it will run on all compute slices. When more than one ComputeCS is active, the compute slices are dynamically assigned to each of the ComputeCS, so that each ComputeCS is running simultaneously.

Programming Notes
CCS_MODE register must be programmed with the required slice allocation to ComputeCS's prior to programming the Compute Engine Dispatch Mode to "Fixed Slice CCS Mode".

RCU_MODE - Render Control Unit Mode Register

Restriction
When in Load Balance Slice CCSMode, if any slice is disabled in the configuration, the ComputeCS with the same ID cannot be used. For example, CCS2 cannot be used if slice 2 is disabled. When in Fixed Slice CCS Mode, the CCS_MODE register is programmed with the specific ComputeCS ID that are enabled.

0 **Compute Engine Enable**

Access:	R/W

Description
This bit indicates if Compute Engine (a.k.a Dual Context or Multi Context) is enabled or not. This bit must be treated as global primary control for enabling and disabling of compute engine. Hardware allocates required resources for the compute engine based on this bit. • Mid Thread Preemption for GPGPU workloads is not supported when compute engine is enabled. Hardware implicitly demotes the GPGPU preemption granularity to Thread Group or lower irrespective of the preemption granularity programmed through GPGPU_PREEMPTION_CONTROL mode bits.
Compute Engine Enable in GT4 mode of operation indicates availability of the compute engines for executing compute contexts. "Compute Engine Dispatch Mode" (bit 1 of this register) and CCS_MODE indicates which contexts can be deployed to various Compute Engines.

Value	Name	Description
0	**[Default]**	Compute engine is disabled.
1		Compute engine is enabled.

Programming Notes
This bit must be programmed when render engine is idle with no contexts getting executed.

Render Control Unit Power Clock State Register

RCU_PWR_CLK_STATE - Render Control Unit Power Clock State Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	148C8h

This register provides a mechanism to override the PWR_CLK_STATE requested by the RenderCS or ComputeCS.Both ComputeCS and RenderCS make their R_PWR_CLK_STATE request to Render Control Unit (RCU), RCU computes the required PWR_CLK_STATE and interfaces with power management to get the desired state.

DWord	Bit	Description
0	31	**Power Clock State Enable** Access: R/W Format: U1 When enabled (set) RCU will force the PWR_CLK_STATE programmed in the RCU_PWR_CLK_STATE to Power Management instead of the PWR_CLK_STATE received from the RenderCS or ComputeCS. RCU will enforce the updated value of RCU_PWR_CLK_STATE on an engines PWR_CLK_STATE request when the requesting engine is the only active engine in the GPU, i.e. RCU will ensure the other engines are not active and are not impacted on changing the PWR_CLK_STATE. (Example: Updated value in RCU_PWR_CLK_STATE will be used to override the RenderCS PWR_CLK_STATE request when ComputeCS is idle or Vice-Versa).

Value	Name	Description
0h	Power Clock State Disabled	No specific power state set, bits[30:0] are ignored.
1h	Power Clock State Enabled	Power state is set and bit[30:0] are valid and have the desired state. RCU will use the powe state to overide the values recevied from RenderCS or ComputeCS.

DWord	Bit	Description
	30:0	**Render Power Clock State** Access: R/W Format: U31

RenderCS to LTISEQ Range Based Flush DW1

RCS_LTI_RANGE_FLSH_DW1 - RenderCS to LTISEQ Range Based Flush DW1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B4B4h

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:28	**L3 Flush Eviction Policy** Access: R/W This field describes the flush eviction policy for the address ranges being flushed

Value	Name	Description
0h	Flush L3 with eviction - INV **[Default]**	All modified content written to memory and L3 state is invalid
1h	Flush L3 with eviction - VLD	All modified content written to memory and L3 state is kept valid (shared state)
2h	Discard	All modified content is discarded (no write out to memory) and L3 state is invalid

DWord	Bit	Description
	27:23	**Engine ID** Access: R/W Indicates the engine which has generated the Range Based Address Flush to L3 cache.

Value	Name
0h	GFX (Render Engine)
1h	VDBox0
2h	VDBox1
3h	VEBox0
4h	Blitter
9h	VDBox2
Ah	VDBox3
Bh	VEBox1
Ch	ComputeCS0
Dh	ComputeCS1
Eh	ComputeCS2

RCS_LTI_RANGE_FLSH_DW1 - RenderCS to LTISEQ Range Based Flush DW1

		Fh: ComputeCS3 11h: VDBox4 12h: VDBox5 13h: VEBox2 19h: VDBox6 1Ah: VDBox7 1Bh: VEBox3 Others: Reserved
	22:16	**Reserved** Access: RO Format: MBZ
	15:0	**Address High** Access: R/W Format: GraphicsAddress[47:32] This filed describes the starting address page of the address ranges to be flushed by L3$. This is hardware internal generated message for communication between the units within GT to handle “Address Based Range Flush” for L3$ as a result of executing L3_CONTROL command.

Reported BitRateControl Convergence Status

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1C928h
ShortName:	MFX_VP8_BRC_CONVERGENCE_STATUS_VD2

This register stores BitRateControl Convergence Status.

DWord	Bit	Description
0	31	**Reserved** Access: R/W
	30:28	**Reserved** Access: R/W
	27	**Reserved** Access: R/W
	26:24	**Reserved** Access: R/W
	23	**Reserved** Access: R/W
	22:20	**Reserved** Access: R/W
	19	**Reserved** Access: R/W
	18:16	**Reserved** Access: R/W
	15:12	**Reserved** Access: RO Format: MBZ
	11:8	**Total Num of Pass** Access: R/W Format: U4 This bit indicates the number of Multipass including current frame. Note that Initial Pass is not counted.

MFX_VP8_BRC_CONVERGENCE_STATUS - Reported BitRateControl Convergence Status

	7:2	**Reserved** Access: RO Format: MBZ
	1	**Overflow OR Underflow Flag** Access: R/W Format: U1 This bit indicates the current frame has BRC overflow OR underflow.
	0	**MB Max. Conformance Flag** Access: R/W Format: U1 This contains flag that indicate Inter MB or Intra MB Max. Conformance is not met. This is legacy support and this feature is not validated.

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1C920h

This register stores per segment Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:24	**Segment1 CumulativeDeltaLoopFilter** Access: R/W Format: S6 This contains Segment1 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment1 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23:22	**Reserved** Access: RO Format: MBZ
	21:16	**Segment1 LoopFilter** Access: R/W Format: U6 This contains Segment1 LoopFilter used in current frame. This register is valid after a BRC pass is done.
	15	**Reserved** Access: RO Format: MBZ
	14:8	**Segment0 CumulativeDeltaLoopFilter** Access: R/W Format: S6 This contains Segment0 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaLoopFilter.

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER01 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 01

	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**Segment0 LoopFilter** Access: R/W Format: U6 This contains Segment0 LoopFilter used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects LoopFilter. If Segmentation is enabled, this field reflects Segment0 LoopFilter.

Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1C924h

This register stores per segment Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:24	**Segment3 CumulativeDeltaLoopFilter** Access: R/W Format: S6 This contains Segment3 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23:22	**Reserved** Access: RO Format: MBZ
	21:16	**Segment3 LoopFilter** Access: R/W Format: U6 This contains Segment3 LoopFilter used in current frame. This register is valid after a BRC pass is done.
	15	**Reserved** Access: RO Format: MBZ
	14:8	**Segment2 CumulativeDeltaLoopFilter** Access: R/W Format: S6 This contains Segment2 CumulativeDeltaLoopFilter in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.

MFX_VP8_BRC_CUMULATIVE_D_LOOP_FILTER23 - Reported BitRateControl CumulativeDeltaLoopFilter and LoopFilter 23

	7:6	**Reserved** Access: RO Format: MBZ
	5:0	**Segment2 LoopFilter** Access: R/W Format: U6 This contains Segment2 LoopFilter used in current frame. This register is valid after a BRC pass is done.

Reported BitRateControl CumulativeDeltaQindex and Qindex 01

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01 - Reported BitRateControl CumulativeDeltaQindex and Qindex 01

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	12918h
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01_VB0
Address:	1C918h
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01_VB1

This register stores per segment Bit Rate Control CumulativeDeltaQindex.

DWord	Bit	Description
0	31:24	**Segment1 CumulativeDeltaQindex** Access: R/W Format: S7 This contains Segment1 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment1 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23	**Reserved** Access: RO Format: MBZ
	22:16	**Segment1 Qindex** Access: R/W Format: U7 This contains Segment1 Qindex used in current frame. This register is valid after a BRC pass is done.
	15:8	**Segment0 CumulativeDeltaQindex** Access: R/W Format: S7 This contains Segment0 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment0 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects CumulativeDeltaQindex. If Segmentation is enabled, this field reflects Segment0 CumulativeDeltaQindex.
	7	**Reserved** Access: RO Format: MBZ

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX01 - Reported BitRateControl CumulativeDeltaQindex and Qindex 01		
	6:0	**Segment0 Qindex** Access: R/W Format: U7 This contains Segment0 Qindex used in current frame. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects Qindex. If Segmentation is enabled, this field reflects Segment0 Qindex.

Reported BitRateControl CumulativeDeltaQindex and Qindex 23

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23 - Reported BitRateControl CumulativeDeltaQindex and Qindex 23

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1291Ch
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23_VB0
Address:	1C91Ch
ShortName:	MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23_VB1

This register stores per segment Bit Rate Control CumulativeDeltaQindex and Qindex.

DWord	Bit	Description
0	31:24	**Segment3 CumulativeDeltaQindex** Access: R/W Format: S7 This contains Segment3 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment3 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	23	**Reserved** Access: RO Format: MBZ
	22:16	**Segment3 Qindex** Access: R/W Format: U7 This contains Segment3 Qindex used in current frame. This register is valid after a BRC pass is done.
	15:8	**Segment2 CumulativeDeltaQindex** Access: R/W Format: S7 This contains Segment2 CumulativeDeltaQindex in Bit Rate Control. It accumulates all Segment2 DeltaQindices per pass in Multipass. This register is valid after a BRC pass is done.
	7	**Reserved** Access: RO Format: MBZ

MFX_VP8_BRC_CUMULATIVE_DQ_INDEX23 - Reported BitRateControl CumulativeDeltaQindex and Qindex 23		
	6:0	**Segment2 Qindex** Access: R/W Format: U7 This contains Segment2 Qindex used in current frame. This register is valid after a BRC pass is done.

Reported BitRateControl DeltaLoopFilter

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	12914h
ShortName:	MFX_VP8_BRC_D_LOOP_FILTER_VB0
Address:	1C914h
ShortName:	MFX_VP8_BRC_D_LOOP_FILTER_VB1

This register stores per segment Bit Rate Control DeltaLoopFilter.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:24	**Segment3 DeltaLoopFilter** Access: RO Format: S6 This contains Segment3 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done
	23	**Reserved** Access: RO Format: MBZ
	22:16	**Segment2 DeltaLoopFilter** Access: RO Format: S6 This contains Segment2 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done
	15	**Reserved** Access: RO Format: MBZ
	14:8	**Segment1 DeltaLoopFilter** Access: RO Format: S6 This contains Segment1 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done.

MFX_VP8_BRC_D_LOOP_FILTER - Reported BitRateControl DeltaLoopFilter

	7	**Reserved** Access: RO Format: MBZ
	6:0	**Segment0 DeltaLoopFilter** Access: RO Format: S6 This contains Segment0 DeltaLoopFilter in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaLoopFilter. If Segmentation is enabled, this field reflects Segment0 DeltaLoopFilter.

Reported BitRateControl DeltaQindex

MFX_VP8_BRC_DQ_INDEX - Reported BitRateControl DeltaQindex

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	12910h
ShortName:	MFX_VP8_BRC_DQ_INDEX_VB0
Address:	1C910h
ShortName:	MFX_VP8_BRC_DQ_INDEX_VB1

This register stores per segment Bit Rate Control DeltaQindex.

DWord	Bit	Description
0	31:24	**Segment3 DeltaQindex** Access: RO Format: S7 This contains Segment3 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done
	23:16	**Segment2 DeltaQindex** Access: RO Format: S7 This contains Segment2 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done
	15:8	**Segment1 DeltaQindex** Access: RO Format: S7 This contains Segment1 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done.
	7:0	**Segment0 DeltaQindex** Access: RO Format: S7 This contains Segment0 DeltaQindex in Bit Rate Control. This register is valid after a BRC pass is done. If Segmentation is not enabled, this field reflects DeltaQindex. If Segmentation is enabled, this field reflects Segment0 DeltaQindex.

Reported BitRateControl parameter Mask

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	12900h
ShortName:	MFX_VP8_CNTRL_MASK_VB0
Address:	1C900h
ShortName:	MFX_VP8_CNTRL_MASK_VB1

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:6	**Reserved** Access: RO Format: MBZ
	5	**Final Bitstream Buffer Overrun Mask** Access: RO Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit5. This denotes Final bitstream buffer overrun feature is enabled.
	4	**Intermediate Bitstream Buffer Overrun Mask** Access: RO Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit4. This denotes intermediate bitstream buffer overrun feature is enabled.
	3	**Intra MB Bit Count Conformance Mask** Access: RO Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit3. This feature is not validated.
	2	**Inter MB Bit Count Conformance Mask** Access: RO Format: U1 This is legacy support as AVC for Inter MB Bit Count conformance. This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit2. This feature is not validated.

MFX_VP8_CNTRL_MASK - Reported BitRateControl parameter Mask

	1	**Frame Bit Rate Overflow Mask** Access: RO Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit0. It denotes if Frame Bit Rate Overflow is enabled for Bit Rate Control
	0	**Frame Bit Rate Underflow Mask** Access: RO Format: U1 This is same bit reflected in MFX_VP8_ENC_CFG DW2 bit1. It denotes if Frame Bit Rate Underflow is enabled for Bit Rate Control

Reported BitRateControl parameter Status

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	12904h
ShortName:	MFX_VP8_CNTRL_STATUS_VB0
Address:	1C904h
ShortName:	MFX_VP8_CNTRL_STATUS_VB1

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**QindexClampHigh Status** Access: RO Format: U1 This denotes if Qindex is clamped by QindexClampHigh value programmed in MFX_VP8_PIC_STATE.DW7.
	6	**QindexClampLow Status** Access: RO Format: U1 This denotes if Qindex is clamped by QindexClampLow value programmed in MFX_VP8_PIC_STATE.DW7.
	5	**Final Bitstream Buffer Overrun Status** Access: RO Format: U1 This denotes if Final bitstream buffer overrun.
	4	**Intermediate Bitstream Buffer Overrun Status** Access: RO Format: U1 This denotes if any of the Intermediate bitstream buffer overrun. (including FrameHeader, Partition1 to Partition8)

MFX_VP8_CNTRL_STATUS - Reported BitRateControl parameter Status

	3	**Intra MB Bit Count Conformance Status** Access: RO Format: U1 This is legacy support as AVC for Intra MB Bit Count conformance. It denotes if Intra MB Bit Count meets conformance size. This feature is not validated.
	2	**Inter MB Bit Count Conformance Status** Access: RO Format: U1 This is legacy support as AVC for Inter MB Bit Count conformance. It denotes if Inter MB Bit Count meets conformance size. This feature is not validated.
	1	**Frame Bit Rate Overflow Status** Access: RO Format: U1 It denotes if Frame Bit Rate Overflow in current frame
	0	**Frame Bit Rate Underflow Status** Access: RO Format: U1 It denotes if Frame Bit Rate Underflow in current frame

Reported Bitstream Output Bit Count for Syntax Elements Only

HCP_BITSTREAMSE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1E9A8h

This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**HCP Bitstream Syntax Element Only Bit Count** Access: RO Format: U32 Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Bit Count for Syntax Elements Only Register

MFC_BITSTREAM_SE_BITCOUNT_FRAME - Reported Bitstream Output Bit Count for Syntax Elements Only Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	128A4h

This register stores the count of number of bits in the bitstream due to syntax elements only. This excludes header/ byte alignment /tail/EMU/CABAC-0word/padding bits but includes the stop-one-bit. This register is part of the context save and restore.

DWord	Bit	Description
0	31:0	**MFC Bitstream Syntax Element Only Bit Count** Access: RO Total number of bits in the bitstream output due to syntax elements only. It includes the data bytes only. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Byte Count per Frame Register

MFC_BITSTREAM_BYTECOUNT_FRAME - Reported Bitstream Output Byte Count per Frame Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	128A0h	
This register stores the count of bytes of the bitstream output per frame		
DWord	**Bit**	**Description**
0	31:0	**MFC Bitstream Byte Count per Frame** Access: RO Total number of bytes in the bitstream output per frame from the encoder. This includes header/tail/byte alignment/data bytes/EMU (emulation) bytes/cabac-zero word insertion/padding insertion. This count is updated for every time the internal bitstream counter is incremented and its reset at image start.

Reported Bitstream Output Byte Count per Tile

HCP_BITSTREAM_BYTECOUNT_TILE - Reported Bitstream Output Byte Count per Tile

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1E9CCh

This register stores the count of bytes of the bitstream output per tile.

DWord	Bit	Description
0	31:0	**HCP Bitstream Byte Count per Tile** Access: RO Format: U32 Total number of bytes in the bitstream output per Tile from the encoder. This includes header/byte alignment/data bytes/EMU (emulation) bytes/. This count is updated for every time the internal bitstream counter is incremented and it's reset at tile start.

Reported Bitstream Output CABAC Bin Count Register

MFC_AVC_CABAC_BIN_COUNT_FRAME - Reported Bitstream Output CABAC Bin Count Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	128A8h

This register stores the count of number of bins per frame.

DWord	Bit	Description
0	31:0	**MFC AVC Cabac Bin Count** Access: RO Total number of BINs in the bitstream output per frame from the encoder. This count is updated for every time the bin counter is incremented and its reset at image start.

Reported Final Bitstream Byte Count

MFX_VP8_FRM_BYTE_CNT - Reported Final Bitstream Byte Count	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	12908h
ShortName:	MFX_VP8_FRM_BYTE_CNT_01
Address:	1C908h
ShortName:	MFX_VP8_FRM_BYTE_CNT_02

This register stores the count of bytes of the bitstream output per frame

DWord	Bit	Description
0	31:0	**Final BitStream Byte Count** Access: RO Format: U32 This register contains Final Bitstream byte count

Reported Frame Zero Padding Byte Count

MFX_VP8_FRM_ZERO_PAD - Reported Frame Zero Padding Byte Count

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1290Ch
ShortName:	MFX_VP8_FRM_ZERO_PAD_VB0
Address:	1C90Ch
ShortName:	MFX_VP8_FRM_ZERO_PAD_VB1

This register stores Frame Zero Padding Byte Count

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Frame Zero Padding Byte Count** Access: RO Format: U16 This register contains Frame Zero Padding byte count This is legacy support. This feature is not validated.

Reported Timestamp Count

TIMESTAMP - Reported Timestamp Count	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02358h-0235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_RCSUNIT
Address:	22358h-2235Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_BCSUNIT
Address:	1C0358h-1C035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT0
Address:	1C4358h-1C435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT1
Address:	1C8358h-1C835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT0
Address:	1D0358h-1D035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT2
Address:	1D4358h-1D435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT3
Address:	1D8358h-1D835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT1
Address:	1E0358h-1E035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT4
Address:	1E4358h-1E435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT5

TIMESTAMP - Reported Timestamp Count

Address:	1E8358h-1E835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT2

Address:	1F0358h-1F035Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT6

Address:	1F4358h-1F435Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VCSUNIT7

Address:	1F8358h-1F835Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_VECSUNIT3

Address:	1A358h-1A35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_CCSUNIT0

Address:	1C358h-1C35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_CCSUNIT1

Address:	1E358h-1E35Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_CCSUNIT2

Address:	26358h-2635Fh
Name:	Reported Timestamp Count
ShortName:	TIMESTAMP_CCSUNIT3

This register provides an elapsed real-time value that can be used as a timestamp for GPU events over short periods of time. Note that the value of this register can be obtained in a 3D pipeline-synchronous fashion without a pipeline flush by using the PIPE_CONTROL command. See 3D Geometry Pipeline in the "3D and Media" volume. This register (effectively) counts at a constant frequency by adjusting the increment amount according to the actual reference clock frequency. SW therefore does not need to know the reference clock frequency.

This register provides an elapsed real-time value that can be used as a timestamp. The accumulated value in this register is of the timestamp stamp granularity (base unit) defined in the Time Stamp Bases subsection in Power Management chapter.

This register is *not* reset by a graphics reset. It will maintain its value unless a full chipset reset is performed.

DWord	Bit	Description	
0..1	63:36	**Reserved**	
		Access:	RO

TIMESTAMP - Reported Timestamp Count		
		Format: MBZ
	35:32	**Timestamp Value UN** Access: R/W Format: U4 This register increments for every timestamp base unit. The granularity of the time stamp base unit is defined in the Time Stamp Bases subsection in Power Management chapter. Note: This is the Upper Nibble of the Timesamp Value, a 36-bit signal.
	31:0	**Timestamp Value LDW** Access: R/W Format: U32 This register increments for every timestamp base unit. The granularity of the time stamp base unit is defined in the Time Stamp Bases subsection in Power Management chapter.

Report Queue CFG HI

RPTQCFGHI - Report Queue CFG HI		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	098ACh	
Config to MCI and DFT Ring		
DWord	**Bit**	**Description**
0	31	**Report fifo cfg hi valid** Access: RO _Custom_GTIReset: BUS
	30:18	**RSVD_30_18** Access: RO _Custom_GTIReset: BUS
	17:16	**Report fifo cfg hi bits 9_8** Access: RO _Custom_GTIReset: BUS
	15:8	**RSVD_15_8** Access: RO _Custom_GTIReset: BUS
	7:0	**Report fifo cfg hi bits 0_7** Access: RO _Custom_GTIReset: BUS

Report Queue CFG LO

RPTQCFGLO - Report Queue CFG LO		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 098A8h		
Config to MCI and DFT Ring		
DWord	**Bit**	**Description**
0	31:0	**Report fifo cfg low** Access: RO _Custom_GTIReset: BUS

Reset Control Register

RESET_CTRL - Reset Control Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	020D0h-020D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_RCSUNIT
Address:	220D0h-220D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_BCSUNIT
Address:	1C00D0h-1C00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT0
Address:	1C40D0h-1C40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT1
Address:	1C80D0h-1C80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT0
Address:	1D00D0h-1D00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT2
Address:	1D40D0h-1D40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT3
Address:	1D80D0h-1D80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT1
Address:	1E00D0h-1E00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT4
Address:	1E40D0h-1E40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT5

RESET_CTRL - Reset Control Register	
Address:	1E80D0h-1E80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT2
Address:	1F00D0h-1F00D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT6
Address:	1F40D0h-1F40D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VCSUNIT7
Address:	1F80D0h-1F80D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_VECSUNIT3
Address:	1A0D0h-1A0D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_CCSUNIT0
Address:	1C0D0h-1C0D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_CCSUNIT1
Address:	1E0D0h-1E0D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_CCSUNIT2
Address:	260D0h-260D3h
Name:	Reset Control Register
ShortName:	RESET_CTRL_CCSUNIT3

Soft reset flow for an engine (Render, Blitter, Video, Video Enhancement) is asynchronous to the context execution in HW. SW needs a deterministic way to ensure it resets the context it intends to. One way to achieve this is to ensure HW doesn't switch out the context while SW is doing a soft reset. This is achieved by having an explicit interface between HW-SW to prepare the engine prior to the soft reset. SW sets the Request Reset in RESET_CTRL register of an engine indicating SW wants to initiate a soft reset flow for the corresponding engine. In response to Request Reset bit set, HW sets Ready for Reset bit of RESET_CTRL register indicating engine readiness for reset. As part of the reset readiness HW will not allow any context switch to take place and also ensure any ongoing context switch is paused on a clean context boundary (context save in progress is completed, Context Switch Status Buffer updates are allowed to complete).
SW polls for Ready for Reset bit to be set before it does soft reset for the corresponding engine. Reading EXECLIST_STATUS register at this point provides the active context in HW that will get reset. On engine reset Request Reset bit will get reset with rest of the engine logic.
Upon polling EXECLIST_STATUS register for active context SW might decide not to reset the engine and can reset the Request Reset in RESET_CTRL register. On Request Reset getting reset by SW, HW must continue with execution.

RESET_CTRL - Reset Control Register

SW setting Ready for Reset bit in RESET_CTRL register of an engine need not be followed by the corresponding engine reset.
SW writing to Request Reset bit in RESET_CTRL register is preparing the engine for reset whereas SW writing to GDRST triggers the actual reset flow in HW.

Programming Notes

SW must not do Reset Readiness Handshake as part of the reset recovery on an CAT error.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:4	**Reserved** Access: R/W
	3	**Reserved** Access: R/W Format: PBC
	2	**Reserved** Access: R/W
	1	**Ready for Reset** Access: R/W Format: U1 When set indicates render engine is ready for reset. This bit gets cleared on engine reset or when Soft Reset In progress is cleared.
	0	**Request Reset** Access: R/W Format: U1 "Request Reset" bit must be read as "Readyness for Reset". When set indicates SW wishes to reset the render engine. On seeing this bit set Command Streamer will take appropriate action and set Ready For Reset status bit. This bit gets cleared on engine reset. This bit can also be cleared by writing "0" to this bit.

Reset Flow Control Messages 0

RSTFCTLMSG0 - Reset Flow Control Messages 0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
CrashLogSaved:	true
CrashLogVisibility:	cspec
Address:	08108h

Soft-Reset and FLR Flow Control Message Registers

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:3	**Reserved** Access: RO _Custom_GTIReset: BUS Reserved
	2	**FLR Done ack from Pmunit** Access: R/W Set _Custom_GTIReset: BUS FLR Done ack from Pmunit: 1: PM unit sets this bit to acknowledge the FLR done message has been forwarded to SA through GAM interface. 0: Default Value. If the bit was set by PM then Cpunit hardware clears it once FLR is completed.
	1	**Global Resource Arbitration Acknowledgement Messages** Access: R/W _Custom_GTIReset: BUS Global Resource Arbitration Acknowledgement Message from PM: '1' : CP_ARB_REQ_ACK - Acknowledgement for CPunit's global resource arbitration request '0' : CP_ARB_RELEASE_ACK - Acknowledgement to CPunit's release of global resources

RSTFCTLMSG0 - Reset Flow Control Messages 0

	0	**CP Busy / Idle Status Acknowledgement Messages** Access: R/W _Custom_GTIReset: BUS CP Busy / Idle Status Acknowledgement Message from PM: '0' : CP_NOT_BUSY_ACK - Acknowledgement that the CPunit is idle. '1' : CP_BUSY_ACK - Acknowledgement that the CPunit is busy.

Revision Identification and Class Code register

RID2_CC_0_2_0_PCI - Revision Identification and Class Code register

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00008h

This register contains the revision number. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

DWord	Bit	Description
0	31:24	**Base Class Code** Default Value: 00000011b Access: RO _Custom_GTIReset: BUS This is an 8-bit value that indicates the base class code. This code has the value 03h, indicating a Display Controller.
	23:16	**Sub-Class Code** Default Value: 00000000b Access: RO Variant _Custom_GTIReset: BUS The value is based on GTTMMADR Baroffset 0x10100Ch bit 9 (Display_Present). When GU_CNTL_PROTECTED[Display_present] = Display exists, this value is 00h, indicating VGA compatible controller. When GU_CNTL_PROTECTED[Display_present] = No display exists, this value is 80h, indicating other display device.
	15:8	**Programming Interface** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Value is 00h
	7:0	**Revision Identification Number** Default Value: 00h Access: R/W Variant _Custom_GTIReset: BUS All 8 bits of Revision ID is acquired through fuse pull as per Chassis 2.1 updates

RING_BUFFER_HEAD_PREEMPT_REG

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0214Ch-0214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_RCSUNIT_CTX
Address:	2214Ch-2214Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_BCSUNIT_CTX
Address:	1C014Ch-1C014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT0_CTX
Address:	1C414Ch-1C414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT1_CTX
Address:	1C814Ch-1C814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT0_CTX
Address:	1D014Ch-1D014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT2_CTX
Address:	1D414Ch-1D414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT3_CTX
Address:	1D814Ch-1D814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT1_CTX
Address:	1E014Ch-1E014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT4_CTX
Address:	1E414Ch-1E414Fh

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT5_CTX
Address:	1E814Ch-1E814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT2_CTX
Address:	1F014Ch-1F014Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT6_CTX
Address:	1F414Ch-1F414Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VCSUNIT7_CTX
Address:	1F814Ch-1F814Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_VECSUNIT3_CTX
Address:	1A14Ch-1A14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_CCSUNIT0_CTX
Address:	1C14Ch-1C14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_CCSUNIT1_CTX
Address:	1E14Ch-1E14Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_CCSUNIT2_CTX
Address:	2614Ch-2614Fh
Name:	RING_BUFFER_HEAD_PREEMPT_REG
ShortName:	RING_BUFFER_HEAD_PREEMPT_REG_CCSUNIT3_CTX

This register contains the Head pointer offset in the ring when the last PREEMPTABLE command was executed and caused the head pointer to move due to the UHPTR register being valid. If the PREEMPTABLE command is executed as part of the batch buffer then the value of the register will be the offset in the ring of the command past the batch buffer start that contained the preemptable command.
This is a global register and context save/restored as part of power context image.

RING_BUFFER_HEAD_PREEMPT_REG - RING_BUFFER_HEAD_PREEMPT_REG

Preemptable Commands	Source
• MI_ARB_CHECK • 3D_PRIMITIVE • GPGPU_WALKER • MEDIA_STATE_FLUSH • PIPE_CONTROL (Only in GPGPU mode of pipeline selection) • MI_ATOMIC (Post Sync Operation set in GPGPU mode of pipeline selection) • MI_SEMAPHORE_SIGNAL (Post Sync Operation set in GPGPU mode of pipeline selection)	RenderCS

Preemptable Commands	Source
MI_ARB_CHECK	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS

Programming Notes

Programming Restriction:
This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:21	**Last Wrap Count** Access: R/W
	20:2	**Preempted Head Offset** Access: R/W Format: U19 This field contains the Head pointer offset in the ring when the last MI_ARB_CHECK command was executed and caused the head pointer to move due to the UHPTR register being valid.
	1:0	**Ring/Batch Indicator** Access: R/W

Value	Name	Description
0h	Ring	Preemptable command was executed in ring and caused head pointer to be updated.
1h	Batch	Preemptable command was executed in batch and caused head pointer to be updated.
2h	2nd level batch	Preemptable command was executed in second level batch and caused head pointer to be updated.

Ring Buffer Control

RING_BUFFER_CTL - Ring Buffer Control	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0203Ch-0203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_RCSUNIT_CTX
Address:	2203Ch-2203Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_BCSUNIT_CTX
Address:	1C003Ch-1C003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT0_CTX
Address:	1C403Ch-1C403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT1_CTX
Address:	1C803Ch-1C803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT0_CTX
Address:	1D003Ch-1D003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT2_CTX
Address:	1D403Ch-1D403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT3_CTX
Address:	1D803Ch-1D803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT1_CTX
Address:	1E003Ch-1E003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT4_CTX
Address:	1E403Ch-1E403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT5_CTX

RING_BUFFER_CTL - Ring Buffer Control

Address:	1E803Ch-1E803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT2_CTX

Address:	1F003Ch-1F003Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT6_CTX

Address:	1F403Ch-1F403Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VCSUNIT7_CTX

Address:	1F803Ch-1F803Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_VECSUNIT3_CTX

Address:	1A03Ch-1A03Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_CCSUNIT0_CTX

Address:	1C03Ch-1C03Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_CCSUNIT1_CTX

Address:	1E03Ch-1E03Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_CCSUNIT2_CTX

Address:	2603Ch-2603Fh
Name:	Ring Buffer Control
ShortName:	RING_BUFFER_CTL_CCSUNIT3_CTX

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.

DWord	Bit	Description
0	31:21	**Reserved** Access: RO Format: MBZ
	20:12	**Buffer Length** Access: R/W Format: U9-1 This field is written by SW to specify the length of the ring buffer in 4 KB Pages.Range = [0 = 1 page = 4 KB, 1FFh = 512 pages = 2 MB]

RING_BUFFER_CTL - Ring Buffer Control

Value	Name	Description
0		1 page = 4 KB
1FFh		512 pages = 2 MB

11 **RBWait**

Access:	R/W

Indicates that this ring has executed a WAIT_FOR_EVENT instruction and is currently waiting. Software can write a "1" to clear this bit, write of "0" has no effect. When the RB is waiting for an event and this bit is cleared, the wait will be terminated, and the RB will be returned to arbitration.

10 **Semaphore Wait**

Access:	R/W

Indicates that this ring has executed a MI_SEMAPHORE_WAIT instruction and is currently waiting for wait condition to satisfy. Software can write a "1" to clear this bit, write of "0" has no effect.

Programming Notes
Writing a value of 1 will unconditionally cancel the semaphore wait on the next memory comparison. Memory comparison is triggered in signal mode on receiving a semaphore signal and in poll mode on wait timer getting expired.

9:3 **Reserved**

Access:	RO
Format:	MBZ

2:1 **Automatic Report Head Pointer**

Access:	R/W

This field is written by software to control the automatic reporting (write) of this ring buffer's Head Pointer register (register DWord 1) to the corresponding location within the Hardware Status Page. Automatic reporting can either be disabled or enabled at 4KB, 64KB or 128KB boundaries within the ring buffer.

When **Execlist Enable** bit is set the head pointer will be reported to the head pointer location in the Per-Process Hardware Status Page.MI_AUTOREPORT_4KB option.

Value	Name	Description
0	MI_AUTOREPORT_OFF	Automatic reporting disabled
1	MI_AUTOREPORT_64KB	Report every 16 pages (64KB)
2	MI_AUTOREPORT_4KB	Report every page (4KB)This mode must not be enabled in Ring Buffer mode of scheduling to minimize the auto reports.
3	MI_AUTO_REPORT_128KB	Report every 32 pages (128KB).

RING_BUFFER_CTL - Ring Buffer Control

	0	**Ring Buffer Enable** Access: R/W Format: Enable This field is used to enable or disable this ring buffer. It can be enabled or disabled regardless of whether there are valid instructions pending. If disabled and the ring head equals ring tail, all state currently loaded in hardware is considered invalid. **Programming Notes** Ring Buffer Mode of Scheduling: SW must follow the below programming notes during SW initialization phase or while enabling render engine's ring buffer for the first time, this would be coming out of boot, standby, hibernate or reset. This flow must be also followed during ring replay when ring buffer is disabled and enabled. • SW must set the Force Wakeup bit to prevent GT from entering C6. • SW must dispatch workload (dummy context) to initialize render engine with default state such that any context switches that occur subsequently (Power Save) will save and restore coherent device state. Indirect pointers used in 3D states must point to valid graphics surface existing in memory. PP_DCLV followed by PP_DIR_BASE register should be programmed as part of initialization workload if PPGTT is enabled in GFX_MODE register. • SW must ensure all the register (MMIO) initialization/programming through CPU happens in this block or latter, this ensures the MMIO state is save/restored on subsequent context switches (Power Sequences). • Once the render engine is programmed with valid state and the configuration, Force Wakeup bit should be reset to enable C6 entry.

Ring Buffer Head

RING_BUFFER_HEAD - Ring Buffer Head	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02034h-02037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_RCSUNIT_CTX
Address:	22034h-22037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_BCSUNIT_CTX
Address:	1C0034h-1C0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT0_CTX
Address:	1C4034h-1C4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT1_CTX
Address:	1C8034h-1C8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT0_CTX
Address:	1D0034h-1D0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT2_CTX
Address:	1D4034h-1D4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT3_CTX
Address:	1D8034h-1D8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT1_CTX
Address:	1E0034h-1E0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT4_CTX
Address:	1E4034h-1E4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT5_CTX

RING_BUFFER_HEAD - Ring Buffer Head

Address:	1E8034h-1E8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT2_CTX

Address:	1F0034h-1F0037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT6_CTX

Address:	1F4034h-1F4037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VCSUNIT7_CTX

Address:	1F8034h-1F8037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_VECSUNIT3_CTX

Address:	1A034h-1A037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_CCSUNIT0_CTX

Address:	1C034h-1C037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_CCSUNIT1_CTX

Address:	1E034h-1E037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_CCSUNIT2_CTX

Address:	26034h-26037h
Name:	Ring Buffer Head
ShortName:	RING_BUFFER_HEAD_CCSUNIT3_CTX

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.

DWord	Bit	Description
0	31:21	**Wrap Count** Access: R/W Format: U11 This field is incremented by 1 whenever the **Head Offset** wraps from the end of the buffer back to the start (i.e., whenever it wraps back to 0). Appending this field to the **Head Offset** field effectively creates a virtual 4GB Head "Pointer" which can be used as a tag associated with instructions placed in a ring buffer. The Wrap Count itself will wrap to 0 upon overflow.

RING_BUFFER_HEAD - Ring Buffer Head

	20:2	**Head Offset** Access: R/W Format: GraphicsAddress[20:2] This field indicates the offset of the *next* instruction DWord to be parsed. Software will initialize this field to select the first DWord to be parsed once the RB is enabled. (Writing the Head Offset while the RB is enabled is UNDEFINED). Subsequently, the device will increment this offset as it executes instructions - until it reaches the QWord specified by the **Tail Offset**. At this point the ring buffer is considered "empty". **Programming Notes** A RB can be enabled empty or containing some number of valid instructions.
	1:0	**Reserved** Access: RO Format: MBZ

Ring Buffer Start

RING_BUFFER_START - Ring Buffer Start	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02038h-0203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_RCSUNIT_CTX
Address:	22038h-2203Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_BCSUNIT_CTX
Address:	1C0038h-1C003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT0_CTX
Address:	1C4038h-1C403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT1_CTX
Address:	1C8038h-1C803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT0_CTX
Address:	1D0038h-1D003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT2_CTX
Address:	1D4038h-1D403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT3_CTX
Address:	1D8038h-1D803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT1_CTX
Address:	1E0038h-1E003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT4_CTX
Address:	1E4038h-1E403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT5_CTX

RING_BUFFER_START - Ring Buffer Start

Address:	1E8038h-1E803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT2_CTX
Address:	1F0038h-1F003Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT6_CTX
Address:	1F4038h-1F403Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VCSUNIT7_CTX
Address:	1F8038h-1F803Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_VECSUNIT3_CTX
Address:	1A038h-1A03Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_CCSUNIT0_CTX
Address:	1C038h-1C03Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_CCSUNIT1_CTX
Address:	1E038h-1E03Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_CCSUNIT2_CTX
Address:	26038h-2603Bh
Name:	Ring Buffer Start
ShortName:	RING_BUFFER_START_CCSUNIT3_CTX

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.

DWord	Bit	Description
0	31:12	**Starting Address** Access: R/W Format: GraphicsAddress[31:12] This field specifies Bits 31:12 of the 4KB-aligned starting Graphics Address of the ring buffer. Address bits 31 down to 29 must be zero. All ring buffer pages must map to Main Memory (uncached) pages. Ring Buffer addresses are always translated through the global GTT.

RING_BUFFER_START - Ring Buffer Start			
	11:0	**Reserved**	
		Access:	RO
		Format:	MBZ

Ring Buffer Tail

RING_BUFFER_TAIL - Ring Buffer Tail	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02030h-02033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_RCSUNIT_CTX
Address:	22030h-22033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_BCSUNIT_CTX
Address:	1C0030h-1C0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT0_CTX
Address:	1C4030h-1C4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT1_CTX
Address:	1C8030h-1C8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT0_CTX
Address:	1D0030h-1D0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT2_CTX
Address:	1D4030h-1D4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT3_CTX
Address:	1D8030h-1D8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT1_CTX
Address:	1E0030h-1E0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT4_CTX
Address:	1E4030h-1E4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT5_CTX

RING_BUFFER_TAIL - Ring Buffer Tail

Address:	1E8030h-1E8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT2_CTX

Address:	1F0030h-1F0033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT6_CTX

Address:	1F4030h-1F4033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VCSUNIT7_CTX

Address:	1F8030h-1F8033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_VECSUNIT3_CTX

Address:	1A030h-1A033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_CCSUNIT0_CTX

Address:	1C030h-1C033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_CCSUNIT1_CTX

Address:	1E030h-1E033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_CCSUNIT2_CTX

Address:	26030h-26033h
Name:	Ring Buffer Tail
ShortName:	RING_BUFFER_TAIL_CCSUNIT3_CTX

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information. These registers can only be updated through a restore of a context thru execution list submission.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:21	**Reserved** Access: RO Format: MBZ

RING_BUFFER_TAIL - Ring Buffer Tail

	20:3	**Tail Offset** Access: R/W Format: GraphicsAddress[20:3] This field is written by software to specify where the valid instructions placed in the ring buffer end. The value written points to the QWord past the last valid QWord of instructions. In other words, it can be defined as the next QWord that software will write instructions into. Software must write subsequent instructions to QWords following the Tail Offset, possibly wrapping around to the top of the buffer (i.e., software can't skip around within the buffer).Note that all DWords prior to the location indicated by the **Tail Offset** must contain valid instruction data - which may require instruction padding by software. See **Head Offset** for more information.
	2:0	**Reserved** Access: RO Format: MBZ

Ring Context Address Register 0 for GTI Doorbell Unit

DRBCTXADDR0 - Ring Context Address Register 0 for GTI Doorbell Unit

Register Space:	MMIO: 0/2/0
Size (in bits):	64
Address:	01950h

DWord	Bit	Description
0..1	63:32	**CTX base address 63:32** Access: R/W _Custom_GTIReset: BUS Bits [63:32] of HPA base address which MDRB will use as the offset for its context save / restore
	31:6	**CTX base address 31:6** Access: R/W _Custom_GTIReset: BUS Bits [31:6] of HPA base address which MDRB will use as the offset for its context save / restore
	5:0	**Reserved** Access: RO Format: MBZ

Ring Context Start Register for GTI Doorbell Unit

DRBCTXSTART - Ring Context Start Register for GTI Doorbell Unit

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0194Ch

Message registers have bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16].
In order to set bit0, for example, the data would be 0x0001_0001. In order to clear bit0, for example, the data would be 0x0001_0000.
Note that mask bit is the data bit offset + 16. Message registers are protected from non-GT writes via the Message Channel.

DWord	Bit	Description
0	31:16	**Context Save Mask** Access: WO _Custom_GTIReset: BUS This register isn't context save/restored.
	15:2	**Reserved** Access: RO Format: MBZ
	1:0	**Context start** Access: R/W Hardware Clear _Custom_GTIReset: BUS RPM will program these bits to notify MDRB to initiate either a context save or a context restore. MDRB will clear these bits once the context procedure is completed and the ACK is sent back to RPM. 2'b11 = Reserved 2'b10 = Context restore start 2'b01 = Context save start 2'b00 = Normal operation - DEFAULT Programming Note - It is assumed that this value will be static once programmed and not changed until MDRB clears the bits after ACKing the context procedure back to RPM

RMTIMEOUTREG_CAPTURE

RMTIMEOUTREG_CAPTURE		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	420E0h-420E3h	
Name:	RM TIMEOUT REGISTER OFFSET	
ShortName:	RMTIMEOUTREG_CAPTURE	
Reset:	soft	

DWord	Bit	Description
0	31:0	**REGISTER OFFSET VALUE** Access: RO Offset of the Register that caused RM TIMEOUT.

Root2Remote FLR Trigger

RT2REMFLR - Root2Remote FLR Trigger

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	101808h

For a multi-tile configuration, this register will be used by hardware. The root tile hardware will trigger a remote tile FLR using this register.
This register is for hardware communication purposes only. This register is not intended to be used by software.

DWord	Bit	Description
0	31:16	**SPARE2** Default Value: 0000h Access: R/W _Custom_GTIReset: BUS Reserved
	15:8	**FLR Function Number** Default Value: 00h Access: R/W _Custom_GTIReset: BUS Indicates which function number to associate FLR with. 00h - Physical Function (PF). 01h - Virtual Function 1 (VF1) 02h - VF2 .. 3Fh - VF63 40h-FFh - undefined
	7:2	**SPARE1** Default Value: 00000000000000b Access: R/W _Custom_GTIReset: BUS Reserved
	1	**FLRTYPE** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Type of FLR to initiated. 0 : FLR 1 : Driver initiated FLR

RT2REMFLR - Root2Remote FLR Trigger

	0	**HWFLRINIT** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Initiate FLR. The root tile hardware will write this register in a remote tile to initiate FLR in a remote tile. 0 : (default)No action 1 : Initiate remote FLR Remote tile hardware will clear this bit as part of "ack'ing" complete.

RSA for uOS/Soft Scratch

UOS_RSA_SCRATCH - RSA for uOS/Soft Scratch

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Description

The very first register C200h of the RSA uOS Scratch Space register has the address to the graphics memory location (GGTT Address Space) containing the RSA signature of the uOS code to be loaded on to the GuC.
Usage:RSA signature data for the uOS code is 96 Dwords in size (3072 bits). RSA signature for the uOS to be loaded on to GuC is programmed by the host in graphics memory (GGTT Address Space) and the address to this memory location is programmed to the very first register (C200h) of the RSA uOS scratch space. Host does this operation prior to triggering the uOS load to the GuC. During the uOS load by the GuC DMA, the onchip Boot ROM code reads the RSA signature from the memory and starts the RSA unwrap. This RSA check is done to ensure that the full HASH check value used for Hash operation of the uOS by Shim, itself is correct.
These registers can also be used as Soft Scratch registers defined for use by Code after the RSA operation at Boot.

DWord	Bit	Description
0	31:0	**RSA/Scratch** Access: R/W

RTADDR_LSB

RTADDR_LSB - RTADDR_LSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	124830h	
Register providing the base address of root-entry table.		
DWord	**Bit**	**Description**
0	31:12	**RTA** Default Value: 0000000h Access: R/W _Custom_GTIReset: BUS This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
	11	**RTT** Default Value: 0h Access: R/W _Custom_GTIReset: BUS This field specifies the type of root-table referenced by the Root Table Address (RTA) field; 0: Root Table1: Extended Root Table
	10:0	**Reserved** Access: RO Format: MBZ

RTADDR_MSB

RTADDR_MSB - RTADDR_MSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	124834h	
Register providing the base address of root-entry table.		
DWord	**Bit**	**Description**
0	31:7	**Reserved** Access: RO Format: MBZ
	6:0	**RTA** Default Value: 00h Access: R/W _Custom_GTIReset: BUS This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.

RTT_CR_SPARE

RTT_CR_SPARE	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	168B90h-168B93h
Name:	RTT_CR_SPARE
ShortName:	RTT_CR_SPARE
Reset:	global

Spare registers for RTT Lane

DWord	Bit	Description
0	31:0	**cfg_rtt_cr_spare** Default Value: 0041000h cfg_rtt_cr_spare_defaultreset Access: R/W PCS_Glue::RTT_CR_SPARE::rtt_cr_spare

Sampler control register

SAMPLER_CTL - Sampler control register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0E140h

DWord	Bit	Description
0	31:16	**ECO Reserved 1** Access: R/W Reserved: MBZ
	15:8	**Reserved** Access: R/W
	7	**ECO Reseved 7** Access: R/W
	6	**ECO Reseved 6** Access: R/W
	5	**ECO Reseved 5** Access: R/W
	4	**ECO Reseved 4** Access: R/W
	3	**ECO Reseved 3** Access: R/W
	2	**ECO Reseved 2** Access: R/W
	1	**ECO Reseved 1** Access: R/W
	0	**ECO Reseved 0** Access: R/W

Sampler Dummy Register

SMP_DUMMY - Sampler Dummy Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0E000h
Name:	Sampler Dummy Address
ShortName:	Sampler_Dummy_Address

This register is defined so that a non-posted MMIO cycle to this destination would ensure all cycles are flushed on the message channel between the source and destination. This register is used in the engine context to ensure all state is delivered. The value programmed in this register must not change the behavior of the GPU.

DWord	Bit	Description
0	31:0	**Reserved** Access: RO Format: MBZ

SAMPLER Mode Register

SAMPLER_MODE - SAMPLER Mode Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	0E18Ch
Name:	SAMPLER Mode Register
ShortName:	SAMPLER_MODE

This register has bit-wise masking applied for writes. The register consists of 16 bits of data in [15:0], and 16 bits of corresponding masks in [31:16]. To set bit0, for example, the data would be 0x0001_0001. To clear bit0, for example, the data would be 0x0001_0000. Note that mask bit is the data bit offset + 16.

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask
	15	**enble smallPL** Access: R/W Format: enable **Programming Notes** This bit MUST be set to ensure optimal power in 3D Sampler. Must not be enabled if **cache_flush** message is sent to sampler.
	14	**L1 Cache Set Selection** Access: R/W This field controls how Set0 and Set1 of the Sampler L1 Cache are selected. Value / Name / Description: 0h / Extended_Tag **[Default]** / When this bit is set to 0h, Sampler will use Bit 8 of the Extended Tag To Control Set selection. 1h / XOR_UVQ / When this bit is set to 1h, Sampler will use an XOR of Various u, v, and q texel coordinate bits to select set
	13:12	**Sampler Cache Set XOR selection** Access: R/W Format: U2 These bits have an impact only when the Sampler cache is configured in 16 way set associative mode. If the cache is being used for immediate data or for blitter data these bits have no effect.

SAMPLER_MODE - SAMPLER Mode Register

Value	Name	Description
00b	None	No XOR.
01b	Scheme 1	New_set_mask[3:0] = Tiled_address[16:13]. New_set[3:0] less than or = New_set_mask[3:0] ^Old_set[3:0]. Rationale: These bits can distinguish among 16 different equivalent classes of virtual pages. These bits also represent the lsb for tile rows ranging from a pitch of 1 tile to 16 tiles.
10b	Scheme 2	New_set_mask[3] = Tiled_address[17] ^ Tiled_address[16]. New_set_mask[2] = Tiled_address[16] ^ Tiled_address[15]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[14] ^ Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: More bits on each XOR can give better statistical uniformity on sets and since two lsbs are taken for each tile row size, it reduces the chance of aliasing on sets.
11b	Scheme 3 **[Default]**	New_set_mask[3] = Tiled_address[22] ^ Tiled_address[21] ^ Tiled_address[20] ^ Tiled_address[19]. New_set_mask[2] = Tiled_address[18] ^ Tiled_address[17] ^ Tiled_address[16]. New_set_mask[1] = Tiled_address[15] ^ Tiled_address[14]. New_set_mask[0] = Tiled_address[13]. New_set[3:0] less than or = New_set_mask[3:0] ^ Old_set[3:0]. Rationale: More bits on each XOR can give better statistical uniformity on sets and since each XOR has different bits, it reduces the chance of aliasing on sets even more.

Programming Notes
This field should be programmed as "00b" corresponding to NO XOR option when 3D map performance fix in MT is enabled using the field "Sampler Set Remapping for 3D Disable" in the SAMPLER Mode Register.

11:10 **ECO Reserved 2b**

Access:	R/W
Format:	MBZ

9 **SC disable power optimization for back to back cache EBB read**

Access:	R/W
Format:	disable

8 **Sampler L2 Disable**

Access:	R/W
Format:	Disable

Will disable the L2 cache and force all access to be misses

SAMPLER_MODE - SAMPLER Mode Register

7 Disable SC flop stage bypass for HDC read

Access:	R/W
Format:	disable

6 Compressed Overfill disable

Access:	R/W
Format:	disable

5 Headerless Message for Pre-emptable Contexts

Access:	R/W
Format:	Enable

When set to 1h, this bit enables sampler to support headerless messages for pre-emptable GPGPU contexts. When set to 0h, it reverts to the previous behavior where pre-emptable GPGPU contexts must have headers on all sampler messages.

Value	Name	Description
0h		Headers must be used on all sampler messages if this bit is programmed to 0h.
1h	**[Default]**	Headerless sampler messages may be used for pre-emptable contexts (this is the default behavior all contexts)

4 Reserved

Access:	RO
Format:	MBZ

3 ECO Reserved 5

Access:	R/W
Format:	MBZ

2 Context-Based Cache Invalidation Disable

Access:	R/W
Format:	DISABLE

This bit will be used to disable context-based invalidation of the State and Texture Cache.

Value	Name	Description
0h	ENABLE **[Default]**	When set to 0h (default) only entries associated with the context requesting the cache invalidation will be invalidated.
1h	DISABLE	When set to 1h context-based invalidation of the state cache is not used. Instead, all entries in the state cache are invalidated regardless of which context it belongs to.

1 Reserved

Access:	RO
Format:	MBZ

SAMPLER_MODE - SAMPLER Mode Register

0 **Indirect State Base Addr Override**

Access:	R/W
Format:	Enable

This bit is used to control whether Indirect State (Border Color) to be relative to same base address as SAMPLER_STATE or relative to the DYNAMIC_STATE_BASE_ADDR
This bit must be set to 1. Border Color must be in the Dynamic State heap in order to allow for resource copy of sampler state to work correctly.

Value	Name	Description
0h	OVERRIDE_DISABLE **[Default]**	When set to 0h, this bit allows Indirect State (.e.g Border Color) to be stored in the Bindless Sampler State heap. This bit should not be set to 0h by SW as this will prevent resource copies of sampler state from being done correct when border color is required.
1h	OVERRIDE_ENABLE	When set to 1h, this bit allows Indirect State (e.g. Border Color) to be stored in the Dynamic State heap. This bit must be set to 1h by SW to ensure resource copies of sampler state are done correctly when border color is required.

SAMPLER READ DATA

SAMPLER_RDATA - SAMPLER READ DATA		
Register Space:	MMIO: 0/2/0	
Access:	RO Variant	
Size (in bits):	32	
Address:	0E144h	
DWord	**Bit**	**Description**
0	31:0	**Reserved** Access: RO Variant

SARB-LTISEQ Flush Done Message

SARB_LTISEQ_FLUSH_DONE - SARB-LTISEQ Flush Done Message

Register Space:	MMIO: 0/2/0
Access:	R/W Hardware Clear
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B4A4h

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:16	**Mask** Access: R/W
	15:4	**Reserved** Access: RO Format: MBZ
	3	**SARB3 Flush Done** Access: R/W Hardware Clear
	2	**SARB2 Flush Done** Access: R/W Hardware Clear
	1	**SARB1 Flush Done** Access: R/W Hardware Clear
	0	**SARB0 Flush Done** Access: R/W Hardware Clear

SBFT Overrides

SBFTOVRD - SBFT Overrides

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B184h

This is a basic register template

DWord	Bit	Description
0	31:7	**Reserved** Access: RO Format: MBZ
	6	**SBFT Mode Enable** Access: R/W Format: Enable Value / Name / Description 1b / / When enabled, cycles are forced cacheable based on programming for Bit5 of this register, engine ID is overridden based on bits4:0 of this register, and ctypes that require address translation are converted to non-translation ctypes. 0 / **[Default]** /
	5	**SBFT Force Cacheability Control Enable** Access: R/W Value / Name / Description 1b / / Make all the cycles as cacheable 0 / **[Default]** /
	4:0	**Engine ID** Access: R/W EngineID to be programmed by Gdtunit and engine id function in the bank will use this value and override the final EngineID generated towards cache or towards the memory when dt_l3sbftmode is set.

SBLC_PWM_CTL1

SBLC_PWM_CTL1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	C8250h-C8253h
Name:	South BLM Control 1
ShortName:	SBLC_PWM_CTL1
Reset:	soft

DWord	Bit	Description
0	31	**PWM Enable** Access: R/W This bit enables the PWM counter logic. Disabled PWM will drive 0, which can be inverted to 1 with the polarity bit. Value / Name: 0b – Disable 1b – Enable Restriction: Program the frequency and duty cycle before enabling PWM.
	30	**Reserved** Access: RO Format: MBZ
	29	**Backlight Polarity** Access: R/W This field controls the polarity of the PWM signal. Value / Name: 0b – Active High 1b – Active Low
	28:3	**Reserved** Access: RO Format: MBZ
	2	**Genlock Direction IO Select** Access: R/W IO pins are muxed between the backlight and genlock direction control signals. Set this field to switch the mux to allow the genlock direction controls to be driven and to enable the IO output for the genlock signals.

SBLC_PWM_CTL1

Value	Name
1b	Genlock
0b	Backlight

1 **Genlock Direction Select Pin Value**

Access:	R/W

This field specifies the value to drive on the genlock direction select pin (shared with backlight PWM). This value is only used when the Genlock Direction IO Select = Genlock.

Value	Name
1b	Genlock Secondary
0b	Genlock Primary

0 **Genlock Direction Enable Pin Value**

Access:	R/W

This field specifies the value to drive on the genlock direction enable pin (shared with backlight enable). This value is only used when the Genlock Direction IO Select = Genlock.

Value	Name
1b	Enable Motherboard Genlock Circuit
0b	Disable Motherboard Genlock Circuit

SBLC_PWM_DUTY

SBLC_PWM_DUTY		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	C8258h-C825Bh	
Name:	South Backlight PWM Duty Cycle	
ShortName:	SBLC_PWM_DUTY	
Reset:	soft	

DWord	Bit	Description
0	31:0	**Duty Cycle** Access: R/W This field controls the active portion of the backlight PWM duty cycle. The value should be programmed to (SBLC_PWM_FREQ Frequency * desired duty cycle percentage / 100). A value of zero will give a 0% active duty cycle. A value equal to SBLC_PWM_FREQ Frequency will give a 100% active duty cycle. When written, the new value will take affect at the end of the current PWM cycle. **Restriction** This should never be larger than SBLC_PWM_FREQ Frequency.

SBLC_PWM_FREQ

SBLC_PWM_FREQ		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	C8254h-C8257h	
Name:	South Backlight PWM Frequency	
ShortName:	SBLC_PWM_FREQ	
Reset:	soft	

DWord	Bit	Description
0	31:0	**Frequency** Access: R/W This field controls the backlight PWM frequency. The value should be programmed to (Reference clock frequency / desired PWM frequency). The reference clock frequency can be found in the RAWCLK_FREQ register.

SCRATCH 1 from LPFCunit

SCRATCH_LPFC1 - SCRATCH 1 from LPFCunit		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
_Custom_GTIReset:	DEV	
Address:	0B474h	
DWord	**Bit**	**Description**
0	31:0	**SCRATCH bits from LPFCunit** Access: R/W _Custom_GTIReset: DEV

SCRATCH2 Register

SCRATCH2 - SCRATCH2 Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B140h

DWord	Bit	Description
0	31:30	**SCRATCH31** Access: R/W
	29:28	**SCRATCH29** Access: R/W
	27	**Reserved** Access: RO Format: MBZ
	26	**Reserved** Access: RO Format: MBZ
	25:21	**SCRATCH25** Access: R/W
	20:15	**Reserved** Access: RO Format: MBZ
	14:9	**Reserved** Access: RO Format: MBZ
	8:4	**LTCD EBB Conflict L3-Read Aging count** Access: R/W This bit-field will determine the number of EBB conflicts experienced by the L3-read in order to age in the L3 FIFO. Value: 10 — **[Default]** Value: [1,31]
	3	**LTCD EBB Conflict L3-Read Aging enable** Access: R/W This bit-field will enable L3-Read aging in LTCD data unit due to EBB conflicts. During EBB conflicts, L3-fill will be preferred over L3-reads, and this aggressive fill selection can hold up the

SCRATCH2 - SCRATCH2 Register

reads in L3 FIFO depending on the duration of EBB conflicts. L3-read aging will ensure fairness to an L3-read cycle that has been held back due to EBB conflicts by making the L3-fills ineligible once the read has aged.

Value	Name	Description
1	**[Default]**	LTCD EBB conflict L3-Read aging is enabled
0		LTCD EBB conflict L3-Read aging is disabled

2 **SCRATCH2**

Access:	R/W

1 **LTCD L3 FIFO OOO Disable**

Access:	R/W

This bit-field will disable L3 FIFO OOO implementation in LTCD-data unit and revert to implementation where only one L3 FIFO was used.

Value	Name	Description
0	**[Default]**	LTCD L3 FIFO OOO implementation is enabled
1		LTCD L3 FIFO OOO implementation is disabled

0 **Reserved**

Access:	RO
Format:	MBZ

SCRATCH3 Register

SCRATCH3 - SCRATCH3 Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B154h

DWord	Bit	Description
0	31	**Reserved**
	31:13	**SPARE FIELDS** Access: R/W
	30:13	**SPARE FIELDS** Access: R/W
	12	**Merge Disable for non-128B Compressible Writes** Default Value: 0 Access: R/W Format: Disable _Custom_GTIReset: DEV By default, if compression partial write merging support is enabled, all compressible writes can serve as mergeable parent cycles. If this bit is set, L3 will limit merging for compressible surfaces to only apply when receiving a 128B write (marked as such by the client).
	11	**Force Uncacheable Big Hammer** Access: R/W Value / Name / Description: 0 **[Default]** — All the POR rules for Cacheable vs Uncacheable are applied 1 — • All the POR rules for C/UC will be overridden and every L3 cycle is made as L3 Uncacheable. 2. • Note: This does not apply for URB related transactions.
	10:8	**LTCD TAG ROINV FSM WAIT TIME** Access: R/W Used to derive the number of clocks for which the ROINV FSM will wait, in a WAIT state, prior to invalidating the state arrays. Valid values start from 4 to account for time it takes ltcc to receive roinv in progress and stall its pipeline towards LTCD-TAGUNIT, to ensure that any functional cycles that sneaks in TAG for those clocks are serviced gracefully.

SCRATCH3 - SCRATCH3 Register

Value	Name
4	default **[Default]**
[4,7]	range

7:4	**Reserved**
Access:	RO
Format:	MBZ
3:0	**Reserved**
Access:	RO
Format:	MBZ

Second Level Batch Buffer Head Pointer Preemption Register

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0213Ch-0213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_RCSUNIT_CTX
Address:	2213Ch-2213Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_BCSUNIT_CTX
Address:	1C013Ch-1C013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT0_CTX
Address:	1C413Ch-1C413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT1_CTX
Address:	1C813Ch-1C813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT0_CTX
Address:	1D013Ch-1D013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT2_CTX
Address:	1D413Ch-1D413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT3_CTX
Address:	1D813Ch-1D813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT1_CTX
Address:	1E013Ch-1E013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT4_CTX
Address:	1E413Ch-1E413Fh

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT5_CTX
Address:	1E813Ch-1E813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT2_CTX
Address:	1F013Ch-1F013Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT6_CTX
Address:	1F413Ch-1F413Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VCSUNIT7_CTX
Address:	1F813Ch-1F813Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_VECSUNIT3_CTX
Address:	1A13Ch-1A13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_CCSUNIT0_CTX
Address:	1C13Ch-1C13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_CCSUNIT1_CTX
Address:	1E13Ch-1E13Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_CCSUNIT2_CTX
Address:	2613Ch-2613Fh
Name:	Second Level Batch Buffer Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_CCSUNIT3_CTX

Description

This register gets updated with the DWord-aligned graphics memory address of the PREEMPTABLE command in the second level batch buffer on which preemption has occurred.
This register value should be looked at only when the preemption has occurred in the second level batch buffer. This is indicated by "Ring/Batch Indicator" in "RING_BUFFER_HEAD_PREEMPT_REG". This register value retains its previous value and doesn't change when the preemption occurs on a preemptable command in ring buffer or in batch buffer.
Preemption is triggered by valid UHPTR in ring buffer mode of scheduling and by a pending execlist in Exec-List mode of scheduling.
This is a global register and context save/restored as part of power context image.

SBB_PREEMPT_ADDR - Second Level Batch Buffer Head Pointer Preemption Register

Refer to **Preemption > ExecList Scheduling** for a list of preemptible commands.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Access: RO Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address of the PREEMPTABLE command in a batch buffer where the Preemption has occurred.
	1:0	**Reserved** Access: RO Format: MBZ

Second Level Batch Buffer Head Pointer Register

SBB_ADDR - Second Level Batch Buffer Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02114h-02117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_RCSUNIT_CTX
Address:	22114h-22117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_BCSUNIT_CTX
Address:	1C0114h-1C0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT0_CTX
Address:	1C4114h-1C4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT1_CTX
Address:	1C8114h-1C8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT0_CTX
Address:	1D0114h-1D0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT2_CTX
Address:	1D4114h-1D4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT3_CTX
Address:	1D8114h-1D8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT1_CTX
Address:	1E0114h-1E0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT4_CTX
Address:	1E4114h-1E4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT5_CTX

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

Address:	1E8114h-1E8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT2_CTX

Address:	1F0114h-1F0117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT6_CTX

Address:	1F4114h-1F4117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VCSUNIT7_CTX

Address:	1F8114h-1F8117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_VECSUNIT3_CTX

Address:	1A114h-1A117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_CCSUNIT0_CTX

Address:	1C114h-1C117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_CCSUNIT1_CTX

Address:	1E114h-1E117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_CCSUNIT2_CTX

Address:	26114h-26117h
Name:	Second Level Batch Buffer Head Pointer Register
ShortName:	SBB_ADDR_CCSUNIT3_CTX

This register contains the current DWord Graphics Memory Address of the last-initiated batch buffer.

Programming Notes

This register should NEVER be programmed by driver, this is for HW internal use only. This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description
0	31:2	**Second Level Batch Buffer Head Pointer** Access: RO Format: GraphicsAddress[31:2] This field specifies the DWord-aligned Graphics Memory Address where the last initiated Second Level Batch Buffer is currently fetching commands. This field is meaningful only when Valid field is set to "1".

SBB_ADDR - Second Level Batch Buffer Head Pointer Register

	1	**Reserved** Access: RO Format: MBZ
	0	**Valid** Access: RO Format: U1

Value	Name	Description
0h	Invalid **[Default]**	Second Level Batch buffer Invalid
1h	Valid	Second Batch buffer Valid.

Second Level Batch Buffer State Register

SBB_STATE - Second Level Batch Buffer State Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02118h-0211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_RCSUNIT_CTX
Address:	22118h-2211Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_BCSUNIT_CTX
Address:	1C0118h-1C011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT0_CTX
Address:	1C4118h-1C411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT1_CTX
Address:	1C8118h-1C811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT0_CTX
Address:	1D0118h-1D011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT2_CTX
Address:	1D4118h-1D411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT3_CTX
Address:	1D8118h-1D811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT1_CTX
Address:	1E0118h-1E011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT4_CTX
Address:	1E4118h-1E411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT5_CTX

SBB_STATE - Second Level Batch Buffer State Register

Address:	1E8118h-1E811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT2_CTX

Address:	1F0118h-1F011Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT6_CTX

Address:	1F4118h-1F411Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VCSUNIT7_CTX

Address:	1F8118h-1F811Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_VECSUNIT3_CTX

Address:	1A118h-1A11Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_CCSUNIT0_CTX

Address:	1C118h-1C11Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_CCSUNIT1_CTX

Address:	1E118h-1E11Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_CCSUNIT2_CTX

Address:	26118h-2611Bh
Name:	Second Level Batch Buffer State Register
ShortName:	SBB_STATE_CCSUNIT3_CTX

This register contains the attributes of the second level batch buffer initiated from the batch Buffer.

This register should not be written by software. These fields should only get written by a context restore. Software should always set these fields via the MI_BATCH_BUFFER_START command when initiating a batch buffer. This register is saved and restored with context.

DWord	Bit	Description	
0	31:10	**Reserved**	
		Access:	RO
		Format:	MBZ
	9:8	**Reserved**	
		Access:	RO
		Format:	MBZ

SBB_STATE - Second Level Batch Buffer State Register

	7:6	**Reserved** Access: RO Format: MBZ
	5	**Address Space Indicator** Access: R/W Note: This field reflects the effective address space indicator security level and may not be the same as the Address Space Indicator written using MI_BATCH_BUFFER_START. **Value** / **Name** / **Description** 0h / GGTT **[Default]** / This second level batch buffer is located in GGTT memory and is privileged 1h / PPGTT / This second level batch buffer is located in PPGTT memory and is non-privileged.
	4	**Reserved** Access: R/W
	3:0	**Reserved** Access: RO Format: MBZ

Second Level Batch Buffer Upper Head Pointer Preemption Register

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02138h-0213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_RCSUNIT_CTX
Address:	22138h-2213Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_BCSUNIT_CTX
Address:	1C0138h-1C013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT0_CTX
Address:	1C4138h-1C413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT1_CTX
Address:	1C8138h-1C813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT0_CTX
Address:	1D0138h-1D013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT2_CTX
Address:	1D4138h-1D413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT3_CTX
Address:	1D8138h-1D813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT1_CTX
Address:	1E0138h-1E013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT4_CTX
Address:	1E4138h-1E413Bh

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register

Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT5_CTX

Address:	1E8138h-1E813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT2_CTX

Address:	1F0138h-1F013Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT6_CTX

Address:	1F4138h-1F413Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VCSUNIT7_CTX

Address:	1F8138h-1F813Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_VECSUNIT3_CTX

Address:	1A138h-1A13Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_CCSUNIT0_CTX

Address:	1C138h-1C13Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_CCSUNIT1_CTX

Address:	1E138h-1E13Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_CCSUNIT2_CTX

Address:	26138h-2613Bh
Name:	Second Level Batch Buffer Upper Head Pointer Preemption Register
ShortName:	SBB_PREEMPT_ADDR_UDW_CCSUNIT3_CTX

Upper 32 bits of the 4GB aligned base address within the host's 64-bit virtual address space of the last preempted second level batch buffer. This register follows the same rules as the SBB_PREEMPT_ADDR register.

Programming Notes

Programming Restriction: This register should NEVER be programmed by driver, this is for HW internal use only.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO

SBB_PREEMPT_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Preemption Register

		Format: MBZ
	24:16	**Reserved** Access: RO Format: MBZ
	15:0	**Second Level Batch Buffer Head Pointer Upper DWORD** Access: R/W Format: GraphicsAddress[47:32]

Second Level Batch Buffer Upper Head Pointer Register

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0211Ch-0211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_RCSUNIT_CTX
Address:	2211Ch-2211Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_BCSUNIT_CTX
Address:	1C011Ch-1C011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT0_CTX
Address:	1C411Ch-1C411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT1_CTX
Address:	1C811Ch-1C811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT0_CTX
Address:	1D011Ch-1D011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT2_CTX
Address:	1D411Ch-1D411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT3_CTX
Address:	1D811Ch-1D811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT1_CTX
Address:	1E011Ch-1E011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT4_CTX
Address:	1E411Ch-1E411Fh

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register

Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT5_CTX
Address:	1E811Ch-1E811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT2_CTX
Address:	1F011Ch-1F011Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT6_CTX
Address:	1F411Ch-1F411Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VCSUNIT7_CTX
Address:	1F811Ch-1F811Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_VECSUNIT3_CTX
Address:	1A11Ch-1A11Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_CCSUNIT0_CTX
Address:	1C11Ch-1C11Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_CCSUNIT1_CTX
Address:	1E11Ch-1E11Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_CCSUNIT2_CTX
Address:	2611Ch-2611Fh
Name:	Second Level Batch Buffer Upper Head Pointer Register
ShortName:	SBB_ADDR_UDW_CCSUNIT3_CTX

Upper 32 bits of the 4GB aligned base address within the host's 64-bit virtual address space, where the last initiated Batch Buffer is currently fetching commands. If no batch buffer is currently active, the Valid bit in BB_ADDR will be 0 and this field is meaningless.

Programming Notes

This register should NEVER be programmed by driver. This is for HW internal use only.

DWord	Bit	Description
0	31:25	**Reserved** Access: RO

SBB_ADDR_UDW - Second Level Batch Buffer Upper Head Pointer Register

		Format: MBZ
	24:16	**Reserved** Access: RO Format: MBZ
	15:0	**Batch Buffer Head Pointer Upper DWORD** Access: RO Format: GraphicsAddress[47:32]

SEL_FETCH_PLANE_CTL

SEL_FETCH_PLANE_CTL	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to PLANE_SURF or plane not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank or pipe not enabled; after armed
Address:	70890h-70893h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_1_A
Reset:	soft
Address:	708B0h-708B3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_2_A
Reset:	soft
Address:	708D0h-708D3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_3_A
Reset:	soft
Address:	708F0h-708F3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_4_A
Reset:	soft
Address:	70920h-70923h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_5_A
Reset:	soft
Address:	71890h-71893h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_1_B
Reset:	soft
Address:	718B0h-718B3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_2_B
Reset:	soft
Address:	718D0h-718D3h

SEL_FETCH_PLANE_CTL	
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_3_B
Reset:	soft
Address:	718F0h-718F3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_4_B
Reset:	soft
Address:	71920h-71923h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_5_B
Reset:	soft
Address:	72890h-72893h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_1_C
Reset:	soft
Address:	728B0h-728B3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_2_C
Reset:	soft
Address:	728D0h-728D3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_3_C
Reset:	soft
Address:	728F0h-728F3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_4_C
Reset:	soft
Address:	72920h-72923h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_5_C
Reset:	soft
Address:	73890h-73893h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_1_D
Reset:	soft
Address:	738B0h-738B3h

SEL_FETCH_PLANE_CTL

Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_2_D
Reset:	soft

Address:	738D0h-738D3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_3_D
Reset:	soft

Address:	738F0h-738F3h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_4_D
Reset:	soft

Address:	73920h-73923h
Name:	Selective Fetch Plane Control
ShortName:	SEL_FETCH_PLANE_CTL_5_D
Reset:	soft

Restriction
Refer to 'Plane Capability and Interoperability' page for plane capabilities and restrictions.

DWord	Bit	Description
0	31	**Selective Fetch Plane Enable** Access: Double Buffered When this bit is set, Plane is enabled for selective fetch update. 0b: Disable 1b: Enable
	30:0	**Spares** Access: Double Buffered

Semaphore Interrupt Register

GUC_SEM_INTR - Semaphore Interrupt Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Bits are set based on the Semaphore Token number sent by Command streamer Read and cleared by the MinIA uKernel or host CPU.		
DWord	**Bit**	**Description**
0	31:0	**Semaphore Token ID** Default Value: 0000h Access: R/WC _Custom_GTIReset: BUS

Semaphore Polling Interval on Wait

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0224Ch-0224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_RCSUNIT
Address:	2224Ch-2224Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_BCSUNIT
Address:	1C024Ch-1C024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT0
Address:	1C424Ch-1C424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT1
Address:	1C824Ch-1C824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT0
Address:	1D024Ch-1D024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT2
Address:	1D424Ch-1D424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT3
Address:	1D824Ch-1D824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT1
Address:	1E024Ch-1E024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT4
Address:	1E424Ch-1E424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT5

SEMA_WAIT_POLL - Semaphore Polling Interval on Wait

Address:	1E824Ch-1E824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT2

Address:	1F024Ch-1F024Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT6

Address:	1F424Ch-1F424Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VCSUNIT7

Address:	1F824Ch-1F824Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_VECSUNIT3

Address:	1A24Ch-1A24Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_CCSUNIT0

Address:	1C24Ch-1C24Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_CCSUNIT1

Address:	1E24Ch-1E24Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_CCSUNIT2

Address:	2624Ch-2624Fh
Name:	Semaphore Polling Interval on Wait
ShortName:	SEMA_WAIT_POLL_CCSUNIT3

The SEMA_WAIT_POLL register contains Poll Interval field which specifies the minimum number of microseconds allowed for command streamer to wait before re-fetching the data from the address mentioned in the MI_SEMAPHORE_WAIT command on WAIT Mode set to POLL until the condition is satisfied while the context is not switched out.When a value of 0 is written the poll interval will be equal to the memory latency of the read completion.

DWord	Bit	Description
0	31:21	**Reserved** Access: RO Format: MBZ
	20:0	**Poll Interval** Access: R/W Minimum number of micro-seconds allowed

Semaphore Signal Port

SEMAPHORE_SIGNAL_PORT - Semaphore Signal Port	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02020h-02023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_RCSUNIT
Address:	22020h-22023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_BCSUNIT
Address:	1C0020h-1C0023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT0
Address:	1C4020h-1C4023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT1
Address:	1C8020h-1C8023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VECSUNIT0
Address:	1D0020h-1D0023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT2
Address:	1D4020h-1D4023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT3
Address:	1D8020h-1D8023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VECSUNIT1
Address:	1E0020h-1E0023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT4
Address:	1E4020h-1E4023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT5

SEMAPHORE_SIGNAL_PORT - Semaphore Signal Port

Address:	1E8020h-1E8023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VECSUNIT2

Address:	1F0020h-1F0023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT6

Address:	1F4020h-1F4023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VCSUNIT7

Address:	1F8020h-1F8023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_VECSUNIT3

Address:	1A020h-1A023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_CCSUNIT0

Address:	1C020h-1C023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_CCSUNIT1

Address:	1E020h-1E023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_CCSUNIT2

Address:	26020h-26023h
Name:	SEMAPHORE_SIGNAL_PORT
ShortName:	SEMAPHORE_SIGNAL_PORT_CCSUNIT3

Each engine implements SEMAPHORE_SIGNAL_PORT register for receiving semaphore signal from the scheduler (SW or FW). A write to the SEMAPHORE_SIGNAL_PORT with data as 0xFFFF_FFFF is decoded as semaphore signal by an engine. An engine waiting on un-successful MI_SEMAPHORE_WAIT (signal mode) command will reacquire the semaphore data from memory and re-evaluate the semaphore comparison on receiving the semaphore signal. SEMAPHORE_SIGNAL_PORT register is privileged. Writing to the SEMAPHORE_SIGNAL_PORT of an idle engine (no context) does not trigger any action in HW and is of no use.

DWord	Bit	Description
0	31:0	**Semaphore Signal Value** Access: R/W Format: U32

Semaphore Token

SEMAPHORE_TOKEN - Semaphore Token	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	022B4h-022B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_RCSUNIT_CTX
Address:	222B4h-222B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_BCSUNIT_CTX
Address:	1C02B4h-1C02B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT0_CTX
Address:	1C42B4h-1C42B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT1_CTX
Address:	1C82B4h-1C82B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VECSUNIT0_CTX
Address:	1D02B4h-1D02B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT2_CTX
Address:	1D42B4h-1D42B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT3_CTX
Address:	1D82B4h-1D82B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VECSUNIT1_CTX
Address:	1E02B4h-1E02B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT4_CTX
Address:	1E42B4h-1E42B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT5_CTX

SEMAPHORE_TOKEN - Semaphore Token

Address:	1E82B4h-1E82B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VECSUNIT2_CTX

Address:	1F02B4h-1F02B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT6_CTX

Address:	1F42B4h-1F42B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VCSUNIT7_CTX

Address:	1F82B4h-1F82B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_VECSUNIT3_CTX

Address:	1A2B4h-1A2B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_CCSUNIT0_CTX

Address:	1C2B4h-1C2B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_CCSUNIT1_CTX

Address:	1E2B4h-1E2B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_CCSUNIT2_CTX

Address:	262B4h-262B7h
Name:	SEMAPHORE_TOKEN
ShortName:	SEMAPHORE_TOKEN_CCSUNIT3_CTX

This register holds the Producer Token Number programmed by the SW. Producer Token Number is reported to the GUC by an engine on executing MI_SEMAPHORE_SIGNAL command. SEMAPHORE_TOKEN register is privileged, and context save/restored.

DWord	Bit	Description
0	31:27	**Semaphore Register ID** Access: R/W This field specifies the GuC Semaphore register (Reg 0- 7) to which the update should be directed.
	26:5	**Reserved** Access: R/W Format: PBC

SEMAPHORE_TOKEN - Semaphore Token

	4:0	**Producer Token Number** Access: R/W Format: U5 **Description** This field specifies the bit (31-0) that should be set in the register specified by SEMAPHORE_REG_ID field.

SG AddrRangeforTile0

SG_TILE0_ADDR_RANGE - SG AddrRangeforTile0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1083A0h

The register below captures how this register will be interpreted. This register itself is simply a R/W register with SAI protection.
Definitions of the bits themselves (ie. Lock bit) has no direct impact on this register.
Base and Range of Local memory TILE 0.
Base and Range is in GBs.
In the single Tilemode, Tile0 ADDR_RANGE registers must be valid and Tile 1/2/3 ADDR_RANGE registers must be invalid.
In the two Tilemode, only TILE0 and TILE1 registers must be programmed to be valid and TILE2 and TILE3 registers must be invalid.
In the four Tile ATS mode, all four TILE registers must be programmed to be valid.

DWord	Bit	Description
0	31	**Local Memory Addr Range Lock** Default Value: 0b Access: R/W
	30:15	**SPARE** Default Value: 0b Access: R/W
	14:8	**Local Memory Addr Range** Default Value: 00b Access: R/W Local Memory range (size) in GBs. Local Memory size of 0 - 127GB is supported at 1GB granularity.
	7:1	**Local Memory Addr Base** Default Value: 0000000b Access: R/W Local Memory Base address in GBs. Base Address of 0 - 127GB is supported at 1GB granularity.
	0	**Valid** Default Value: 0 Access: R/W Local Memory Base Address and Range is valid. Range is expected to be non-zero when valid.

SG AddrRangeforTile1

SG_TILE1_ADDR_RANGE - SG AddrRangeforTile1

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1083A4h

The register below captures how this register will be interpreted. This register itself is simply a R/W register with SAI protection.
Definitions of the bits themselves (i.e.. Lock bit) has no direct impact on this register.
Base and Range of Local memory TILE1.
Base and Range is in GBs.
In the single Tilemode, Tile0 ADDR_RANGE registers must be valid and Tile 1/2/3 ADDR_RANGE registers must be invalid.
In the two Tilemode, only TILE0 and TILE1 registers must be programmed to be valid and TILE2 and TILE3 registers must be invalid.
In the four Tile ATS mode, all four TILE registers must be programmed to be valid.

DWord	Bit	Description
0	31	**Local Memory Addr Range Lock** Default Value: 0b Access: R/W
	30:15	**SPARE** Default Value: 0b Access: R/W
	14:8	**Local Memory Addr Range** Default Value: 00b Access: R/W Local Memory range (size) in GBs. Local Memory size of 0 - 127GB is supported at 1GB granularity.
	7:1	**Local Memory Addr Base** Default Value: 0000000b Access: R/W Local Memory Base address in GBs. Base Address of 0 - 127GB is supported at 1GB granularity.
	0	**Valid** Default Value: 0 Access: R/W Local Memory Base Address and Range is valid. Range is expected to be non-zero when valid.

SG AddrRangeforTile2

SG_TILE2_ADDR_RANGE - SG AddrRangeforTile2

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1083A8h

The register below captures how this register will be interpreted. This register itself is simply a R/W register with SAI protection.
Definitions of the bits themselves (i.e.. Lock bit) has no direct impact on this register.
Base and Range of Local memory TILE2
Base and Range is in GBs.
In the single Tilemode, Tile0 ADDR_RANGE registers must be valid and Tile 1/2/3 ADDR_RANGE registers must be invalid.
In the two Tilemode, only TILE0 and TILE1 registers must be programmed to be valid and TILE2 and TILE3 registers must be invalid.
In the four Tile ATS mode, all four TILE registers must be programmed to be valid.

DWord	Bit	Description
0	31	**Local Memory Addr Range Lock** Default Value: 0b Access: R/W
	30:15	**SPARE** Default Value: 0b Access: R/W
	14:8	**Local Memory Addr Range** Default Value: 00b Access: R/W Local Memory range (size) in GBs. Local Memory size of 0 - 127GB is supported at 1GB granularity.
	7:1	**Local Memory Addr Base** Default Value: 0000000b Access: R/W Local Memory Base address in GBs. Base Address of 0 - 127GB is supported at 1GB granularity.
	0	**Valid** Default Value: 0 Access: R/W Local Memory Base Address and Range is valid. Range is expected to be non-zero when valid.

SG AddrRangeforTile3

SG_TILE3_ADDR_RANGE - SG AddrRangeforTile3

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1083ACh

The register below captures how this register will be interpreted. This register itself is simply a R/W register with SAI protection.
Definitions of the bits themselves (ie. Lock bit) has no direct impact on this register.
Base and Range of Local memory TILE3
Base and Range is in GBs.
In the single Tilemode, Tile0 ADDR_RANGE registers must be valid and Tile 1/2/3 ADDR_RANGE registers must be invalid.
In the two Tilemode, only TILE0 and TILE1 registers must be programmed to be valid and TILE2 and TILE3 registers must be invalid.
In the four Tile ATS mode, all four TILE registers must be programmed to be valid.

DWord	Bit	Description
0	31	**Local Memory Addr Range Lock** Default Value: 0b Access: R/W
	30:15	**SPARE** Default Value: 0b Access: R/W
	14:8	**Local Memory Addr Range** Default Value: 00b Access: R/W Local Memory range (size) in GBs. Local Memory size of 0 - 127GB is supported at 1GB granularity.
	7:1	**Local Memory Addr Base** Default Value: 0000000b Access: R/W Local Memory Base address in GBs. Base Address of 0 - 127GB is supported at 1GB granularity.
	0	**Valid** Default Value: 0 Access: R/W Local Memory Base Address and Range is valid. Range is expected to be non-zero when valid.

SGunit Internal Interrupt Port

GT_TO_SGUNIT_INTR_PORT - SGunit Internal Interrupt Port

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 190000h

Gunit internal interrupt port that is used by engines to communicate interrupts

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:27	**Virtual Function Number** Default Value: 000b Access: R/W _Custom_GTIReset: BUS VF Number
	26	**Reserved** Access: RO Format: MBZ
	25:20	**Engine Instance ID** Default Value: 000000b Access: R/W _Custom_GTIReset: BUS Engine Instance ID format is defined in structure "Engine ID Definition
	19	**Reserved** Access: RO Format: MBZ
	18:16	**Engine Class ID** Default Value: 000b Access: R/W _Custom_GTIReset: BUS Engine class ID format is defined in structure "Engine ID Definition

GT_TO_SGUNIT_INTR_PORT - SGunit Internal Interrupt Port

	15:0	**Engine Interrupt** Default Value: 0000h Access: R/W _Custom_GTIReset: BUS Format is specific to the engine that is sending the interrupt. Format is defined in structure Engine Interrupt Vector (where engine is Blitter/G-Unit/GTPM/GuC/Render Engine/Video Decoder/VideoEnhancement).

SGunit Posted Queue Head

SGUNIT_PQUEUE_HEAD - SGunit Posted Queue Head		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
CrashLogSaved:	true	
CrashLogVisibility:	cspec	
Address:	00FF4h	
DWord	**Bit**	**Description**
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**SGunit Posted Queue Head Pointer** Default Value: 00000b Access: R/W Head pointer for SGunit 16 deep posted port FIFO. Incremented by MGSR on posted write to SGunit.

SGunit Posted Queue Tail

SGUNIT_PQUEUE_TAIL - SGunit Posted Queue Tail	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
CrashLogSaved:	true
CrashLogVisibility:	cspec
Address:	00FF0h

DWord	Bit	Description
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**SGunit Posted Queue Tail Pointer** Default Value: 10000b Access: R/W Tail pointer for SGunit 16 deep posted port FIFO.

SHOTPLUG_CTL_DDI

SHOTPLUG_CTL_DDI

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	C4030h-C4033h
Name:	South Hot Plug Control for DDI
ShortName:	SHOTPLUG_CTL_DDI
Reset:	soft

The status fields indicate the hot plug detect status on each DDI combo PHY port.
When HPD is enabled and either a long or short pulse is detected for a port, one of the status bits will set and the hotplug IIR will be set (if unmasked in the IMR). The status bits are sticky bits, cleared by writing 1s to the bits.

Each HPD pin can be configured as an input or output. The HPD status function will only work when the pin is configured as an input. The HPD Output Data function will only work when the HPD pin is configured as an output.

The short pulse duration is programmed in SHPD_PULSE_CNT.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15	**DDID HPD Enable** Access: R/W 0b – Disable 1b – Enable
	14	**DDID HPD Output Data** Access: R/W 0b – Drive 0 1b – Drive 1
	13:12	**DDID HPD Status** Access: R/WC 00b – Hot plug event not detected

SHOTPLUG_CTL_DDI

		01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected
	11	**DDIC HPD Enable** Access: R/W 0b: Disable 1b: Enable
	10	**DDIC HPD Output Data** Access: R/W 0b: Drive 0 1b: Drive 1
	9:8	**DDIC HPD Status** Access: R/WC 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected 11b: Short and long pulses detected
	7	**DDIB HPD Enable** Access: R/W 0b: Disable 1b: Enable
	6	**DDIB HPD Output Data** Access: R/W 0b: Drive 0 1b: Drive 1

SHOTPLUG_CTL_DDI

	5:4	**DDIB HPD Status** Access: R/WC Value: 00b — Hot plug event not detected Value: 01b — Short pulse detected Value: 10b — Long pulse detected Value: 11b — Short and long pulses detected
	3	**DDIA HPD Enable** Access: R/W Value: 0b — Disable Value: 1b — Enable
	2	**DDIA HPD Output Data** Access: R/W Value: 0b — Drive 0 Value: 1b — Drive 1
	1:0	**DDIA HPD Status** Access: R/WC Value: 00b — Hot plug event not detected Value: 01b — Short pulse detected Value: 10b — Long pulse detected Value: 11b — Short and long pulses detected

SHOTPLUG_CTL_TC

SHOTPLUG_CTL_TC

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	C4034h-C4037h
Name:	South Hot Plug Control for TypeC
ShortName:	SHOTPLUG_CTL_TC
Reset:	soft

The status fields indicate the hot plug detect status on each type C port when using non-type C connectors (legacy or static configuration).
When HPD is enabled and either a long or short pulse is detected for a port, one of the status bits will set and the hotplug IIR will be set (if unmasked in the IMR). The status bits are sticky bits, cleared by writing 1s to the bits.

The short pulse duration is programmed in SHPD_PULSE_CNT.

DWord	Bit	Description
0	31:4	**Reserved** Access: RO Format: MBZ
	3	**TC1 HPD Enable** Access: R/W 0b: Disable 1b: Enable
	2	**TC1 HPD Output Data** Access: R/W 0b: Drive 0 1b: Drive 1
	1:0	**TC1 HPD Status** Access: R/WC 00b: Hot plug event not detected 01b: Short pulse detected 10b: Long pulse detected

SHOTPLUG_CTL_TC			
		11b	Short and long pulses detected

SHPD_FILTER_CNT

SHPD_FILTER_CNT	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	C4038h-C403Bh
Name:	South HPD Filter count
ShortName:	SHPD_FILTER_CNT
Reset:	global

This register must be programmed properly before enabling HPD detection.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16:0	**HPD Filter Count** Default Value: 001F2h 500 microseconds Access: R/W These bits define the duration of the filter for HPD. The value is the number of microseconds minus 2.

SHPD_PULSE_CNT

SHPD_PULSE_CNT	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	C4050h-C4053h
Name:	South HPD Pulse Count DDIA
ShortName:	SHPD_PULSE_CNT_DDIA
Reset:	global
Address:	C4054h-C4057h
Name:	South HPD Pulse Count DDIB
ShortName:	SHPD_PULSE_CNT_DDIB
Reset:	global
Address:	C4058h-C405Bh
Name:	South HPD Pulse Count DDIC
ShortName:	SHPD_PULSE_CNT_DDIC
Reset:	global
Address:	C405Ch-C405Fh
Name:	South HPD Pulse Count DDID
ShortName:	SHPD_PULSE_CNT_DDID
Reset:	global
Address:	C4070h-C4073h
Name:	South HPD Pulse Count TypeC Port1
ShortName:	SHPD_PULSE_CNT_TC1
Reset:	global

This register must be programmed properly before enabling hotplug detection.

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16:0	**ShortPulse Count** Access: R/W These bits define the duration of the pulse defined as a short pulse for hotplug detection. The value is the number of microseconds minus 2. Value: 007CEh — Name: 2,000 microseconds for DisplayPort **[Default]** Value: 1869Eh — Name: 100,000 microseconds for HDMI or DVI

Slice 0 BONUS1 Reg

SL0SPCBONUS1 - Slice 0 BONUS1 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24194h
Clock Gating Messages Register	

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SL0SPCBONUS1 - Slice 0 BONUS1 Reg

	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 BONUS2 Reg

SL0SPCBONUS2 - Slice 0 BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24198h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SL0SPCBONUS2 - Slice 0 BONUS2 Reg

	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 PGFET control register with lock

SL0SPCPFETCTL - Slice 0 PGFET control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24188h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 0 PGFETCTL register are R/W 1 = All bits of Slice 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

SL0SPCPFETCTL - Slice 0 PGFET control register with lock

3'b010: 160ns
3'b011: 240ns
3'b100: 320ns
3'b101: 480ns
3'b110: 640ns
3'b111: 1280ns

18:16 **Strobe pulse period**

Access:	R/W Lock
_Custom_GTIReset:	BUS

Time period b/w two adjacent strobes to the primary FETs
3'b000: 10ns (or 1 bclk)
3'b001: 20ns (or 2 bclk)
3'b010: 30ns (or 3 bclk)
3'b111: 80ns (or 8 bclk)

Value	Name
011b	**[Default]**

15:0 **PFET Ladder Step Sequence**

Access:	R/W Lock
_Custom_GTIReset:	BUS

PFET Ladder STEP sequence
The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage.
The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0]
Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal.
15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15.
15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped.
15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped.
15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Value	Name
1111111111111111b	**[Default]**

Slice 0 Power Context Save request

SL0PGCTXREQ - Slice 0 Power Context Save request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24184h	
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Slice 0 Power Down FSM control register with lock

SL0SPCPOWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24190h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 0 POWERDNFSMCTL register are R/W 1 = All bits of Slice 0 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e., firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e., don't firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

SL0SPCPOWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

SL0SPCPOWERDNFSMCTL - Slice 0 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Slice 0 Power Gate Control Request

SL0PGCTLREQ - Slice 0 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24180h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 0 Power on FSM control register with lock

SL0SPCPOWERUPFSMCTL - Slice 0 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2418Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 0 POWERUPFSMCTL register are R/W 1 = All bits of Slice 0 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets

SL0SPCPOWERUPFSMCTL - Slice 0 Power on FSM control register with lock

		1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Slice 0 SubSlice 0 PGFET control register with lock

SSM0SPCPFETCTL - Slice 0 SubSlice 0 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24408h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 101b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns

SSM0SPCPFETCTL - Slice 0 SubSlice 0 PGFET control register with lock

		3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock _Custom_GTIReset: BUS Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock _Custom_GTIReset: BUS PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be ‘1; A ‘0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Slice 0 SubSlice 1 PGFET control register with lock

SSM1SPCPFETCTL - Slice 0 SubSlice 1 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24488h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 101b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns

SSM1SPCPFETCTL - Slice 0 SubSlice 1 PGFET control register with lock

		3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock _Custom_GTIReset: BUS Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock _Custom_GTIReset: BUS PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Slice 0 SubSlice 2 PGFET control register with lock

SSM2SPCPFETCTL - Slice 0 SubSlice 2 PGFET control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24508h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of PGFETCTL register are R/W 1 = All bits of PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: RO _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 101b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns

SSM2SPCPFETCTL - Slice 0 SubSlice 2 PGFET control register with lock

		3'b001: 80ns 3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock _Custom_GTIReset: BUS Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 23ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock _Custom_GTIReset: BUS PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Slice 1 - 5 BONUS1 Reg

SL15SPCBONUS1 - Slice 1 - 5 BONUS1 Reg

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24214h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SL15SPCBONUS1 - Slice 1 - 5 BONUS1 Reg

	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 1 - 5 BONUS2 Reg

SL15SPCBONUS2 - Slice 1 - 5 BONUS2 Reg

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24218h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SL15SPCBONUS2 - Slice 1 - 5 BONUS2 Reg

	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 1 - 5 PGFET control register with lock

SL15SPCPFETCTL - Slice 1 - 5 PGFET control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24208h

DWord	Bit	Description
0	31	**PFET Control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 0 PGFETCTL register are R/W 1 = All bits of Slice 0 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:24	**Reserved** Access: RO Format: MBZ
	23	**Power Well Status** Access: R/WC _Custom_GTIReset: BUS strbpulsprdwered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	22	**Powergood timer error** Access: R/WC _Custom_GTIReset: BUS 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	21:19	**Delay from enabling secondary PFETs to power good.** Default Value: 111b Access: R/W Lock _Custom_GTIReset: BUS Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns

SL15SPCPFETCTL - Slice 1 - 5 PGFET control register with lock

		3'b010: 160ns 3'b011: 240ns 3'b100: 320ns 3'b101: 480ns 3'b110: 640ns 3'b111: 1280ns
	18:16	**Strobe pulse period** Default Value: 011b Access: R/W Lock _Custom_GTIReset: BUS Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)
	15:0	**PFET Ladder Step Sequence** Default Value: 1111111111111111b Access: R/W Lock _Custom_GTIReset: BUS PFET Ladder STEP sequence The PFET ladder has 16 steps, each represented by its corresponding bit in pfetlddrstepseq[15:0]. If the bit location is set, it means we must step on that ladder stage before we go to the next stage. The SPC controller will step through all the steps with asserted bits periodically with period equal to strbpulsprd[2:0] Programming Rule: pfetldrstepseq[15] and pfetldrstepseq[0] must be '1; A '0 setting for these bits is illegal. 15'FFFFh: Ladder step (ladder_sel) goes 0, 1, 2, ?.15. 15'FFF1h: Ladder step goes 0, 4, 5, 6,?15; Steps 1, 2, 3 are skipped. 15'D555h: Ladder step goes 0, 2, 4, 6, 8, 10, 12, 14, 15; Steps 1, 3, 5, 7, 9, 11, 13 are skipped. 15'80001h: Ladder step goes 0, 15; Steps 1, 2, 3, 4, ?14 are skipped.

Slice 1 - 5 Power Down FSM control register with lock

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24210h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 1 POWERDNFSMCTL register are R/W 1 = All bits of Slice 1 POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e dont firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock

10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

SL15SPCPOWERDNFSMCTL - Slice 1 - 5 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

Slice 1 - 5 Power Gate Control Request

SL15PGCTLREQ - Slice 1 - 5 Power Gate Control Request		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24200h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

Slice 1 -5 Power on FSM control register with lock

SL15SPCPOWERUPFSMCTL - Slice 1 -5 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2420Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of Slice 1 POWERUPFSMCTL register are R/W 1 = All bits of Slice 1 POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets

SL15SPCPOWERUPFSMCTL - Slice 1 -5 Power on FSM control register with lock

		1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

Slice Common Power Context Save request

SCPCTXSAVEREQ - Slice Common Power Context Save request

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 08140h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO _Custom_GTIReset: BUS Reserved
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Slice Context 1 NODE CCS Mode

NODE_CCS - Slice Context 1 NODE CCS Mode

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	07FF8h
Name:	Slice Context 1 NODE CCS Mode
ShortName:	NODE_CCS
Access:	WO

Context 1 for each DSS in a slice is assigned an active Compute CSID and an EXID value by CS when the context is started. NODE supplies both the non-pipelined state and the EXID for the active CCSID to SARB units that use that state.
Context 0 for each DSS always uses EXID 0.

DWord	Bit	Description
0	31:6	**Reserved** Access: RO Format: MBZ
	5:3	**Active State** Access: WO Format: U3 CS sends the non-pipelined state for every Compute CS to each slice that the context can run on. When the HW binds a slice to a specific CCS context, then that context's non-pipelined state is selected as active by setting this control to that CCSID, and SARB uses those state values available to the SARB unit. 0 – CCS0 1 – CCS1 2 – CCS2 3 – CCS3 7 – NONE **[Default]**
	2:0	**Context 1 EXID** Access: WO Format: U3 [0-7]

Slice unit Level Clock Gating Control 94D0

SCCGCTL94D0 - Slice unit Level Clock Gating Control 94D0

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	094D0h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:2	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	1	**GCPunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**SMCRunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS SMCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

Slice unit Level Clock Gating Control 94D4

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	094D4h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**SPARE Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**oaal1unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS oaal1unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	29	**ccunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**DAPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

27	**GACBunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

GACBunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

26	**GAFSRRB Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

GAFSRRB Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

25	**GAHSunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

GAHSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

24	**GAPCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

GAPCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

23	**GAPL3unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

GAPL3unit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

22	**GAPSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GAPSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
21	**GAPZunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GAPZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
20	**zarbunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS zarbunit Clock Gating Disable Control
19	**HIZunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HIZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
18	**IZunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
17:15	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

14 **RRU Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

RRU Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

13 **SLCFG Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SLCFG Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12 **NODEDSS Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

NODEDSS Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

11 **NODEX Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

NODEX Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

10 **MSCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

MSCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

9 OAADDRunit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

OAADDRunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

8 OASCREP Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

OASCREP Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

7 Reserved

Access:	R/W
_Custom_GTIReset:	BUS

Reserved

6 RCZunit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

RCZunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

5 Sarbunit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

Sarbunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4

4	**SBEunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SBEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

3	**STCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

STCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

2	**SVLunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SVLunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

1	**WMBE Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

WMBE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

0	**WMFEunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

WMFEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

SCCGCTL94D4 - Slice unit Level Clock Gating Control 94D4		
		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Slice unit Level Clock Gating Control 94D8

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	094D8h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**SFR unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SFR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	30	**SF unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SF unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	29	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	28	**RCU unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RCU unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

27	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
26	**OVR unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS OVR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
25	**HS unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
24	**GS unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
23	**GAFSWRBLK unit Clock Gating Disable wmf** Access: R/W _Custom_GTIReset: BUS GAFSWRBLK unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

22	**GAFSWRBLK unit Clock Gating Disable vf** Access: R/W _Custom_GTIReset: BUS GAFSWRBLK unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
21:19	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
18	**GAFD unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GAFD unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
17	**GAFS unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GAFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
16	**GAFM unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GAFM unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

	Workaround SW is required to disable clock gating to converge timing.
15	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
14	**CLR unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CLR unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
13	**CL unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CL unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
12	**AMFSF unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
11	**AMFSC unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

		Workaround SW is required to disable clock gating to converge timing.
	10	**AMFSD unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS AMFS unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	9:8	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	7	**SFBEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SFBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	5	**LNIunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LNIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94D8 - Slice unit Level Clock Gating Control 94D8

4	**RCPBunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
3	**RCPBEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RCPBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
2	**TDCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS TDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
1	**RAMdft Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RAMdft Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
0	**NOA Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS NOA Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Slice unit Level Clock Gating Control 94DC

SCCGCTL94DC - Slice unit Level Clock Gating Control 94DC

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	094DCh

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:15	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	14	**URBUNIT Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS URBUNIT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	13:4	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	3:0	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved

Slice unit Level Clock Gating Control 94E0

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	094E0h	
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	30	**PSS Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS PSS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**VSR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VSR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**VS Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

27	**VFR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VFR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
26	**VF Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VF Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
25	**TDS Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS TDS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
24	**SVGR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SVGR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
23	**SVG Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SVG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

	Workaround SW is required to disable clock gating to converge timing.
22	**SOL Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SOL Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
21:20	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
19	**OVR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS OVR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
18	**HS Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
17	**GS Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

Workaround
SW is required to disable clock gating to converge timing.

16 CS Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

CS Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

15 SPARE Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

SPARE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14 CPSSunit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

CPSSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

13 PSDunit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

PSDunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12 BCunit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

BCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

11	**MSCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

MSCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

10	**RCPFEunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

RCPFEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

9	**AVSunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

AVSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

8	**Reserved**

Access:	R/W
_Custom_GTIReset:	BUS

Reserved

7	**HIZunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HIZunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

	6	**IZunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	4	**RCZunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**SBEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**STCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS STCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	1	**SVLunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS

SCCGCTL94E0 - Slice unit Level Clock Gating Control 94E0

		SVLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**WMFEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS WMFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

Slice unit Level Clock Gating Control 94E4

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	094E4h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**PCP Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS PCP Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	30	**PCPR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS PCPR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	29	**reserved** Access: R/W _Custom_GTIReset: BUS reserved '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**sdfifo Clock Gating Disable svg** Access: R/W _Custom_GTIReset: BUS sdfifo Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

	Workaround
	SW is required to disable clock gating to converge timing.

27 sdfifo Clock Gating Disable svl

Access:	R/W
_Custom_GTIReset:	BUS

sdfifo Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

26 PSS unit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

PSS Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

25 CARB unit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

CARB Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

24 ZPBE unit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

ZPBE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

23 ZSCBANK unit Clock Gating Disable

Access:	R/W
_Custom_GTIReset:	BUS

ZSCBANK Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

22 **ZSCCOMPUTE unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

ZSCCOMPUTE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

21 **GAFARB unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

GAFARB Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

20 **VSR unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VSR Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19 **VS unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VS Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18 **VFR unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VFR Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

	17	**VFE Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VFE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**VF unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VF Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**URBM unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS URBM Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**TSG unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS TSG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**TETG unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS TETG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

12	**TE unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS TE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
11	**TDS unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS TDS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
10	**TDG unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS TDG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
9	**SVGR unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SVGR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
8	**SVG unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SVG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

		Workaround SW is required to disable clock gating to converge timing.
	7	**SOL unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SOL Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	6	**gwunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS gwunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	5	**psdunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS psdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**hdcunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

SCCGCTL94E4 - Slice unit Level Clock Gating Control 94E4

	3	**cpssunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS cpssunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**besbufunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS besbufunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**sbc Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS sbcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**tdpunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS tdpEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Slice unit Level Clock Gating override during rstflow 94F0

SCMISCCP94F0 - Slice unit Level Clock Gating override during rstflow 94F0		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 094F0h		
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31:0	**ECO Spare Bits** Access: R/W _Custom_GTIReset: BUS Reserved

SLM Correctible Error Count

SLM_ECC_ERROR_CNT - SLM Correctible Error Count		
Register Space:	MMIO: 0/2/0	
Access:	R/W	
Size (in bits):	32	
Address:	0E7F4h	
DWord	**Bit**	**Description**
0	31:0	**ERROR COUNT** Access: R/W This counter indicates number of single bit correctible errors in the SLM of this DSS. The counter saturates at the max value (2^32 -1). The counter can be cleared by GuC or PF KMD. A Message Channel write is sent by TDL to GuC for the first error encountered after the counter is cleared. **Programming Notes** This counter counts correctible ECC errors in the combined Untyped L1 cache and SLM data RAM.

Small Draw Watermark

DRAW_WATERMARK - Small Draw Watermark

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	026C0h-026C3h
Name:	Small Draw Watermark
ShortName:	DRAW_WATERMARK_RCSUNIT_BE_GEOMETRY

Address:	186C0h-186C3h
Name:	Small Draw Watermark
ShortName:	DRAW_WATERMARK_POCSUNIT_BE_GEOMETRY

This register specifies the size of the DRAW in vertices that will be committed without any chance of preemption. If the DRAW is smaller than the watermark, then it allows command streamer to continue to the next command which may help on overall performance in cases where we execute smaller vertex count 3DPRIMITIVE commands.

DWord	Bit	Description
0	31:10	**Reserved** Access: RO Format: MBZ
	9:0	**Vertex Watermark Value** Default Value: 100h Access: R/W Format: U10 **Description** This value is in increments of vertices. If((Instance Count * Vertex Count) > Watermark Value) Then command stream will allow preemption of the 3DPRIMITIVE. Otherwise it will continue the next command with no stalling. This value is in increments of vertices. If((Instance Count * Vertex Count) > Watermark Value) Then command stream will allow preemption of the 3DPRIMITIVE. Otherwise it will continue the next command with no stalling. This value is in increments of Thread Groups. If(Thread Group Count X > Watermark Value) Then command stream will allow preemption of the 3DMESH_1D. Otherwise it will continue the next command with no stalling. This value is in increments of Thread Groups. If(Thread Group Count X * Thread Group Count Y * Thread Group Count Z> Watermark Value) Then command stream will allow preemption of the 3DMESH_3D. Otherwise it will continue the next command with no stalling.

SNP_FILTER_Q_STATUS

SNP_FILTER_Q_STATUS - SNP_FILTER_Q_STATUS	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	00B00h
Name:	SNP_FILTER_Q_STATUS
ShortName:	SNP_FILTER_Q_STATUS
This is a basic register template	

DWord	Bit	Description
0	31	**Reserved**
	30:29	**SF_Q_STATUS_SPARE_BITS_30_29** Access: RO _Custom_GTIReset: BUS
	28:8	**Reserved**
	7:6	**Reserved**
	5:4	**Reserved**
	3:2	**Reserved**
	1:0	**Reserved**

SNPS_PHY_AUX_CNFG

SNPS_PHY_AUX_CNFG - SNPS_PHY_AUX_CNFG	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168180h-168183h
Name:	SNPS_PHY_AUX_CNFG
ShortName:	SNPS_PHY_AUX_CNFG_PORT_A
Reset:	global
Address:	169180h-169183h
Name:	SNPS_PHY_AUX_CNFG
ShortName:	SNPS_PHY_AUX_CNFG_PORT_B
Reset:	global
Address:	16A180h-16A183h
Name:	SNPS_PHY_AUX_CNFG
ShortName:	SNPS_PHY_AUX_CNFG_PORT_C
Reset:	global
Address:	16B180h-16B183h
Name:	SNPS_PHY_AUX_CNFG
ShortName:	SNPS_PHY_AUX_CNFG_PORT_D
Reset:	global
Address:	16C180h-16C183h
Name:	SNPS_PHY_AUX_CNFG
ShortName:	SNPS_PHY_AUX_CNFG_PORT_TC1
Reset:	global

Each display port will have 2 instances of SNPS low speed PHY supporting AUX/I2C for one SNPS high speed PHY.

DWord	Bit	Description
0	31	**AUX mode enable** Access: R/W This bit enables/disables the entire AUX block. To enable AUX mode, set to 1 when ALL_PWR_OK is HIGH. AUXMODE will be driven LOW during PHY power-up This signal is asserted HIGH in response to the PHY asserting ALL_PWR_OK HIGH.

SNPS_PHY_AUX_CNFG - SNPS_PHY_AUX_CNFG

Value	Name
0b	PHY not configured as AUX **[Default]**
1b	PHY configured as AUX

30 **All Power Ok**

Access:	RO

Power OK indicator.
Delayed version of this signal gates AUX mode being set HIGH.
Delay should be greater than maximum supply ramp up time.
This signal indicates that both supplies VPH and DVDD are within a percentage of the supply's settled value.
A value of "1" does not guarantee that power has reached to final value.
SW should delay this signal until the VPH and DVDD power is as fully settled as possible to final value before enabling AUXMODE register bits.

Value	Name
0b	Not within target value **[Default]**
1b	within target value

29:28 **Reserved**

Access:	RO
Format:	MBZ

27 **AUX_DP_DN_SWAP**

Access:	R/W

Controls polarity of AUX data with respect to PADP and PADN.
SW needs to update this bit according to Type-C orientation on the controller side.
TCA on the high speed PHY (Main Link PHY) does not take care of AUX orientation.

Value	Name
0b	PADP positive and PADN negative **[Default]**
1b	PADN positive and PADP negative

26 **NEN_RTERM**

Access:	R/W

Strap signal to enable/disable AUX on-chip termination

Value	Name	Description
0b	Termination is enabled **[Default]**	EnableAUX differential termination, weak pre-bias to a common-mode voltage, and protection for plug transients. Use for all functional modes.
1b	Termination is disabled	Disable on-die termination and weak common-mode drive. Use for pin leakage testing.

25:24 **AUX_VOD_TUNE**

Access:	R/W

Straps to tune AUX Tx differential swing.

SNPS_PHY_AUX_CNFG - SNPS_PHY_AUX_CNFG

Value	Name	Description
00b		-40 mV
01b	**[Default]**	Tunes VOD to 290 mV.
10b		40 mV
11b		Tunes to DP v1.2 to support old monitors.

23:22 **AUX_HYS_TUNE**

Access:	R/W

Straps to tune the hysteresis width of AUX Rx differential-to-single-ended input buffer.

Value	Name	Description
00b		0 mV
01b		20 mV
10b	**[Default]**	30 mV
11b		40 mV

21:0 **Reserved**

Access:	RO
Format:	MBZ

SNPS_PHY_I2C_CNFG

SNPS_PHY_I2C_CNFG - SNPS_PHY_I2C_CNFG

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global

Address:	168184h-168187h
Name:	SNPS_PHY_I2C_CNFG
ShortName:	SNPS_PHY_I2C_CNFG_PORT_A
Reset:	global

Address:	169184h-169187h
Name:	SNPS_PHY_I2C_CNFG
ShortName:	SNPS_PHY_I2C_CNFG_PORT_B
Reset:	global

Address:	16A184h-16A187h
Name:	SNPS_PHY_I2C_CNFG
ShortName:	SNPS_PHY_I2C_CNFG_PORT_C
Reset:	global

Address:	16B184h-16B187h
Name:	SNPS_PHY_I2C_CNFG
ShortName:	SNPS_PHY_I2C_CNFG_PORT_D
Reset:	global

Address:	16C184h-16C187h
Name:	SNPS_PHY_I2C_CNFG
ShortName:	SNPS_PHY_I2C_CNFG_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

Each display port will have 2 instances of SNPS low speed PHY supporting AUX/I2C for one SNPS high speed PHY.
Each port will configure either an AUX register (SNPS_PHY_AUX_CNFG) or an I2C register (SNPS_PHY_I2C_CNFG) but not both.

DWord	Bit	Description
0	31	**I2C mode enable** Access: R/W This bit enables/disables the entire I2C block. To enable I2C mode, set to 1 when ALL_PWR_OK is HIGH.

SNPS_PHY_I2C_CNFG - SNPS_PHY_I2C_CNFG

I2C mode will be driven LOW during PHY power-up
This signal is asserted HIGH in response to the PHY asserting ALL_PWR_OK HIGH.

Value	Name
0b	PHY not configured as I2C **[Default]**
1b	PHY configured as I2C

30 **All Power Ok**

Access:	RO

Power OK indicator.
Delayed version of this signal gates I2C mode being set HIGH.
Delay should be greater than maximum supply ramp up time.
This signal indicates that both supplies VPH and DVDD are within a percentage of the supply's settled value.
A value of "1" does not guarantee that power has reached to final value.
SW should delay this signal until the VPH and DVDD power is as fully settled as possible to final value before enabling I2CMODE register bits.

Value	Name
0b	Not within target value **[Default]**
1b	within target value

29 **I2CPADP_PD**

Access:	R/W

Weak pull down enable signal in I2C mode.
Weak pull down is disabled if I2C_PADP_PD=0 in I2C mode.
This signal must not be high in normal mode.
PADP is weak pull down if I2C_PADP_PD=1 in I2C mode.

Value	Name
0b	Pull down disable **[Default]**
1b	Pull down enable

28 **I2CPADN_PD**

Access:	R/W

Weak pull down enable signal in I2C mode.
Weak pull down is disabled if I2C_PADN_PD=0 in I2C mode.
This signal must not be high in normal mode.
PADN is weak pull down if I2C_PADN_PD=1 in I2C mode.

Value	Name
0b	Pull down disable **[Default]**
1b	Pull down enable

27 **I2C_VIL_VIH_TUNE**

Access:	R/W

This signal is used to improve VIL/VIH value of I2C receiver.

SNPS_PHY_I2C_CNFG - SNPS_PHY_I2C_CNFG

Value	Name	Description
0b	Schmit based **[Default]**	Schimt based receiver is used to improve the VIL/VIH value.
1b	Comparator based	Comparator based receiver is used to improve the VIL/VIH value.

26 **I2C_CTRL**

Default Value:	0b
Access:	R/W

Spare pin I2C mode.

25:0 **Reserved**

Access:	RO
Format:	MBZ

SNPS_PHY_MPLLB_CP

SNPS_PHY_MPLLB_CP - SNPS_PHY_MPLLB_CP

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global

Address:	168000h-168003h
Name:	SNPS_PHY_MPLLB_CP
ShortName:	SNPS_PHY_MPLLB_CP_PORT_A
Reset:	global

Address:	169000h-169003h
Name:	SNPS_PHY_MPLLB_CP
ShortName:	SNPS_PHY_MPLLB_CP_PORT_B
Reset:	global

Address:	16A000h-16A003h
Name:	SNPS_PHY_MPLLB_CP
ShortName:	SNPS_PHY_MPLLB_CP_PORT_C
Reset:	global

Address:	16B000h-16B003h
Name:	SNPS_PHY_MPLLB_CP
ShortName:	SNPS_PHY_MPLLB_CP_PORT_D
Reset:	global

Address:	16C000h-16C003h
Name:	SNPS_PHY_MPLLB_CP
ShortName:	SNPS_PHY_MPLLB_CP_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:25	**dp_mpllb_cp_int** Default Value: 0000101b Access: R/W Integral Charge Pump Control
	24	**Reserved** Access: RO Format: MBZ

SNPS_PHY_MPLLB_CP - SNPS_PHY_MPLLB_CP		
	23:17	**dp_mpllb_cp_int_gs** Default Value: 1000001b Access: R/W Integral Charge Pump "Gear Shift" Control
	16	**Reserved** Access: RO Format: MBZ
	15:9	**dp_mpllb_cp_prop** Default Value: 0101101b Access: R/W Proportional CP control
	8	**Reserved** Access: RO Format: MBZ
	7:1	**dp_mpllb_cp_prop_gs** Default Value: 1111111b Access: R/W Proportional CP in gearshift mode
	0	**Reserved** Access: RO Format: MBZ

SNPS_PHY_MPLLB_DIV

SNPS_PHY_MPLLB_DIV - SNPS_PHY_MPLLB_DIV

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global

Address:	168004h-168007h
Name:	SNPS_PHY_MPLLB_DIV
ShortName:	SNPS_PHY_MPLLB_DIV_PORT_A
Reset:	global

Address:	169004h-169007h
Name:	SNPS_PHY_MPLLB_DIV
ShortName:	SNPS_PHY_MPLLB_DIV_PORT_B
Reset:	global

Address:	16A004h-16A007h
Name:	SNPS_PHY_MPLLB_DIV
ShortName:	SNPS_PHY_MPLLB_DIV_PORT_C
Reset:	global

Address:	16B004h-16B007h
Name:	SNPS_PHY_MPLLB_DIV
ShortName:	SNPS_PHY_MPLLB_DIV_PORT_D
Reset:	global

Address:	16C004h-16C007h
Name:	SNPS_PHY_MPLLB_DIV
ShortName:	SNPS_PHY_MPLLB_DIV_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

The defaults in this register are set for 13.5 GHz link rate and 100 MHz reference clock.

DWord	Bit	Description
0	31	**dp_mpllb_force_en** Default Value: 0b Access: R/W MPLLB force enable. When asserted, MPLLB is forced to be powered up, irrespective of the txX_mpllb_en input.

SNPS_PHY_MPLLB_DIV - SNPS_PHY_MPLLB_DIV

30	**dp_mpllb_div_clk_en** Default Value: 1b Access: R/W MPLLB divide clock enable
29	**dp_mpllb_div5_clk_en** Default Value: 1b Access: R/W Divide by 5 enable. When asserted, mpllb_word_clk output clock is MPLLB frequency divided by 10. When unasserted, mpllb_word_clk is MPLLB freq divided by 8.
28	**dp_mpllb_init_cal_disable** Default Value: 0b Access: R/W MPLLB calibration disable control. Set to 1 to disable MPLLB power-on calibration. Allows invalid PLL configurations. Recommend always setting to 0.
27:26	**dp_mpllb_v2i** Default Value: 11b Access: R/W V2I operating range. Allows configuration of V2I operating range.
25:24	**dp_mpllb_freq_vco** Default Value: 00b Access: R/W MPLLB VCO range control. Controls the desired VCO operating range.
23:16	**dp_mpllb_div_multiplier** Default Value: 00001000b Access: R/W MPLLB output frequency multiplier. Frequency multiplication factor used to generate MPLL (after ref_clk_div2_en and ref_clk_mpll[a,b]_div2_en dividers) Can only be changed when txX_mpll_en inputs for all lanes are de-asserted.
15:11	**Reserved** Access: RO Format: MBZ

SNPS_PHY_MPLLB_DIV - SNPS_PHY_MPLLB_DIV

10 **dp_mpllb_pmix_en**

Default Value:	1b
Access:	R/W

This input functionality is reserved.

9 **dp2_mode**

Access:	R/W

This bit when set indicates DP2.0 mode is operational.

Value	Name
0b	DP2.0 not selected **[Default]**
1b	DP2.0 selected

8 **dp_mpllb_word_div2_en**

Default Value:	1b
Access:	R/W

MPLLB word clock divide by 2 enable. When asserted, the frequency of MPLLB word clock is additionally divided by 2.
Change only when txX_mpllb_en inputs for all lanes are de-asserted.

7:5 **dp_mpllb_tx_clk_div**

Access:	R/W

MPLLB output clock divider's divide ratio.
This signal can only be changed when the TX clocks are disabled within the analog.
This corresponds to the power states P1 and P2.

Value	Name
000b	Divide by 1 **[Default]**
001b	Divide by 2
010b	Divide by 4
011b	Divide by 8
100b	Divide by 3
101b	Divide by 5
110b	Divide by 6
111b	Divide by 0

4:1 **Reserved**

Access:	RO
Format:	MBZ

0 **Reserved**

Access:	R/W

SNPS_PHY_MPLLB_DIV2

SNPS_PHY_MPLLB_DIV2 - SNPS_PHY_MPLLB_DIV2

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global

Address:	16801Ch-16801Fh
Name:	SNPS_PHY_MPLLB_DIV2
ShortName:	SNPS_PHY_MPLLB_DIV2_PORT_A
Reset:	global

Address:	16901Ch-16901Fh
Name:	SNPS_PHY_MPLLB_DIV2
ShortName:	SNPS_PHY_MPLLB_DIV2_PORT_B
Reset:	global

Address:	16A01Ch-16A01Fh
Name:	SNPS_PHY_MPLLB_DIV2
ShortName:	SNPS_PHY_MPLLB_DIV2_PORT_C
Reset:	global

Address:	16B01Ch-16B01Fh
Name:	SNPS_PHY_MPLLB_DIV2
ShortName:	SNPS_PHY_MPLLB_DIV2_PORT_D
Reset:	global

Address:	16C01Ch-16C01Fh
Name:	SNPS_PHY_MPLLB_DIV2
ShortName:	SNPS_PHY_MPLLB_DIV2_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:18	**hdmi_mpllb_hdmi_pixel_clk_div** Default Value: 00b Access: R/W Adjusts hdmi_mpllb_hdmi_pixel_clk to account for color depth. hdmi_mpllb_hdmi_pixel_clk = (mpllb_ana_hdmi_hdmi_div_clk / hdmi_mpllb_hdmi_pixel_clk_div).

SNPS_PHY_MPLLB_DIV2 - SNPS_PHY_MPLLB_DIV2

	17:15	**hdmi_mpllb_hdmi_div** Default Value: 000b Access: R/W HDMI divider clock selector for MPLLB.
	14:12	**dp_ref_clk_mpllb_div** Default Value: 010b Access: R/W MPLLB reference clock divider control. The reference clock used for MPLLB calibration and locking can be divided by 2. Hence the total division ratio from the input reference clock is 1, 2 or 4.
	11:0	**dp_mpllb_mulitplier** Default Value: 1FCh Access: R/W MPLLB frequency multiplier control. Multiplies the reference clock. (See the MPLL Feedback Divider Ratio(N) Configuration table. The ref clock used by the MPLLB are generated after applying ref_clk_mpllbdiv[2:0] division of the ref_pad_clk or ref_alt_clk.

SNPS_PHY_MPLLB_FRACN1

SNPS_PHY_MPLLB_FRACN1 - SNPS_PHY_MPLLB_FRACN1	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168008h-16800Bh
Name:	SNPS_PHY_MPLLB_FRACN1
ShortName:	SNPS_PHY_MPLLB_FRACN1_PORT_A
Reset:	global
Address:	169008h-16900Bh
Name:	SNPS_PHY_MPLLB_FRACN1
ShortName:	SNPS_PHY_MPLLB_FRACN1_PORT_B
Reset:	global
Address:	16A008h-16A00Bh
Name:	SNPS_PHY_MPLLB_FRACN1
ShortName:	SNPS_PHY_MPLLB_FRACN1_PORT_C
Reset:	global
Address:	16B008h-16B00Bh
Name:	SNPS_PHY_MPLLB_FRACN1
ShortName:	SNPS_PHY_MPLLB_FRACN1_PORT_D
Reset:	global
Address:	16C008h-16C00Bh
Name:	SNPS_PHY_MPLLB_FRACN1
ShortName:	SNPS_PHY_MPLLB_FRACN1_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**dp_mpllb_fracn_en** Default Value: 0b Access: R/W MPLLB fractional mode enable.

SNPS_PHY_MPLLB_FRACN1 - SNPS_PHY_MPLLB_FRACN1

	30	**dp_mpllb_fracn_cfg_update_en** Default Value: 1b Access: R/W MPLLB config latch signal. Should be always set to "1".
	29:16	**Reserved** Access: RO Format: MBZ
	15:0	**dp_mpllb_fracn_den** Default Value: 0001h Access: R/W MPLLB fractional denominator control. Controls MPLLB modulated frequency fractional ratio.

SNPS_PHY_MPLLB_FRACN2

SNPS_PHY_MPLLB_FRACN2 - SNPS_PHY_MPLLB_FRACN2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	16800Ch-16800Fh
Name:	SNPS_PHY_MPLLB_FRACN2
ShortName:	SNPS_PHY_MPLLB_FRACN2_PORT_A
Reset:	global
Address:	16900Ch-16900Fh
Name:	SNPS_PHY_MPLLB_FRACN2
ShortName:	SNPS_PHY_MPLLB_FRACN2_PORT_B
Reset:	global
Address:	16A00Ch-16A00Fh
Name:	SNPS_PHY_MPLLB_FRACN2
ShortName:	SNPS_PHY_MPLLB_FRACN2_PORT_C
Reset:	global
Address:	16B00Ch-16B00Fh
Name:	SNPS_PHY_MPLLB_FRACN2
ShortName:	SNPS_PHY_MPLLB_FRACN2_PORT_D
Reset:	global
Address:	16C00Ch-16C00Fh
Name:	SNPS_PHY_MPLLB_FRACN2
ShortName:	SNPS_PHY_MPLLB_FRACN2_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:16	**dp_mpllb_fracn_rem** Default Value: 0000h Access: R/W MPLLB fractional remainder control. Controls the PLL modulated freqeuncy fractional ratio.

SNPS_PHY_MPLLB_FRACN2 - SNPS_PHY_MPLLB_FRACN2

	15:0	**dp_mpllb_fracn_quot** Default Value: 0000h Access: R/W MPLLB fractional quotient control. Controls the PLL modulated frequency fractional ratio.

SNPS_PHY_MPLLB_SSCEN

SNPS_PHY_MPLLB_SSCEN - SNPS_PHY_MPLLB_SSCEN

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global

Address:	168014h-168017h
Name:	SNPS_PHY_MPLLB_SSCEN
ShortName:	SNPS_PHY_MPLLB_SSCEN_PORT_A
Reset:	global

Address:	169014h-169017h
Name:	SNPS_PHY_MPLLB_SSCEN
ShortName:	SNPS_PHY_MPLLB_SSCEN_PORT_B
Reset:	global

Address:	16A014h-16A017h
Name:	SNPS_PHY_MPLLB_SSCEN
ShortName:	SNPS_PHY_MPLLB_SSCEN_PORT_C
Reset:	global

Address:	16B014h-16B017h
Name:	SNPS_PHY_MPLLB_SSCEN
ShortName:	SNPS_PHY_MPLLB_SSCEN_PORT_D
Reset:	global

Address:	16C014h-16C017h
Name:	SNPS_PHY_MPLLB_SSCEN
ShortName:	SNPS_PHY_MPLLB_SSCEN_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

Defaults of this register are adjusted for 13.5G link rate with 100 MHz reference clock.

DWord	Bit	Description
0	31	**dp_mpllb_ssc_en** Access: R/W SSC enable. Turns on SSC on mpllb_div_clk output. Change only when txX_mpllb_en is disabled. 0b – Disable 1b – Enable **[Default]**

SNPS_PHY_MPLLB_SSCEN - SNPS_PHY_MPLLB_SSCEN

	30	**dp_mpllb_ssc_up_spread** Access: R/W SSC profile control. Value: 0b — **[Default]** Value: 1b
	29:10	**dp_mpllb_ssc_peak** Default Value: 1370Ah Access: R/W SSC peak control. Controls the PPM shift amplitude of the SSC profile.
	9:0	**Reserved** Access: RO Format: MBZ

SNPS_PHY_MPLLB_SSCSTEP

SNPS_PHY_MPLLB_SSCSTEP - SNPS_PHY_MPLLB_SSCSTEP

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global

Address:	168018h-16801Bh
Name:	SNPS_PHY_MPLLB_SSCSTEP
ShortName:	SNPS_PHY_MPLLB_SSCSTEP_PORT_A
Reset:	global

Address:	169018h-16901Bh
Name:	SNPS_PHY_MPLLB_SSCSTEP
ShortName:	SNPS_PHY_MPLLB_SSCSTEP_PORT_B
Reset:	global

Address:	16A018h-16A01Bh
Name:	SNPS_PHY_MPLLB_SSCSTEP
ShortName:	SNPS_PHY_MPLLB_SSCSTEP_PORT_C
Reset:	global

Address:	16B018h-16B01Bh
Name:	SNPS_PHY_MPLLB_SSCSTEP
ShortName:	SNPS_PHY_MPLLB_SSCSTEP_PORT_D
Reset:	global

Address:	16C018h-16C01Bh
Name:	SNPS_PHY_MPLLB_SSCSTEP
ShortName:	SNPS_PHY_MPLLB_SSCSTEP_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

Defaults of this register are adjusted for 13.5G link rate with 100 MHz reference clock.

DWord	Bit	Description
0	31:11	**dp_mpllb_ssc_stepsize** Default Value: 19151h Access: R/W SSC step size. Controls the SSC profile step.

SNPS_PHY_MPLLB_SSCSTEP - SNPS_PHY_MPLLB_SSCSTEP		
	10:0	**Reserved** Access: RO Format: MBZ

SNPS_PHY_MPLLB_STATUS

SNPS_PHY_MPLLB_STATUS - SNPS_PHY_MPLLB_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168010h-168013h
Name:	SNPS_PHY_MPLLB_STATUS
ShortName:	SNPS_PHY_MPLLB_STATUS_PORT_A
Reset:	global
Address:	169010h-169013h
Name:	SNPS_PHY_MPLLB_STATUS
ShortName:	SNPS_PHY_MPLLB_STATUS_PORT_B
Reset:	global
Address:	16A010h-16A013h
Name:	SNPS_PHY_MPLLB_STATUS
ShortName:	SNPS_PHY_MPLLB_STATUS_PORT_C
Reset:	global
Address:	16B010h-16B013h
Name:	SNPS_PHY_MPLLB_STATUS
ShortName:	SNPS_PHY_MPLLB_STATUS_PORT_D
Reset:	global
Address:	16C010h-16C013h
Name:	SNPS_PHY_MPLLB_STATUS
ShortName:	SNPS_PHY_MPLLB_STATUS_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30	**dp_tx3_req** Default Value: 0b Access: R/WC DP TX0 lane request status indicator. Asserted when HW controls REQ/ACK handshake with PHY. SW should not initiate any REQ/ACK handshake with PHY while HW is in PSR.

SNPS_PHY_MPLLB_STATUS - SNPS_PHY_MPLLB_STATUS

	29	**dp_tx3_ack** Default Value: 0b Access: R/WC indicates the requested TX setting is completed. Stays asserted until the request input is de-asserted. Also asserts during lane reset. An ack can assert following a hardware generated TX lane request.
	28	**dp_tx2_req** Default Value: 0b Access: R/WC DP TX0 lane request status indicator. Asserted when HW controls REQ/ACK handshake with PHY. SW should not initiate any REQ/ACK handshake with PHY while HW is in PSR.
	27	**dp_tx2_ack** Default Value: 0b Access: R/WC indicates the requested TX setting is completed. Stays asserted until the request input is de-asserted. Also asserts during lane reset. An ack can assert following a hardware generated TX lane request.
	26	**dp_tx1_req** Default Value: 0b Access: R/WC DP TX0 lane request status indicator. Asserted when HW controls REQ/ACK handshake with PHY. SW should not initiate any REQ/ACK handshake with PHY while HW is in PSR.
	25	**dp_tx1_ack** Default Value: 0b Access: R/WC indicates the requested TX setting is completed. Stays asserted until the request input is de-asserted. Also asserts during lane reset. An ack can assert following a hardware generated TX lane request.
	24	**dp_tx0_req** Default Value: 0b Access: R/WC DP TX0 lane request status indicator. Asserted when HW controls REQ/ACK handshake with PHY. SW should not initiate any REQ/ACK handshake with PHY while HW is in PSR.

SNPS_PHY_MPLLB_STATUS - SNPS_PHY_MPLLB_STATUS

	23	**dp_tx0_ack** Default Value: 0b Access: R/WC indicates the requested TX setting is completed. Stays asserted until the request input is de-asserted. Also asserts during lane reset. An ack can assert following a hardware generated TX lane request.
	22:4	**Reserved** Access: RO Format: MBZ
	3:0	**hw_seq_state** Access: RO This bit indicates the current HW sequencer state.

Value	Name
0000b	PHY_INIT **[Default]**
0001b	PLL_OFF
0010b	REQ_PLL_ON
0011b	PLL_ON_P3
0100b	LANE_RST
0101b	REQ_P0
0110b	LANES_OUT_OF_RST_P0
0111b	REQ_P3
1000b	WAIT_FOR_PLL_OFF_ACK
1001b	DRIVE_DPALT_DISABLE_SIGNALS
1010b	REQ_PSR_PSTATE
1011b	PSR_STATE

SNPS_PHY_REF_CONTROL

SNPS_PHY_REF_CONTROL - SNPS_PHY_REF_CONTROL	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168188h-16818Bh
Name:	SNPS_PHY_REF_CONTROL
ShortName:	SNPS_PHY_REF_CONTROL_PORT_A
Reset:	global
Address:	169188h-16918Bh
Name:	SNPS_PHY_REF_CONTROL
ShortName:	SNPS_PHY_REF_CONTROL_PORT_B
Reset:	global
Address:	16A188h-16A18Bh
Name:	SNPS_PHY_REF_CONTROL
ShortName:	SNPS_PHY_REF_CONTROL_PORT_C
Reset:	global
Address:	16B188h-16B18Bh
Name:	SNPS_PHY_REF_CONTROL
ShortName:	SNPS_PHY_REF_CONTROL_PORT_D
Reset:	global
Address:	16C188h-16C18Bh
Name:	SNPS_PHY_REF_CONTROL
ShortName:	SNPS_PHY_REF_CONTROL_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:27	**ref_range** Access: R/W Specifies the frequency range of the input reference clock (post ref_clk_div2_en division if any). Any change in this input must be done while dp_ref_clken=0 and ss_ref_clken=0 and phy_reset=1 or be followed by phy_reset assertion before using the phy. This value is ignored for the TC1 instance of this register. The type-C subsystem has a separate register to control it.

SNPS_PHY_REF_CONTROL - SNPS_PHY_REF_CONTROL

Value	Name	Description
00000b		19.2 MHz - 26.0 MHz
00001b		26.1 MHz - 52.0 MHz
00010b		52.1 MHz - 78.0 MHz
00011b	**[Default]**	78.1 MHz - 104.0 MHz
00100b		104.1 MHz - 130.0 MHz
00101b		130.1 MHz - 156.0 MHz
00110b		156.1 MHz - 182.0 MHz
00111b		182.1 MHz - 200.0 MHz

26 **dp_ref_clk_en**

Access:	R/W

This bit when set enables the MPLLB reference clock for the PHY.
This bit must remain de-asserted until the reference clock is running at the appropriate frequency.
The clock must be glitch-free at the primary reference clock input to the PHY.
PHY CR interface is not available during the time reference clock is suspended.

Value	Name
0b	Ref clock is not enabled **[Default]**
1b	Ref clock is enabled

25 **dp_ref_clk_req**

Access:	RO

The purpose of this bit is to request reference clock to the PHY.
Reference clock to the PHY cannot be disabled when this bit is set.

Value	Name
0b	Ref clock can be disabled **[Default]**
1b	Ref clock cannot be disabled

24 **refclk mux select**

Access:	RO

The purpose of this bit is read the current status of reference clock mux select for the type-C PHY.
This bit will be set by SoC for 5th (type-C PORT_TC1) DE Shim instance only, and comes from the strap that selects between native and type-C connectivity for the PHY.

Value	Name	Description
1b	100 MHz	PHY is configured for native DP and HDMI connections.
0b	38.4 MHz **[Default]**	PHY is configured for type-C connections.

23:16 **Reserved**

Access:	RO
Format:	MBZ

SNPS_PHY_REF_CONTROL - SNPS_PHY_REF_CONTROL

15 **Filter PLL Enable**

Access:	R/W

Default of this register bit is set to '1' so that all Combo PHY PLLs will pick up filtered reference clock automatically.
SoC will fan out this register to all 4 combo PHY instances.
XCU unit has mux selection before the filter. Note that filter is always selected.
In filter bypass output reference clock will be 38.4 MHz.

Value	Name	Description
0b	Disable	Filter PLL disabled.
1b	Enable	Filter PLL enabled.

14 **Filter PLL Lock**

Access:	RO

This fields indicates the status of the PLL Lock.

Value	Name
0b	Not locked or not enabled
1b	Locked

13 **Filter PLL input mux select**

Access:	R/W

For additional details, please review genlock page.
This field selects the PLL input mux between internal 38.4 MHz crystal and external genlock reference.
During reset, the genlock filter PLL locks with 38.4 MHz crystal because genlock won't be enabled until after boot.
XCU unit has mux selection before the filter. Note that filter is always selected.
When genlock is started after boot:the driver has to switch over to the genlock reference (secondary). Refer to the table below.

Mode	Reference clock	secondary genlock mux select	PLL output
Non genlock	38.4 MHz crystal	0	100 MHz
genlock primary	38.4 MHz crystal	0	100 MHz
genlock secondary	external genlock reference	1	100 MHz

Value	Name
0b	Non-genlock **[Default]**
1b	genlock

12:0 **Reserved**

Access:	RO
Format:	MBZ

SNPS_PHY_TX_COMMON

SNPS_PHY_TX_COMMON - SNPS_PHY_TX_COMMON

Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global

Address:	168100h-168103h
Name:	SNPS_PHY_TX_COMMON
ShortName:	SNPS_PHY_TX_COMMON_PORT_A
Reset:	global

Address:	169100h-169103h
Name:	SNPS_PHY_TX_COMMON
ShortName:	SNPS_PHY_TX_COMMON_PORT_B
Reset:	global

Address:	16A100h-16A103h
Name:	SNPS_PHY_TX_COMMON
ShortName:	SNPS_PHY_TX_COMMON_PORT_C
Reset:	global

Address:	16B100h-16B103h
Name:	SNPS_PHY_TX_COMMON
ShortName:	SNPS_PHY_TX_COMMON_PORT_D
Reset:	global

Address:	16C100h-16C103h
Name:	SNPS_PHY_TX_COMMON
ShortName:	SNPS_PHY_TX_COMMON_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30	**dp_tx_invert** Default Value: 0b Access: R/W Invert logical sense of _p and _m signals. This is only polarity inversion.

SNPS_PHY_TX_COMMON - SNPS_PHY_TX_COMMON

	29:27	**dp_tx_term_ctrl** Default Value: 010b Access: R/W TX termination control.
	26	**dp_tx_vregdrv_byp** Default Value: 0b Access: R/W Bypasses the DP TX regulator and uses VPTX directly.
	25:0	**Reserved** Access: RO Format: MBZ

SNPS_PHY_TX_EQ

SNPS_PHY_TX_EQ - SNPS_PHY_TX_EQ	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168300h-168303h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN0_PORT_A
Reset:	global
Address:	168310h-168313h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN1_PORT_A
Reset:	global
Address:	168320h-168323h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN2_PORT_A
Reset:	global
Address:	168330h-168333h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN3_PORT_A
Reset:	global
Address:	169300h-169303h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN0_PORT_B
Reset:	global
Address:	169310h-169313h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN1_PORT_B
Reset:	global
Address:	169320h-169323h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN2_PORT_B
Reset:	global
Address:	169330h-169333h

SNPS_PHY_TX_EQ - SNPS_PHY_TX_EQ	
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN3_PORT_B
Reset:	global
Address:	16A300h-16A303h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN0_PORT_C
Reset:	global
Address:	16A310h-16A313h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN1_PORT_C
Reset:	global
Address:	16A320h-16A323h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN2_PORT_C
Reset:	global
Address:	16A330h-16A333h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN3_PORT_C
Reset:	global
Address:	16B300h-16B303h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN0_PORT_D
Reset:	global
Address:	16B310h-16B313h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN1_PORT_D
Reset:	global
Address:	16B320h-16B323h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN2_PORT_D
Reset:	global
Address:	16B330h-16B333h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN3_PORT_D
Reset:	global
Address:	16C300h-16C303h

SNPS_PHY_TX_EQ - SNPS_PHY_TX_EQ

Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN0_PORT_TC1
Reset:	global

Address:	16C310h-16C313h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN1_PORT_TC1
Reset:	global

Address:	16C320h-16C323h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN2_PORT_TC1
Reset:	global

Address:	16C330h-16C333h
Name:	SNPS_PHY_TX_EQ
ShortName:	SNPS_PHY_TX_EQ_LN3_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**dp_tx_bypass_eq_calc** Default Value: 0b Access: R/W bypass eq calculated values.
	30:24	**Reserved** Access: RO Format: MBZ
	23:18	**dp_tx_eq_main** Default Value: 000000b Access: R/W main EQ level adj.
	17:16	**Reserved** Access: RO Format: MBZ
	15:10	**dp_tx_eq_post** Default Value: 000000b Access: R/W post EQ level adj.

SNPS_PHY_TX_EQ - SNPS_PHY_TX_EQ		
	9:8	**Reserved** Access: RO Format: MBZ
	7:2	**dp_tx_eq_pre** Default Value: 000000b Access: R/W pre EQ level adj.
	1:0	**Reserved** Access: RO Format: MBZ

SNPS_PHY_TX_REQ

SNPS_PHY_TX_REQ - SNPS_PHY_TX_REQ	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168200h-168203h
Name:	SNPS_PHY_TX_REQ
ShortName:	SNPS_PHY_TX_REQ_PORT_A
Reset:	global
Address:	169200h-169203h
Name:	SNPS_PHY_TX_REQ
ShortName:	SNPS_PHY_TX_REQ_PORT_B
Reset:	global
Address:	16A200h-16A203h
Name:	SNPS_PHY_TX_REQ
ShortName:	SNPS_PHY_TX_REQ_PORT_C
Reset:	global
Address:	16B200h-16B203h
Name:	SNPS_PHY_TX_REQ
ShortName:	SNPS_PHY_TX_REQ_PORT_D
Reset:	global
Address:	16C200h-16C203h
Name:	SNPS_PHY_TX_REQ
ShortName:	SNPS_PHY_TX_REQ_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31:30	**Lane disable power state in PSR** Default Value: 11b Access: R/W This register field defines power state when lane is disabled in PSR cases. Shim HW uses this power state when lane enables are de-asserted in P0 (mission mode). A PSR entry is assumed when lane enables are de-asserted and this field is programmed to a non-default value.

SNPS_PHY_TX_REQ - SNPS_PHY_TX_REQ

29:19 **Reserved**

Access:	RO
Format:	MBZ

18:16 **dp_tx_rate**

Access:	R/W

TX data rate. Selects the baud rate for transmit path.

Value	Name
000b	baud **[Default]**
001b	baud/2
010b	baud/4

15 **dp_tx0_lpd**

Default Value:	0b
Access:	R/W

lane power down.
If tx0_pstate[1:0] input is set to P2, it takes priority over tx0_lpd and the transmitter is placed in P2 state.

14 **dp_tx1_lpd**

Default Value:	0b
Access:	R/W

lane power down.
Refer to description for dp_tx0_lpd.

13 **dp_tx2_lpd**

Default Value:	0b
Access:	R/W

lane power down.
Refer to description for dp_tx0_lpd.

12 **dp_tx3_lpd**

Default Value:	0b
Access:	R/W

lane power down.
Refer to description for dp_tx0_lpd.

11:4 **Reserved**

Access:	RO
Format:	MBZ

SNPS_PHY_TX_REQ - SNPS_PHY_TX_REQ

	3:2	**dp_tx_width** Access: R/W TX data width. **Value** / **Name** 00b: 8-bit 01b: 10-bit 10b: 16-bit 11b: 20-bit **[Default]**
	1:0	**Reserved** Access: RO Format: MBZ

SNPS_PHY_TYPEC_STATUS

SNPS_PHY_TYPEC_STATUS - SNPS_PHY_TYPEC_STATUS	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Access:	R/W
Size (in bits):	32
Reset:	global
Address:	168400h-168403h
Name:	SNPS_PHY_TYPEC_STATUS
ShortName:	SNPS_PHY_TYPEC_STATUS_PORT_A
Reset:	global
Address:	169400h-169403h
Name:	SNPS_PHY_TYPEC_STATUS
ShortName:	SNPS_PHY_TYPEC_STATUS_PORT_B
Reset:	global
Address:	16A400h-16A403h
Name:	SNPS_PHY_TYPEC_STATUS
ShortName:	SNPS_PHY_TYPEC_STATUS_PORT_C
Reset:	global
Address:	16B400h-16B403h
Name:	SNPS_PHY_TYPEC_STATUS
ShortName:	SNPS_PHY_TYPEC_STATUS_PORT_D
Reset:	global
Address:	16C400h-16C403h
Name:	SNPS_PHY_TYPEC_STATUS
ShortName:	SNPS_PHY_TYPEC_STATUS_PORT_TC1
Reset:	global

This register is not reset by the device 2 FLR.

DWord	Bit	Description
0	31	**dpalt_disable live status** Access: RO DP Alt-mode Disable/Enable request. TCA asserts this signal to tell the DP controller that DP alt mode is disabled. The DP controller should disable lanes it controls and respond with dpalt_disable_ack. TCA de-asserts ths signal to let the DP controller know that DP alt mode is required. The DP controller should configure and enable lanes it controls.

SNPS_PHY_TYPEC_STATUS - SNPS_PHY_TYPEC_STATUS

	30	**dpalt_disable_ack_status** Access: RO This is a status signal for driver to read. This bit indicates DP controller acknowledge to DP Alt mode disable/enable request. This is in response to dpalt_disable request from TCA.
	29	**dpalt_dp4** Access: RO DP ALT mode DP2/DP4 indication - whether 2 lanes or 4 lanes are accessible to DP controller. DP2 always uses the lower 2 TX lanes. Value: 0b — 2 lanes accessible **[Default]** Value: 1b — 4 lanes accessible
	28	**dpalt_disable_ack** Access: R/W SW asserts this signal in response to dpalt_disable request from TCA only when PHY_MISC1[select_SW_seq] register bit is set. This bit should be at default when PHY_MISC1[select_SW_seq] register bit is not set.
	27:0	**Reserved** Access: RO Format: MBZ

Soft Scratch

SOFT_SCRATCH - Soft Scratch

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	512

These are 16 dword software scratchpad dword registers defined for use.

Programming Notes

These registers are saved in the power context

DWord	Bit	Description
0..15	511:0	**Scratch** Access: R/W

South Display Engine Interrupt Bit Definition

South Display Engine Interrupt Bit Definition

Register Space:	MMIO: 0/2/0
Address:	C4000h-C400Fh
Name:	South Display Engine Interrupts
ShortName:	SDE_INTERRUPT
Reset:	soft

South Display Engine (SDE) interrupt bits come from events within the south display engine. The SDE_IIR bits are ORed together to generate the South/PCH Display Interrupt Event which will appear in the North Display Engine Interrupt Control Registers. The South Display Engine Interrupt Control Registers all share the same bit definitions from this table.

Programming Notes

Due to the possibility of back to back Hotplug events it is recommended that software filters the value read from the Hotplug ISRs.

A wake pin is driven with the inverted value of the south display interrupt event line. The output of the wake pin is used to exit any power state that may prevent the interrupt from propagating to driver.
When any interrupt is enabled, the I/O buffer will be enabled for the Wake pin.

The hotplug typeC interrupts here are only for hotplug on a type-C PHY using a native DP or HDMI connector. Hotplug with type-C connector is covered in a separate type-C hotplug interrupt section.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:26	**Reserved** Access: RO Format: MBZ
	25	**Hotplug TypeC Port 1** The ISR indicates the live value of the hotplug line when hotplug detect is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register. See note on hotplug typeC interrupts.
	24	**Reserved** Access: RO Format: MBZ
	23	**Gmbus** This is an active high pulse when any of the events unmasked events in GMBUS4 Interrupt Mask register occur.

South Display Engine Interrupt Bit Definition

	22:20	**Reserved** Access: RO Format: MBZ
	19	**Hotplug DDID** The ISR indicates the live value of the hotplug line when hotplug detect is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	18	**Hotplug DDIC** The ISR indicates the live value of the hotplug line when hotplug detect is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	17	**Hotplug DDIB** The ISR indicates the live value of the hotplug line when hotplug detect is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	16	**Hotplug DDIA** The ISR indicates the live value of the hotplug line when hotplug detect is enabled. The IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
	15:10	**Reserved** Access: RO Format: MBZ
	9	**SCDC TypeC Port 1** The IIR is set when a HDMI 2.0 SCDC read request event is detected. The ISR is active high level signal that will indicate if the read request (RR) is still active.
	8:4	**Reserved** Access: RO Format: MBZ
	3	**SCDC DDID** The IIR is set when a HDMI 2.0 SCDC read request event is detected. The ISR is active high level signal that will indicate if the read request (RR) is still active.
	2	**SCDC DDIC** The IIR is set when a HDMI 2.0 SCDC read request event is detected. The ISR is active high level signal that will indicate if the read request (RR) is still active.
	1	**SCDC DDIB** The IIR is set when a HDMI 2.0 SCDC read request event is detected. The ISR is active high level signal that will indicate if the read request (RR) is still active.
	0	**SCDC DDIA** The IIR is set when a HDMI 2.0 SCDC read request event is detected. The ISR is active high level signal that will indicate if the read request (RR) is still active.

SPI_ERROR_OPTIONROMBAR_ADDRESS

SPI_ERROR_OPTIONROMBAR_ADDRESS - SPI_ERROR_OPTIONROMBAR_ADDRESS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1020B8h

Programming Notes

This register records the OptionROM BAR SPI address which resulted in a SPI access error.

DWord	Bit	Description
0	31:0	**PrimarySPIAddress** Access: R/W One Clear _Custom_GTIReset: BUS This register contains the SPI address offset which had an error from a OptionROM BAR source.

SPI_ERROR_PRIMARY_ADDRESS

SPI_ERROR_PRIMARY_ADDRESS - SPI_ERROR_PRIMARY_ADDRESS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1020B4h

Programming Notes

This register records the Primary SPI address which resulted in a SPI access error.

DWord	Bit	Description
0	31:0	**PrimarySPIAddress** Access: R/W One Clear _Custom_GTIReset: BUS This register contains the SPI address offset which had an error from a Primary source..

SPI_ERROR_SRC

SPI_ERROR_SRC - SPI_ERROR_SRC

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	1020B0h

Programming Notes

This register records SPI access error information.

DWord	Bit	Description
0	31:12	**SPARE** Access: R/W One Clear _Custom_GTIReset: BUS Spare.
	11	**SPARE3** Access: R/W One Clear _Custom_GTIReset: BUS Spare.
	10:9	**GSC_SPI_ERROR_OPCODE** Access: R/W One Clear _Custom_GTIReset: BUS gSC SPI access error opcode (00=Write, 01=Read, 10=Erase, 11=Reserved).
	8	**GSC_SPI_ERROR** Access: R/W One Clear _Custom_GTIReset: BUS 0=No gSC SPI access error. 1=gSC SPI access error occurred.
	7	**SPARE2** Access: R/W One Clear _Custom_GTIReset: BUS Spare.
	6:5	**OPTIONROMBAR_SPI_ERROR_OPCODE** Access: R/W One Clear _Custom_GTIReset: BUS OPTIONROMBAR SPI access error opcode (00=Write, 01=Read, 10=Erase, 11=Reserved).

SPI_ERROR_SRC - SPI_ERROR_SRC

	4	**OPTIONROMBAR_SPI_ERROR** Access: R/W One Clear _Custom_GTIReset: BUS 0=No OptionROMBAR SPI access error. 1=OptionROMBAR SPI access error occurred.
	3	**SPARE1** Access: R/W One Clear _Custom_GTIReset: BUS Spare.
	2:1	**PRIMARY_SPI_ERROR_OPCODE** Access: R/W One Clear _Custom_GTIReset: BUS OPTIONROMBAR SPI access error opcode (00=Write, 01=Read, 10=Erase, 11=Reserved).
	0	**PRIMARY_SPI_ERROR** Access: R/W One Clear _Custom_GTIReset: BUS 0=No Primary SPI access error. 1=Primary SPI access error occurred.

SPI_STATIC_REGIONS

SPISTATICREGIONS - SPI_STATIC_REGIONS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	102090h

Programming Notes

Write-able via BIOS PG, if needed. This register would be updated for work-around purposes only.

DWord	Bit	Description
0	31:17	**SPARE** Default Value: 0000h Access: RO _Custom_GTIReset: BUS Spare for future usage.
	16	**Remove OROM exposure** Default Value: 0b Access: R/W _Custom_GTIReset: BUS 0 - OptionROM Bar is write-able 1 - OptionROM Bar is RO gSC will program this to the appropriate value
	15:8	**Reserved** Access: RO Format: MBZ
	7:0	**OPTIONROMSPIREGIONID** Default Value: 02h Access: R/W _Custom_GTIReset: BUS This register supplies the OptionROM BAR associated RegionID for SPI accesses.

SRD_CTL

SRD_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60800h-60803h
Name:	Transcoder SRD Control
ShortName:	SRD_CTL_A
Reset:	soft
Address:	61800h-61803h
Name:	Transcoder SRD Control
ShortName:	SRD_CTL_B
Reset:	soft
Address:	62800h-62803h
Name:	Transcoder SRD Control
ShortName:	SRD_CTL_C
Reset:	soft
Address:	63800h-63803h
Name:	Transcoder SRD Control
ShortName:	SRD_CTL_D
Reset:	soft

Restriction : PSR needs to be enabled only when at least one plane is enabled.

Programming Notes

To use FBC modification tracking for idleness calculations when FBC is disabled, program FBC_CTL CPU Fence Enable, FBC_CONTROL_SA_REGISTER, FBC_CPU_FENCE_OFFSET_REGISTER, FBC_RT_BASE_ADDR_REGISTER, and BLITTER_TRACKING_REGISTER as they are programmed when FBC is enabled.

Cursor front buffer modifications are not tracked in hardware. If the cursor front buffer is modified, touch (write without changing) any cursor register to trigger the PSR idleness tracking.

Restriction

Only the SRD Enable and Single Frame Update Enable fields can be changed while SRD is enabled. The other fields must not be changed while SRD is enabled.

DWord	Bit	Description
0	31	**SRD Enable** Access: R/W This bit enables the Self Refreshing Display function. Updates will take place at the start of the next vertical blank. The port will send SRD VDMs while enabled. When idleness conditions have been met for the programmed number of idle frames, hardware will enter SRD (sleep) and can

disable the link and stop fetching data from memory. When activity occurs, hardware will exit SRD (wake) and re-enable the link and resume fetching data from memory.

Value	Name
0b	Disable
1b	Enable

Restriction
SRD must not be enabled when the PSR Setup time from DPCD 00071h is greater than the time for vertical blank minus one line.
SRD must not be enabled together with Interlacing, Black Frame Insertion (BFI), or audio on the same transcoder.

30 **Single Frame Update Enable**

Access:	Double Buffered

This field enables the single frame update mode where a plane flip will cause a single frame to be sent to the receiver. Updates to this field will take effect at the next vertical blank.

Value	Name
0b	Disable
1b	Enable

Programming Notes
Set register PIPE_MISC field Change Mask for Vblank Vsync Int to 1b (Masked) if vblank or vsync interrupts will be used together with single frame update.

Workaround
When Single Frame Update is enabled, the CRC must be disabled for panel compatibility.

Restriction
This mode should only be enabled with link standby.

29 **Context restore to PSR Active**

Access:	R/W

This field restores eDP context to PSR Active on a context restore.

Value	Name
0b	Disable
1b	Enable

Restriction
This field is used for hardware communication. Software must not change this field.

SRD_CTL

28 **Adaptive Sync Frame Update**

Access:	R/W

This field enables the Adaptive Sync Frame Update mode where a flip will cause a single frame to be sent to the receiver. Updates to this field will take effect at the next vertical blank. This field must be enabled with VRR enable.

Restriction : This mode should only be enabled with the SRD Link Disable mode. This mode does not support VRR Max Shift. However, normal and flipline VRR modes are supported.

Value	Name
0b	Disable
1b	Enable

Programming Notes
Set register PIPE_MISC field **Change Mask for Vblank Vsync Int** to 1b (Masked) if vblank or vsync interrupts will be used together with single frame update.

27 **Link Ctrl**

Access:	R/W

This field controls the behavior of the link when in SRD (sleeping). The timing generator and pixel data fetches are disabled when the link is disabled. Only pixel data fetches are disabled when the link is in standby.
This field is ignored by transcoder A/B/C since they only operate in standby.

Value	Name	Description
0b	Disable	Link is disabled when in SRD (sleeping)

26:25 **Reserved**

Access:	RO
Format:	MBZ

24:20 **Max Sleep Time**

Default Value:	00001b 1/8 second
Access:	R/W

This field is the maximum time to spend in SRD (sleeping). It is programmed in increments of approximately 1/8 a second. Programming all 1s gives ~3.875 seconds.

Restriction
Programming all 0s is invalid.

19:17 **Reserved**

Access:	RO
Format:	MBZ

SRD_CTL

16:14 Reserved

Access:	RO
Format:	MBZ

13 Reserved

Access:	R/W

12 Reserved

Access:	R/W

11 TP2 TP3 Select

Access:	R/W

This field controls whether TP1 is followed by TP2 or TP3 for training the link on exiting SRD (waking).

Value	Name	Description
0b	TP2	Use TP1 followed by TP2
1b	TP3	Use TP1 followed by TP3

Programming Notes
This bit impacts PSR2. Clear it before enabling PSR2 and do not set it while PSR2 is enabled.

10 CRC Enable

Access:	R/W

This field controls whether the PSR CRC value will be placed in the VSC packet.

Value	Name	Description
0b	Disable	Disable CRC output in VSC. VSC packet CRC value will be populated by VIDEO_DIP_DATA.
1b	Enable	Enable CRC output in VSC. VSC packet CRC value will be populated by the calculated CRC value.

Programming Notes
When CRC is enabled, the Max Sleep Timer should be disabled to provide additional power savings. Disable the Max Sleep Timer by setting register 0x6F860 bit 28 to 1. Re-enable the Max Sleep Timer by clearing register 0x6F860 bit 28 to 0.

Workaround
When Single Frame Update is enabled, the CRC must be disabled for panel compatibility.

9:8 TP2 TP3 Time

Access:	R/W

This field selects the TP2 or TP3 time when training the link on exiting SRD (waking).

Value	Name
00b	500us
01b	100us

SRD_CTL

	10b	2.5ms
	11b	0us Skip TP2/TP3

7:6 TP4 time

Access:	R/W

This field selects the TP4 time when training the link on exiting SRD (waking).
If this field is set to any value other than "11", TP4 pattern will be sent at PSR reentry.

Value	Name	Description
00b	500 us	
01b	100 us	
10b	2.5 ms	
11b	0 us	Skip TP4

Programming Notes
Always program TP4 to 11b.

5:4 TP1 Time

Access:	R/W

This field selects the TP1 time when training the link on exiting SRD (waking).

Value	Name	Description
00b	500us	
01b	100us	
10b	2.5ms	
11b	0us	Skip TP1

3:0 Idle Frames

Default Value:	0001b 1 idle frame
Access:	R/W

This field is the number of idle frames required before entering SRD (sleeping).

SRD_PERF_CNT

SRD_PERF_CNT	
Register Space:	MMIO: 0/2/0
Access:	Write/Read Status
Size (in bits):	32
Address:	60844h-60847h
Name:	Transcoder SRD Performance Counter
ShortName:	SRD_PERF_CNT_A
Reset:	soft
Address:	61844h-61847h
Name:	Transcoder SRD Performance Counter
ShortName:	SRD_PERF_CNT_B
Reset:	soft
Address:	62844h-62847h
Name:	Transcoder SRD Performance Counter
ShortName:	SRD_PERF_CNT_C
Reset:	soft
Address:	63844h-63847h
Name:	Transcoder SRD Performance Counter
ShortName:	SRD_PERF_CNT_D
Reset:	soft

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**SRD Perf Cnt** Access: Write/Read Status This field increments every millisecond while in SRD (sleeping) and the display CD clock is running. It will stop incrementing when out of SRD (awake), then resume when back in SRD (sleeping). The value is maintained while SRD is disabled, and counting will resume from the previous value when SRD is re-enabled. Writes to this register will set the count to the written value, then it will increment from that value onwards.

SRD_STATUS

SRD_STATUS	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	60840h-60843h
Name:	Transcoder SRD Status
ShortName:	SRD_STATUS_A
Reset:	soft
Address:	61840h-61843h
Name:	Transcoder SRD Status
ShortName:	SRD_STATUS_B
Reset:	soft
Address:	62840h-62843h
Name:	Transcoder SRD Status
ShortName:	SRD_STATUS_C
Reset:	soft
Address:	63840h-63843h
Name:	Transcoder SRD Status
ShortName:	SRD_STATUS_D
Reset:	soft

DWord	Bit	Description
0	31:29	**SRD State** Access: RO This field indicates the live state of SRD

Value	Name	Description
000b	IDLE	Reset state
001b	SRDONACK	Wait for TG/Stream to send on frame of data after SRD conditions are met
010b	SRDENT	SRD entry with Link OFF
011b	BUFOFF	Wait for buffer turn off
100b	BUFON	Wait for buffer turn on
101b	AUXACK	Wait for AUX to acknowledge on SRD exit
110b	SRDOFFACK	Wait for TG/Stream to acknowledge the SRD VDM exit
111b	SRDENT_ON	SRD entry with Link ON
Others	Reserved	Reserved

SRD_STATUS

28 Reserved

Access:	RO
Format:	MBZ

27:26 Link Status

Access:	RO

This field indicates the live status of the link.

Value	Name	Description
00b	Full Off	Link is fully off
01b	Full On	Link is fully on
11b	Reserved	Reserved

25 Reserved

Access:	RO
Format:	MBZ

24:20 Max Sleep Time Counter

Access:	RO

This field provides the live status of the sleep time counter.

19:16 SRD Entry Count

Access:	RO

The value in this register represents the number of times SRD has been entered (gone to sleep). The count will increment with each entry. After reaching the maximum count value the counter will rollover and continue from 0.

15 Aux Error

Access:	RO

This field indicates an error on the last SRD AUX handshake.

Value	Name	Description
0b	No Error	AUX had no error
1b	Error	AUX error (receive error or timeout) occurred

14:13 Reserved

Access:	RO
Format:	MBZ

12 Sending Aux

Access:	RO

This field indicates if the SRD AUX handshake is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending AUX handshake
1b	Sending	Sending AUX handshake

SRD_STATUS

11:10 Reserved

Access:	RO
Format:	MBZ

9 Sending Idle

Access:	RO

This field indicates if idles are currently being sent.

Value	Name	Description
0b	Not Sending	Not sending idle
1b	Sending	Sending idle

8 Sending TP2 TP3

Access:	RO

This field indicates if TP2 or TP3 is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending TP2 or TP3
1b	Sending	Sending TP2 or TP3

7 Sending TP4

Access:	RO

This field indicates if TP4 is currently being sent.

Value	Name
0b	Not Sending
1b	Sending

6:5 Reserved

Access:	RO
Format:	MBZ

4 Sending TP1

Access:	RO

This field indicates if TP1 is currently being sent.

Value	Name	Description
0b	Not Sending	Not sending TP1
1b	Sending	Sending TP1

3:0 Idle Frame Counter

Access:	RO

This field provides the live status of the idle frame counter.

Programming Notes
The value of this field is not preserved across power down states such as DC5 and up.

SRIOV Capabilities

SRIOV_CAP_0_2_0_PCI - SRIOV Capabilities

Register Space: PCI: 0/2/0
Size (in bits): 32

Address: 00324h

Defines SR-IOV Capabilities

DWord	Bit	Description
0	31:21	**VF Migration Interrupt Message Number** Default Value: 00000000000b Access: RO _Custom_GTIReset: BUS Value: 0. VF Migration is not supported.
	20:3	**Reserved** Access: RO Format: MBZ
	2	**VF 10-Bit Tag Requester Supported** Default Value: 1b Access: RO _Custom_GTIReset: BUS If Set, all VFs must support 10-Bit Tag Requester capability. If Clear, VFs must not support 10-Bit Tag Requester capability.
	1	**ARI Capable Hierarchy Preserved** Default Value: 0b Access: RO _Custom_GTIReset: BUS Value: 0. ARI not supported.
	0	**VF Migration Capable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Value:0. VF Migration not supported.

SRIOV Control Register

SRIOV_CTRL_0_2_0_PCI - SRIOV Control Register

Register Space: PCI: 0/2/0
Size (in bits): 16

Address: 00328h

SR-IOV Control Register.

DWord	Bit	Description
0	15:6	**Reserved** Access: RO Format: MBZ
	5	**VF 10-Bit Tag Requester Enable** Access: R/W _Custom_GTIReset: BUS If Set, all VFs must use 10-Bit Tags for all Non-Posted Requests they generate. If Clear, VFs must not use 10-Bit Tags for Non-Posted Requests they generate Value: 0b **[Default]**; 1b Name:
	4	**ARI Capable Hierarchy** Default Value: 0b Access: R/W _Custom_GTIReset: DEV This bit must be RW in the lowest-numbered PF of the Device and hardwired to 0b in all other PFs. If the value of this bit is 1b, the Device is permitted to locate VFs in Function Numbers 8 to 255 of the captured Bus Number. Otherwise, the Device must locate VFs as if it were a non-ARI Device. This bit is not affected by FLR of any PF or VF. Default value is 0b
	4	**ARI Capable Hierarchy** Default Value: 0b Access: R/W _Custom_GTIReset: DEV This bit must be RW in the lowest-numbered PF of the Device and hardwired to 0b in all other PFs. If the value of this bit is 1b, the Device is permitted to locate VFs in Function Numbers 8 to 255 of the captured Bus Number. Otherwise, the Device must locate VFs as if it were a non-ARI Device. This bit is not affected by FLR of any PF or VF. Default value is 0b

SRIOV_CTRL_0_2_0_PCI - SRIOV Control Register

3 VF Memory Space Enable

Default Value:	0b
Access:	R/W
_Custom_GTIReset:	BUS

SW shall set this bit before setting VF Enable. (to allow VF memory space response)

2 VF Migration Interrupt Enable

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

VF migration is not supported.

1 VF Migration Enable

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

VF migration is not supported.

0 VF Enable

Access:	R/W
_Custom_GTIReset:	BUS

System SW shall set this bit to enable VFs.
Note: This bit becomes RO defaulting to 0 if SRIOV is disabled by fuse.
Its R/W only when SRIOV is enabled by fuse.

System SW shall set this bit to enable VFs. Setting/Clearing this bit shall result in an interrupt to GUC. This allows the GuC and subsequently the PF to take appropriate action to comprehend virtualization.

Value	Name
0b	Disable VFs **[Default]**
1b	Enable VFs

SRIOV Extended Capability Header

SRIOV_ECAPHDR_0_2_0_PCI - SRIOV Extended Capability Header

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00320h

SR-IOV Extended Capability Header.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Default Value: 010000000000b Access: RO _Custom_GTIReset: BUS Next capability Offset. Value = 0x400 to indicate the next capability structure: LTR messaging
	19:16	**Capability Version** Default Value: 1b Access: RO _Custom_GTIReset: BUS Indicates the version of the capability
	15:0	**PCIE Extended Capability ID** Default Value: 0000000000010000b Access: RO _Custom_GTIReset: BUS PCIE Extended Capability ID

SRIOV Initial VFs

SRIOV_INITVFS_0_2_0_PCI - SRIOV Initial VFs		
Register Space: PCI: 0/2/0 Size (in bits): 16		
Address: 0032Ch		
Defines Initial number of VFs available to the VMM.		
DWord	**Bit**	**Description**
0	15:0	**INITIAL VFS** Access: RO Variant _Custom_GTIReset: BUS For SR-IOV implementation, this value must exactly match the Total VFs

SRIOV Status

SRIOV_STS_0_2_0_PCI - SRIOV Status		
Register Space:	PCI: 0/2/0	
Size (in bits):	16	
Address:	0032Ah	
SR-IOV Status Register.		
DWord	**Bit**	**Description**
0	15:1	**Reserved** Access: RO Format: MBZ
	0	**VF Migration Status** Default Value: 0b Access: RO _Custom_GTIReset: BUS VF Migration Status

SRIOV Total VFs

SRIOV_TOTVFS_0_2_0_PCI - SRIOV Total VFs

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	0032Eh

Defines the Total number of VFs available to the VMM.
Fuses determine the value exposed, so product fusing will ultimately determine the value reported.

DWord	Bit	Description
0	15:0	**Total VFS** Access: RO Variant _Custom_GTIReset: BUS Indicates the maximum number of VFs that could be associated with the PF

Value	Name
0000000000000111b	
0000000000000001b	
0000000000001111b	
0000000000011111b	

SSM0 BONUS1 Reg

SSM0SPCBONUS1 - SSM0 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24414h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM0SPCBONUS1 - SSM0 BONUS1 Reg

	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM0 BONUS2 Reg

SSM0SPCBONUS2 - SSM0 BONUS2 Reg		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24418h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM0SPCBONUS2 - SSM0 BONUS2 Reg

	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM1 BONUS1 Reg

SSM1SPCBONUS1 - SSM1 BONUS1 Reg		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	24494h	
Clock Gating Messages Register		
DWord	**Bit**	**Description**
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM1SPCBONUS1 - SSM1 BONUS1 Reg

	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM1 BONUS2 Reg

SSM1SPCBONUS2 - SSM1 BONUS2 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24498h
Clock Gating Messages Register	

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM1SPCBONUS2 - SSM1 BONUS2 Reg

	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM2 BONUS1 Reg

SSM2SPCBONUS1 - SSM2 BONUS1 Reg

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24514h
Clock Gating Messages Register	

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS1 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS1 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS1 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS1 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM2SPCBONUS1 - SSM2 BONUS1 Reg

	3	**BONUS1 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS1 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS1 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS1 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS1 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM2 BONUS2 Reg

SSM2SPCBONUS2 - SSM2 BONUS2 Reg

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24518h

Clock Gating Messages Register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**BONUS2 BIT 7** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	6	**BONUS2 BIT 6** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	5	**BONUS2 BIT 5** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	4	**BONUS2 BIT 4** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SSM2SPCBONUS2 - SSM2 BONUS2 Reg

	3	**BONUS2 BIT 3** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	2	**BONUS2 BIT 2** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req
	1	**BONUS2 BIT 1** Access: R/W _Custom_GTIReset: BUS SLICE 0 BONUS2 BIT: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**BONUS2 BIT 0** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

ssmcp Sub Slice Power Context Save request

SSMPCTXSAVEREQ - ssmcp Sub Slice Power Context Save request

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 08150h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO _Custom_GTIReset: BUS Reserved
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

Stream Output 0 Num Primitives Written Counter

SO0_NUM_PRIMS_WRITTEN - Stream Output 0 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05200h-05207h
Name:	Stream Output 0 Num Primitives Written Counter
ShortName:	SO0_NUM_PRIMS_WRITTEN

There is one 64-bit register for each of the 4 supported streams:

- 5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
- 5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
- 5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
- 5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.
More details about the precise event counted by this register are located **Statistics Gathering.**

DWord	Bit	Description
0	31:0	**Num Prims Written Count 0** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count 1** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 0 Primitive Storage Needed Counter

SO0_PRIM_STORAGE_NEEDED - Stream Output 0 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05240h-05247h
Name:	Stream Output 0 Primitive Storage Needed Counter
ShortName:	SO0_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:

- 5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
- 5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
- 5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
- 5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)

These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.
More details about the precise event counted by this register are located **here.**

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count 0** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count 1** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 0 Write Offset

SO0_WRITE_OFFSET - Stream Output 0 Write Offset

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	05280h-05283h
Name:	Stream Output 0 Write Offset
ShortName:	SO0_WRITE_OFFSET

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Access: R/W Format: U30 _Custom_GTIReset: DEV This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Access: RO Format: MBZ

Stream Output 1 Num Primitives Written Counter

SO1_NUM_PRIMS_WRITTEN - Stream Output 1 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05208h-0520Fh
Name:	Stream Output 1 Num Primitives Written Counter
ShortName:	SO1_NUM_PRIMS_WRITTEN

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count 0** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count 1** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 1 Primitive Storage Needed Counter

SO1_PRIM_STORAGE_NEEDED - Stream Output 1 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05248h-0524Fh
Name:	Stream Output 1 Primitive Storage Needed Counter
ShortName:	SO1_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count 0** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count 1** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 1 Write Offset

SO1_WRITE_OFFSET - Stream Output 1 Write Offset

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	05284h-05287h
Name:	Stream Output 1 Write Offset
ShortName:	SO1_WRITE_OFFSET

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Access: R/W Format: U30 _Custom_GTIReset: DEV This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Access: RO Format: MBZ

Stream Output 2 Num Primitives Written Counter

SO2_NUM_PRIMS_WRITTEN - Stream Output 2 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05210h-05217h
Name:	Stream Output 2 Num Primitives Written Counter
ShortName:	SO2_NUM_PRIMS_WRITTEN

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count 0** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count 1** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 2 Primitive Storage Needed Counter

SO2_PRIM_STORAGE_NEEDED - Stream Output 2 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05250h-05257h
Name:	Stream Output 2 Primitive Storage Needed Counter
ShortName:	SO2_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count 0** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count 1** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 2 Write Offset

SO2_WRITE_OFFSET - Stream Output 2 Write Offset

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	05288h-0528Bh
Name:	Stream Output 2 Write Offset
ShortName:	SO2_WRITE_OFFSET

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Access: R/W Format: U30 _Custom_GTIReset: DEV This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Access: RO Format: MBZ

Stream Output 3 Num Primitives Written Counter

SO3_NUM_PRIMS_WRITTEN - Stream Output 3 Num Primitives Written Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05218h-0521Fh
Name:	Stream Output 3 Num Primitives Written Counter
ShortName:	SO3_NUM_PRIMS_WRITTEN

There is one 64-bit register for each of the 4 supported streams:
5200h-5207h SO_NUM_PRIMS_WRITTEN0 (for Stream Out Stream #0)
5208h-520Fh SO_NUM_PRIMS_WRITTEN1 (for Stream Out Stream #1)
5210h-5217h SO_NUM_PRIMS_WRITTEN2 (for Stream Out Stream #2)
5218h-521Fh SO_NUM_PRIMS_WRITTEN3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has successfully written to a particular "stream's" Streamed Vertex Output buffers, subject to buffer overflow detection. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Num Prims Written Count 0** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)
1	31:0	**Num Prims Written Count 1** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) every time a GS thread outputs a DataPort Streamed Vertex Buffer Write message with the Increment Num Prims Written bit set in the message header (see the Geometry Shader and Data Port chapters in the 3D Volume.)

Stream Output 3 Primitive Storage Needed Counter

SO3_PRIM_STORAGE_NEEDED - Stream Output 3 Primitive Storage Needed Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
Address:	05258h-0525Fh
Name:	Stream Output 3 Primitive Storage Needed Counter
ShortName:	SO3_PRIM_STORAGE_NEEDED

There is one 64-bit register for each of the 4 supported streams:
5240h-5247h SO_PRIM_STORAGE_NEEDED0 (for Stream Out Stream #0)
5248h-524Fh SO_PRIM_STORAGE_NEEDED1 (for Stream Out Stream #1)
5250h-5257h SO_PRIM_STORAGE_NEEDED2 (for Stream Out Stream #2)
5258h-525Fh SO_PRIM_STORAGE_NEEDED3 (for Stream Out Stream #3)
These registers are used to count the number of primitives (aka objects: points, lines, triangles) which the SO stage has or would have written to a particular "stream's" Streamed Vertex Output buffers if all buffers had been large enough to accommodate the writes. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

DWord	Bit	Description
0	31:0	**Prim Storage Needed Count 0** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.
1	31:0	**Prim Storage Needed Count 1** Access: R/W Format: U32 _Custom_GTIReset: DEV This count is incremented (by one) by the SOL stage for each object (point, line, triangle) it writes or attempts to write to the corresponding stream's output buffers. The count is not affected by the actual number of buffers bound to the stream.

Stream Output 3 Write Offset

SO3_WRITE_OFFSET - Stream Output 3 Write Offset

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	0528Ch-0528Fh
Name:	Stream Output 3 Write Offset
ShortName:	SO3_WRITE_OFFSET

There is one R/W 32-bit register for each of the 4 supported stream output buffer slots:
5280h-5283h SO_WRITE_OFFSET0 (for Stream Out Buffer #0)
5284h-5287h SO_WRITE_OFFSET1 (for Stream Out Buffer #1)
5288h-528Bh SO_WRITE_OFFSET2 (for Stream Out Buffer #2)
528Ch-528Fh SO_WRITE_OFFSET3 (for Stream Out Buffer #3)
These registers are used to set and track a DWord-granular Write Offset for each of the 4 Stream Output Buffer slots. Software can directly write them via MI_LOAD_REGxxx commands. The SOL stage will increment them as part of stream output processing. Software can cause them to be written to memory via MI_STORE_REGxxx commands. (See the Stream Output section of the 3D pipeline volume).
These registers are part of the context save and restore.

Programming Notes

- Software must ensure that no HW stream output operations can be in process or otherwise pending at the point that the MI_LOAD/STORE commands are processed. This will likely require a pipeline flush.
- The SOL stage will effectively advance the write offset by the buffer's Surface Pitch after each vertex is written (assuming no overflow is detected in any targeted SO buffer). Under "normal" conditions one would expect software to initialize the WriteOffset to some (possibly zero) multiple of Surface Pitch in order to align vertex writes to the buffer's Base Address, though it is not required to do so.

DWord	Bit	Description
0	31:2	**Write Offset** Access: R/W Format: U30 _Custom_GTIReset: DEV This field contains a DWord offset from the corresponding SO buffer's Base Address value. The SOL stage uses this value as a write offset when performing writes to the buffer. The SOL stage will increment this value as a part of performing stream output to the buffer. Note that the SOL stage uses the buffer's Surface Pitch to advance the Write Offset, without regard to the buffer's Base Address (see Programming Notes above).
	1:0	**Reserved** Access: RO Format: MBZ

SubSlice0 Power Down FSM control register with lock

SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 24410h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don’t firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e dont assert reset, but complete logical flow

SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e dont clock gate, but complete logical flow
9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e dont power off pfet, but complete logical flow
8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

SSM0SPCPOWERDNFSMCTL - SubSlice0 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

SubSlice 0 Power Gate Control Request

SSM0PGCTLREQ - SubSlice 0 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24400h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SubSlice 0 Power on FSM control register with lock

SSM0SPCPOWERUPFSMCTL - SubSlice 0 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2440Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets

SSM0SPCPOWERUPFSMCTL - SubSlice 0 Power on FSM control register with lock

		1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

SubSlice 1 Power Context Save request

SSM1PGCTXREQ - SubSlice 1 Power Context Save request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24484h

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask bots for lower 16 bits
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Power context save request** Access: R/W Set _Custom_GTIReset: BUS Power Context Save Request 1'b0 : Power context save is not being requested 1'b1 : Power context save is being requested CPUnit self-clears this bit upon sampling.
	8:0	**Power Context Save request crdit count** Access: R/W _Custom_GTIReset: BUS QWord Credits for Power Context Save Request Minimum Credits = 1 : Unit may send 1 QWord pair (enough for first LRI at least) Maximum Credits = 511 : Unit may send 511 QWord pairs A QWord pair is defined as a 32-bit register address and the corresponding 32-bits of register data. Note that the LRI header and END commands are 64-bits each (32-bit command followed by 32-bit NOOP) and will consume one QWord credit. Only valid with PWRCTX_SAVE_REQ (Bit9).

SubSlice 1 Power Down FSM control register with lock

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24490h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

SSM1SPCPOWERDNFSMCTL - SubSlice 1 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

SubSlice 1 Power Gate Control Request

SSM1PGCTLREQ - SubSlice 1 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24480h
Clock Gating Messages Register	

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SubSlice 1 Power on FSM control register with lock

SSM1SPCPOWERUPFSMCTL - SubSlice 1 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2448Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets

SSM1SPCPOWERUPFSMCTL - SubSlice 1 Power on FSM control register with lock

		1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

SubSlice 2 Power Down FSM control register with lock

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24510h

DWord	Bit	Description
0	31	**power down control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of POWERDNFSMCTL register are R/W 1 = All bits of POWERDNFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:13	**Reserved** Access: RO Format: MBZ
	12	**Leave firewall disabled** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, i.e don't firewall the gated domain, but complete logical flow
	11	**Leave reset de-asserted** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not assert reset for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e assert resets during power down flows 1 = Leave reset de-asserted mode, i.e don't assert reset, but complete logical flow

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock

	10	**Leave CLKs ON** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not gate clks for power off flow. But it will pretend to complete the flow with PM Encodings: 0 = Default mode, i.e gate clocks during power down flows 1 = Leave CLKS ON mode, i.e don't clock gate, but complete logical flow
	9	**Leave FET On** Access: R/W Lock _Custom_GTIReset: BUS When This bit is set SPC will not turn off the PFET even though it will complete the flow with PM Encodings: 0 = Default mode, i.e power off fets during power down flows 1 = Leave ON mode, i.e don't power off pfet, but complete logical flow
	8:6	**Power Down state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Gate Clocks
	5:3	**Power Down state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default :Firewall ON

SSM2SPCPOWERDNFSMCTL - SubSlice 2 Power Down FSM control register with lock

	2:0	**Power Down state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state before power is turned OFF in the well Encodings: 000 = Assert Reset 001 = Firewall ON 010 = Gate clocks 1xx = Rsvd for future Default : Assert Reset

SubSlice 2 Power Gate Control Request

SSM2PGCTLREQ - SubSlice 2 Power Gate Control Request

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	24500h

Clock Gating Messages Register

DWord	Bit	Description
0	31:16	**Message Mask** Access: RO _Custom_GTIReset: BUS Message Mask In order to write to bits 15:0, the corresponding message mask bits must be written. For example, for bit 14 to be set, bit 30 needs to be 1 : 40004000
	15:2	**Reserved** Access: RO Format: MBZ
	1	**CLK RST FWE Request** Access: R/W _Custom_GTIReset: BUS SLICE 0 CLK RST FWE request: '0' : Initiate power down sequence (clk/rst/fwe) '1' : Initiate power up sequence (clk/rst/fwe)
	0	**Power Gate Request** Access: R/W _Custom_GTIReset: BUS SLice 0 power well request: '0' : Initiate Power Down request '1' : Initiate Power UP req

SubSlice 2 Power on FSM control register with lock

SSM2SPCPOWERUPFSMCTL - SubSlice 2 Power on FSM control register with lock

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	2450Ch

DWord	Bit	Description
0	31	**power up control Lock** Access: R/W Lock _Custom_GTIReset: BUS 0 = Bits of POWERUPFSMCTL register are R/W 1 = All bits of POWERUPFSMCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:9	**Reserved** Access: RO Format: MBZ
	8:6	**Power UP state 3** Default Value: 010b Access: R/W Lock _Custom_GTIReset: BUS This will be the 3rd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - De-assert resets 3'b000: 10ns (or 1 bclk)
	5:3	**Power UP state 2** Default Value: 001b Access: R/W Lock _Custom_GTIReset: BUS This will be the 2nd state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets

SSM2SPCPOWERUPFSMCTL - SubSlice 2 Power on FSM control register with lock

		1xx = Rsvd for future Default - Firewall OFF
	2:0	**Power UP state 1** Default Value: 000b Access: R/W Lock _Custom_GTIReset: BUS This will be the 1st state after power is turned ON in the well Encodings: 000 = Clock Ungate 001 = Firewall OFF 010 = De-assert resets 1xx = Rsvd for future Default - Clock Ungate

SubSlice unit Level Clock Gating Control 9520

SSMCGCTL9520 - SubSlice unit Level Clock Gating Control 9520

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09520h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:2	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	1	**GCPunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**SMCRunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS SMCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

SubSlice unit Level Clock Gating Control 9524

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09524h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**EU_FPUunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS EU_FPUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**EU_GAunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS EU_GAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	29	**EU_TCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS EU_TCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	28	**DSS Router Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DSS Router Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

		Workaround SW is required to disable clock gating to converge timing.
	27	**BCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**GADSS Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GADSS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	25	**CREunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**DGunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**DMunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**SLMBE Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SLMBE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	20	**FLunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS FLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	19	**DPAS_EU Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DPAS_EU Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**Ftunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS Ftunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

17	**VMEMSOARB Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMEMSOARB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
16	**GWunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
15	**VMEMREQARB Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMEMREQARB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
14:12	**HDCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
11	**ICunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

10	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
9	**IMEunit's Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS IMEunit's Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
8	**MAunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
7	**MTunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
6	**OATREPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS OATREPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

5	**PLunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS PLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
4	**PSDunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
3	**RAMDFT Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RAMDFT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
2	**SCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
1	**SIunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SSMCGCTL9524 - SubSlice unit Level Clock Gating Control 9524

		Workaround SW is required to disable clock gating to converge timing.
	0	**SOunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SubSlice unit Level Clock Gating Control 9528

SSMCGCTL9528 - SubSlice unit Level Clock Gating Control 9528

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09528h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:27	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	26	**I1intf Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMESC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	25	**I3intf Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMESC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	24	**seqfe Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMESC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

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23	**seqintf Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMESC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
22	**seqbe Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMESC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
21	**l1bank Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMESC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
20	**VMESC Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMESC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
19	**MediaSampler arb unit2 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MSArb2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

SSMCGCTL9528 - SubSlice unit Level Clock Gating Control 9528

		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**MediaSampler arb unit1 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MSArb1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**sslaunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS sslaunit Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	15	**TSL unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS TSLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**MediaSampler arb unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MSArb Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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	13	**DTOunit unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DTOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**SLMFE unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SLMBE unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**RDEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RDEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**Noaunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS Noaunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**CPSSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CPSSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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8	**EUunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS EUunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
7	**EU_EMunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS EU_EMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
6	**sbe_ssbuf Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS sbe_ssbuf Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
5	**DAPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DAPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
4	**starb Clock unit Disable** Access: R/W _Custom_GTIReset: BUS starb Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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3	**STunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

STunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

2	**Reserved**

Access:	R/W
_Custom_GTIReset:	BUS

Reserved

1	**SVSMunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SVSMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

0	**TDLunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

TDLunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

SubSlice unit Level Clock Gating Control 9530

SSMCGCTL9530 - SubSlice unit Level Clock Gating Control 9530

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 09530h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:20	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	19	**stsunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS stsunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**rtfunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS rtfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**rttunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS rttunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**rtcunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS rtcunit Clock Gating Disable Control:

SSMCGCTL9530 - SubSlice unit Level Clock Gating Control 9530

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	15	**rtmunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS rtmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**rttqunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS rttqunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**SPARE Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**CPSSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CPSSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11:10	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved

SSMCGCTL9530 - SubSlice unit Level Clock Gating Control 9530

9	**BCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
8	**CREunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
7	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
6	**GAunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
5	**ICunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ICunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SSMCGCTL9530 - SubSlice unit Level Clock Gating Control 9530

4	**IMEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS IMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
3	**MTunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
2	**PSDunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
1	**SCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
0	**VSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

SubSlice unit Level Clock Gating override during rstflow 9540

SSMMISCCP9540 - SubSlice unit Level Clock Gating override during rstflow 9540		
Register Space: MMIO: 0/2/0 Size (in bits): 32		
Address: 09540h		
Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31:0	**ECO Spare Bits** Access: R/W _Custom_GTIReset: BUS Reserved

Subsystem Identification

SID2_0_2_0_PCI - Subsystem Identification

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	0002Eh

This register is used to uniquely identify the subsystem where the PCI device resides.

DWord	Bit	Description
0	15:0	**Subsystem ID** Default Value: 0000000000000000b Access: R/W _Custom_GTIReset: BUS This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up.

Subsystem Vendor Identification

SVID2_0_2_0_PCI - Subsystem Vendor Identification

Register Space:	PCI: 0/2/0
Size (in bits):	16
Address:	0002Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

DWord	Bit	Description
0	15:0	**Subsystem Vendor ID** Access: R/W _Custom_GTIReset: BUS This value is used to identify the vendor of the subsystem. Value: 8086h — Name: **[Default]**

Supported Page Sizes

SUPPORTED_PAGE_SIZES_0_2_0_PCI - Supported Page Sizes

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	0033Ch

Defines the System Page Sizes supported by this SR-IOV implementation.

DWord	Bit	Description
0	31:0	**SUPPORTED PAGE SIZES VALUE** Default Value: 00000000000000000000010101010011b Access: RO _Custom_GTIReset: BUS This field indicates the page sizes supported by the PF. This PF supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the PF supports 4-KB page sizes. PFs are required to support 4-KB, 8-KB, 64-KB, 256-KB, 1-MB, and 4-MB page sizes. All other page sizes are optional, and not supported in this implementation.

SVL Barrier Done

SVL_BARRIER_DONE - SVL Barrier Done		
Register Space:	MMIO: GTTMMADR	
Size (in bits):	32	
Address:	07FF0h	
This register is used to send messages when a render barrier is done. This register may not be written from CPU.		
DWord	**Bit**	**Description**
0	31:16	**Reserved** Access: RO Format: MBZ
	15:8	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	7:0	**BarrierID**

SWF

SWF	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	4F000h-4F08Fh
Name:	Software Flags
ShortName:	SWF_*

These registers are used as scratch pad data storage space and have no direct effect on hardware operation. There are 36 instances of this register format.

DWord	Bit	Description
0	31:0	**Software Flags** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS Software flags

System Page Sizes

SYSTEM_PAGE_SIZES_0_2_0_PCI - System Page Sizes

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00340h

Defines the System Page Size chosen by the VMM.

DWord	Bit	Description
0	31:0	**SYSTEM PAGE SIZES VALUE** Default Value: 00000000000000000000000000000001b Access: R/W _Custom_GTIReset: BUS This field defines the page size the system will use to map the VFs memory addresses. Software must set the value of the System Page Size to one of the page sizes set in the Supported Page Sizes field (see Section 3.3.12). As with Supported Page Sizes, if bit is Set in System Page Size, the VFs associated with this PF are required to support a page size of 2^(n+12). For example, if bit 1 is Set, the system is using an 8-KB page size. The results are undefined if System Page Size is zero. The results are undefined if more than one bit is set in System Page Size. The results are undefined if a bit is Set in System Page Size that is not Set in Supported Page Sizes. When System Page Size is set, the VF associated with this PF is required to align all BAR resources 20 on a System Page Size boundary. Each VF BARn or VF BARn pair (see Section 3.3.14) shall be aligned on a System Page Size boundary. Each VF BARn or VF BARn pair defining a non-zero address space shall be sized to consume an integer multiple of System Page Size bytes. All data structures requiring page size alignment within a VF shall be aligned on a System Page Size boundary. VF Enable must be zero when System Page Size is written. The results are undefined if System Page Size is written when VF Enable is Set. Default value is 1h (i.e., 4 KB), and that is the only value allowed for this implementation

Tailpointer delay counter

TP_DELAY_CNTR - Tailpointer delay counter	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1C2DA0h-1C2DA3h
Name:	Tailpointer delay counter
ShortName:	TP_DELAY_CNTR_VDENC_REG0
Address:	1C6DA0h-1C6DA3h
Name:	Tailpointer delay counter
ShortName:	TP_DELAY_CNTR_VDENC_REG1
Address:	1D2DA0h-1D2DA3h
Name:	Tailpointer delay counter
ShortName:	TP_DELAY_CNTR_VDENC_REG2
Address:	1D6DA0h-1D6DA3h
Name:	Tailpointer delay counter
ShortName:	TP_DELAY_CNTR_VDENC_REG3
Address:	1E2DA0h-1E2DA3h
Name:	Tailpointer delay counter
ShortName:	TP_DELAY_CNTR_VDENC_REG4
Address:	1E6DA0h-1E6DA3h
Name:	Tailpointer delay counter
ShortName:	TP_DELAY_CNTR_VDENC_REG5
Address:	1F2DA0h-1F2DA3h
Name:	Tailpointer delay counter
ShortName:	TP_DELAY_CNTR_VDENC_REG6
Address:	1F6DA0h-1F6DA3h
Name:	Tailpointer delay counter
ShortName:	TP_DELAY_CNTR_VDENC_REG7

This register has stall counter for the VDENC. In an ideal case, this value should be zero

DWord	Bit	Description
0	31:0	**Tail pointer count delay** Access: R/W Hardware Clear

TASK Invocation Counter

TASK_INVOCATION_COUNT - TASK Invocation Counter

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	026E8h
Name:	TASK Invocation Counter
ShortName:	TASK_INVOCATION_COUNT

The **TASK_INVOCATION_COUNT** accumulates API-levelTask Shader invocations dispatched by the pipeline. For each TaskShader ThreadGroup dispatched, this register is incremented by the thread group size. This register doesnotcount EU thread dispatches.
SW shall comprehend that a pipeline flush is required to ensure that preceding TaskShader work is included in the register value.

DWord	Bit	Description
0	63:32	**TASK Invocation Count UDW** Access: R/W Number of patch objects processed by the TASK stage. Updated only when TASK Enable and TASK Statistics Enable are set in 3DSTATE_TASK
	31:0	**TASK Invocation Count LDW** Access: R/W Number of patch objects processed by the TASK stage. Updated only when TASK Enable and TASK Statistics Enable are set in 3DSTATE_TASK

TASK Invocation Counter per Slice

TASK_INVOCATION_COUNT_SLICE - TASK Invocation Counter per Slice

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

Address:	065C8h-065CFh
Name:	TASK Invocation Counter per Slice
ShortName:	TASK_INVOCATION_COUNT_SLICE_SVGUNIT

Address:	175C8h-175CFh
Name:	TASK Invocation Counter per Slice
ShortName:	TASK_INVOCATION_COUNT_SLICE_SVGRUNIT

The **TASK_INVOCATION_COUNT** accumulatesAPI-levelTask Shader invocations dispatched by the pipeline per Gslice. For each TaskShader ThreadGroup dispatched in that Gslice, this register is incremented by the thread group size. This register doesnotcount EU thread dispatches.
SW shall comprehend that a pipeline flush is required to ensure that preceding TaskShader work is included in the register value.

DWord	Bit	Description
0..1	63:32	**TASK Invocation Count UDW in Slice** Access: R/W Number of patch objects processed by the TASK stage within the slice. Updated only when TASK Enable and TASK Statistics Enable are set in 3DSTATE_TASK
	31:0	**TASK Invocation Count LDW in Slice** Access: R/W Number of patch objects processed by the TASK stage within the slice. Updated only when TASK Enable and TASK Statistics Enable are set in 3DSTATE_TASK

TBIMR Mode Register

TBIMR_MODE - TBIMR Mode Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	06200h-06203h
Name:	TBIMR Mode Register
ShortName:	TBIMR_MODE_SVGUNIT
Address:	17200h-17203h
Name:	TBIMR Mode Register
ShortName:	TBIMR_MODE_SVGRUNIT

TBIMR Mode register.

DWord	Bit	Description
0	31:16	**Mask Bits** Access: WO Format: Mask Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)
	15:12	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	11:8	**Output starved Timer Count** Access: R/W _Custom_GTIReset: DEV This count indicates how many clocks hardware will wait to close the batch if there is no poly packet at the input.

Value	Name
0h	16 Clocks_Output
1h	32 Clocks_Output
2h	48 Clocks_Output
3h	64 Clocks_Output
4h	96 Clocks_Output
5h	128 Clocks_Output **[Default]**
6h	192 Clocks_Output
7h	256 Clocks_Output
8h	384 Clocks_Output
9h	512 Clocks_Output

TBIMR_MODE - TBIMR Mode Register

ah	1024 Clocks_Output
bh	2048 Clocks_Output
ch	4096 Clocks_Output
dh	8192 Clocks_Output
eh	Reserved
fh	Reserved

7:4 **Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

3:0 **Input starved Timer Count**

Access:	R/W
_Custom_GTIReset:	DEV

This count indicates how many clocks hardware will wait to close the batch if the pixel pipe is starved and batch has some poly data.

Value	Name
0h	16 Clocks_Input
1h	32 Clocks_Input
2h	48 Clocks_Input
3h	64 Clocks_Input **[Default]**
4h	96 Clocks_Input
5h	128 Clocks_Input
6h	192 Clocks_Input
7h	256 Clocks_Input
8h	384 Clocks_Input
9h	512 Clocks_Input
ah	1024 Clocks_Input
bh	2048 Clocks_Input
ch	4096 Clocks_Input
dh	8192 Clocks_Input
eh	Reserved
fh	Reserved

TCSS_DISP_MAILBOX_IN_CMD

TCSS_DISP_MAILBOX_IN_CMD

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	3710B0h-3710B3h
Name:	TCSS_DISP_MAILBOX_IN_CMD
ShortName:	TCSS_DISP_MAILBOX_IN_CMD
Reset:	global

DE to IOM Mailbox

DWord	Bit	Description
0	31	**RUN_BUSY** Access: R/W Run/Busy Value / Name: 0b 1b
	30:24	**Reserved** Access: RO Format: MBZ
	23:16	**PARAM2** Access: R/W Parameter 2
	15:8	**PARAM1** Access: R/W Parameter 1
	7:0	**CMD** Access: R/W Command or completion code

TCSS_DISP_MAILBOX_IN_DATA

TCSS_DISP_MAILBOX_IN_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	3710B4h-3710B7h
Name:	TCSS_DISP_MAILBOX_IN_DATA
ShortName:	TCSS_DISP_MAILBOX_IN_DATA
Reset:	global

DE to IOM Mailbox

DWord	Bit	Description
0	31:0	**DATA** Access: R/W Mailbox data

TCSS_DISP_MAILBOX_OUT_CMD

TCSS_DISP_MAILBOX_OUT_CMD

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	3710A8h-3710ABh
Name:	TCSS_DISP_MAILBOX_OUT_CMD
ShortName:	TCSS_DISP_MAILBOX_OUT_CMD
Reset:	global

IOM to DE Mailbox

DWord	Bit	Description
0	31	**RUN_BUSY** Access: R/W Run/Busy Value / Name: 0b; 1b
	30:24	**Reserved** Access: RO Format: MBZ
	23:16	**PARAM2** Access: R/W Parameter 2
	15:8	**PARAM1** Access: R/W Parameter 1
	7:0	**CMD** Access: R/W Command or completion code

TCSS_DISP_MAILBOX_OUT_DATA

TCSS_DISP_MAILBOX_OUT_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	3710ACh-3710AFh
Name:	TCSS_DISP_MAILBOX_OUT_DATA
ShortName:	TCSS_DISP_MAILBOX_OUT_DATA
Reset:	global

IOM to DE Mailbox

DWord	Bit	Description
0	31:0	**DATA** Access: R/W Mailbox data

Thread Dispatched Count Register

TDL_THR_DISP_COUNT - Thread Dispatched Count Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	0E4BCh

This register provides the count of threads dispatched/valid in the subslice.

DWord	Bit	Description
0	31:6	**Reserved** Access: RO Format: MBZ
	5:0	**Thread Count** Access: RO Value: 0-56 — Name: Valid Range

Thread Faulted Count Register

TDL_THR_PF_COUNT - Thread Faulted Count Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	0E5BCh

This register provides the count of threads faulted in each subslice.

DWord	Bit	Description
0	31	**Canonical fault indication bit to CS** Access: RO The bit is set when a canonical fault on data fetch is reported by EU.
	30:6	**Reserved** Access: RO Format: MBZ
	5:0	**Thread Count** Access: RO Value: 0-56 — Name: Valid Range

Thread Fault Status Register 0

TDL_THR_PF_STATUS0 - Thread Fault Status Register 0	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	0E6B8h

This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.

DWord	Bit	Description
0	31:24	**Row0, EU3, [Reserved, T6-T0]** Access: RO
	23:16	**Row0, EU2, [Reserved, T6-T0]** Access: RO
	15:8	**Row0, EU1, [Reserved, T6-T0]** Access: RO
	7:0	**Row0, EU0, [Reserved, T6-T0]** Access: RO

Thread Fault Status Register 1

TDL_THR_PF_STATUS1 - Thread Fault Status Register 1	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	0E7B8h

This register provides the status of each thread in the SubSlice. A bit set indicates the thread in the specific thread slot is faulted.

DWord	Bit	Description
0	31:24	**Row1, EU3, [Reserved, T6-T0]** Access: RO
	23:16	**Row1, EU2, [Reserved, T6-T0]** Access: RO
	15:8	**Row1, EU1, [Reserved, T6-T0]** Access: RO
	7:0	**Row1, EU0, [Reserved, T6-T0]** Access: RO

Thread Load Status Register 0

TDL_THR_STATUS0 - Thread Load Status Register 0			
Register Space:	MMIO: 0/2/0		
Access:	RO		
Size (in bits):	32		
Address:	0E4B8h		
This register provides the status of each thread in the SubSlice.			
DWord	**Bit**	**Description**	
0	31:24	**Row0, EU3, [T7-T0]**	
		Access:	RO
	23:16	**Row0, EU2, [T7-T0]**	
		Access:	RO
	15:8	**Row0, EU1, [T7-T0]**	
		Access:	RO
	7:0	**Row0, EU0, [T7-T0]**	
		Access:	RO

Thread Load Status Register 1

TDL_THR_STATUS1 - Thread Load Status Register 1	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	0E5B8h

This register provides the status of each thread in the SubSlice. A bit set indicates a valid thread is loaded in the thread slot.

DWord	Bit	Description
0	31:24	**Row1, EU3, [Reserved, T6-T0]** Access: RO
	23:16	**Row1, EU2, [Reserved, T6-T0]** Access: RO
	15:8	**Row1, EU1, [Reserved, T6-T0]** Access: RO
	7:0	**Row1, EU0, [Reserved, T6-T0]** Access: RO

Thread Mode Register

FF_MODE - Thread Mode Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	06210h-06213h
Name:	Thread Mode Register
ShortName:	FF_MODE_SVGUNIT
Address:	17210h-17213h
Name:	Thread Mode Register
ShortName:	FF_MODE_SVGRUNIT

This register is used to program the FF shader Mode.

DWord	Bit	Description
0	31	**TE Autostrip Disable** Access: R/W Format: U1 0h – Enable **[Default]** – TE will generate "autostrip" primitives (if/where possible) during tessellation. 1h – Disable – TE will not generate "autostrip" primitives.
	30	**TDS external Cache Disable** Access: R/W 0b – Enable **[Default]** – The external TDS Cache is enabled if there is enough handles to enable the cache. 1b – Disable – The external TDS Cache is disabled even if there is enough handles to enable the cache. Only the internal TDS Cache will be used.
	29:26	**DS Hit Max Value** Access: R/W Format: U4 If the number of hits reaches the DS Hit Max Value and there is a pending miss to be dispatched, the DS will dispatch the pending miss vertex as a single dispatch. Programming a value of 0 will disable the DS Hit Max counter logic and therefore partial dispatches will not be forced due to the number of hits seen during the accumulation of inputs

for a thread dispatch.

Value	Name
15	**[Default]**
[0,15]	

25:20 **VS Hit Max Value**

Access:	R/W
Format:	U6

If the number of hits reaches the VS Hit Max Value and there is a pending miss to be dispatched, the VS will dispatch the pending miss vertex as a single dispatch.

Since VS Reference Count Full Force miss enable was removed, the value can be [1,63].

Value	Name
10	**[Default]**
[1,63]	

19 **Tessellation DOP gating Disable**

Access:	R/W
Format:	Disable

Value	Name	Description
0h	Enable **[Default]**	HS, TE, TETG, DS, GS and SOL units are DOP gated if all units are disabled
1h	Disable	DOP gating is disabled for HS, TE, TETG, DS, GS and SOL units

Programming Notes
Once this bit is set to a 1, it must not be cleared to a 0 until after a reset.

18 **TRI NOINSIDE Autostrip Cache Invalidate Disable**

Access:	R/W
Format:	Disable

This bit can be used to control the TRI NOINSIDE Autostrip Cache Invalidate feature. By default the invalidation is ENABLED (allowing higher performance).

Value	Name	Description
0h	Enable **[Default]**	TE will suppress the Autostrip cache invalidate for TRI NOINSIDE patches. This setting may improve performance.
1h	Disable	TE will not suppress the Autostrip cache invalidate for TRI NOINSIDE patches.

FF_MODE - Thread Mode Register

		Programming Notes The setting of this field impacts the selection of the "provoking vertex" for the center triangle of TRI domains (if a center triangle exists given the tessellation factors), and this will in turn impact the generated image if any PS attributes are enabled as "flat shaded" and that/those attributes are not identical on all 3 vertices of the triangle. Given the fact that the APIs do not impose requirements on the starting/provoking vertices of the tessellation-generated triangles, the selection of provoking vertices can be arbitrary as long as it is deterministic (i.e., repeated rendering the same patch will yield the same results). Note: If FF_mode.TE autostrip Disable is set to 1, then TRI NOINSIDE Autostrip Cache Invalidate will also be disabled.
	17	**Thread fusing disable** Access: R/W **Value** / **Name** / **Description** 1h / Disable / Fusing of threads will be disabled. Threads will not be fused. 0h / **[Default]** / Fusing of threads will be enabled. Threads will be fused if all conditions are met to fuse a thread.
	16	**Mesh Shader Partial Autostrip Disable** Access: R/W Format: Disable **Value** / **Name** / **Description** 0h / **[Default]** / The Mesh Shader unit can generate "partial autostrip" primitives from TRILIST inputs. 1h / / The Mesh Shader unit will not generate "partial autostrip" primitives
	16:15	**Reserved** Access: R/W Format: PBC
	15	**Mesh Shader Autostrip Disable** Access: R/W Format: Disable **Value** / **Name** / **Description** 0h / **[Default]** / The mesh shader unit can generate "autostrip" primitives from TRILIST inputs. 1h / / The mesh shader unit will not generate "autostrip" primitives.
	14:13	**Reserved** Access: R/W Format: PBC

FF_MODE - Thread Mode Register

	12	**Reserved** Default Value: 0h Access: R/W Format: PBC
	11:7	**Reserved** Access: R/W Format: PBC
	6:5	**Reserved** Access: R/W Format: PBC
	4	**Reserved** Default Value: 0h Access: R/W Format: PBC
	3	**Reserved** Access: R/W Format: PBC
	2	**TDS Tracking fifo wrap fix disable** Access: R/W Format: Disable

Value	Name	Description
1h		Disable the tds tracking fifo wrap fix.
0h	**[Default]**	Enable the tds tracking fifo wrap fix.

	1	**Reserved** Access: R/W Format: PBC
	0	**Reserved** Access: R/W Format: PBC

Thread Restart Control Register

TDL_THR_RESTART - Thread Restart Control Register		
Register Space:	MMIO: 0/2/0	
Access:	WO	
Size (in bits):	32	
Address:	0E450h	
This register provides control to restart page faulted and halted threads in each subslice.		
DWord	**Bit**	**Description**
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Restart All Faulted Threads** Access: WO A write of 1 to this register restarts all threads that have halted due to page fault.

Tile 0 Posted Queue Head

TILE0_PQUEUE_HEAD - Tile 0 Posted Queue Head		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	101810h	
DWord	**Bit**	**Description**
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**Tile 0 Posted Queue Head Pointer** Default Value: 00000b Access: R/W _Custom_GTIReset: BUS Head pointer for Tile 0 16 deep posted port FIFO. Incremented by SGRunit on posted write to Tile 0.

Tile 0 Posted Queue Tail

TILE0_PQUEUE_TAIL - Tile 0 Posted Queue Tail		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	101814h	
DWord	**Bit**	**Description**
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**Tile 0 Posted Queue Tail Pointer** Default Value: 10000b Access: R/W _Custom_GTIReset: BUS Tail pointer for Tile 0 16 deep posted port FIFO.

Tile 1 Posted Queue Head

TILE1_PQUEUE_HEAD - Tile 1 Posted Queue Head		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	101820h	
DWord	**Bit**	**Description**
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**Tile 1 Posted Queue Head Pointer** Default Value: 00000b Access: R/W _Custom_GTIReset: BUS Head pointer for Tile 1 16 deep posted port FIFO. Incremented by SGRunit on posted write to Tile 1.

Tile 1 Posted Queue Tail

TILE1_PQUEUE_TAIL - Tile 1 Posted Queue Tail		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	101824h	
DWord	**Bit**	**Description**
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**Tile 1 Posted Queue Tail Pointer** Default Value: 10000b Access: R/W _Custom_GTIReset: BUS Tail pointer for Tile 1 16 deep posted port FIFO.

Tile 2 Posted Queue Head

TILE2_PQUEUE_HEAD - Tile 2 Posted Queue Head		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	101830h	
DWord	**Bit**	**Description**
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**Tile 2 Posted Queue Head Pointer** Default Value: 00000b Access: R/W _Custom_GTIReset: BUS Head pointer for Tile 2 16 deep posted port FIFO. Incremented by SGRunit on posted write to Tile 2.

Tile 2 Posted Queue Tail

TILE2_PQUEUE_TAIL - Tile 2 Posted Queue Tail		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	101834h	

DWord	Bit	Description
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**Tile 2 Posted Queue Tail Pointer** Default Value: 10000b Access: R/W _Custom_GTIReset: BUS Tail pointer for Tile 2 16 deep posted port FIFO.

Tile 3 Posted Queue Head

TILE3_PQUEUE_HEAD - Tile 3 Posted Queue Head		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	101840h	
DWord	**Bit**	**Description**
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**Tile 3Posted Queue Head Pointer** Default Value: 00000b Access: R/W _Custom_GTIReset: BUS Head pointer for Tile 3 16 deep posted port FIFO. Incremented by SGRunit on posted write to Tile 3.

Tile 3 Posted Queue Tail

TILE3_PQUEUE_TAIL - Tile 3 Posted Queue Tail		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	101844h	
DWord	**Bit**	**Description**
0	31:5	**Reserved** Access: RO Format: MBZ
	4:0	**Tile 3 Posted Queue Tail Pointer** Default Value: 10000b Access: R/W _Custom_GTIReset: BUS Tail pointer for Tile 3 16 deep posted port FIFO.

Tile Cache Control Register

TCCNTLREG - Tile Cache Control Register	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0B138h
Name:	Tile Cache Control Register
ShortName:	TCCNTLREG
Address:	0B238h
ShortName:	TCCNTLREG_CCS0

DWord	Bit	Description
0	31:25	**Unified Tile Cache Pool** Default Value: 00h Access: R/W Number of ways allocated for the unified client pool. This is a combined pool for all streams.
	24:18	**Z Tile Cache Pool** Default Value: 00h Access: R/W Number of ways allocated for Z streams.
	17:11	**C Tile Cache Pool** Default Value: 00h Access: R/W Number of ways allocated for Color Streams
	10:4	**Command Streamer Allocation** Default Value: 00h Access: R/W Number of ways allocated for CS(Command Streamer)
	3	**State cache redirect to CS section Enable** Access: R/W Format: Enable Enables the redirection of the state cache from the Unified/RO sections of the L3 to the CS Command buffer section

TCCNTLREG - Tile Cache Control Register

Value	Name	Description
1	**[Default]**	Enables the re-direction
0		Disables the re-direction. State lines will be cached into RO/L3 rest section of the cache.

2 **L3 Data partial write merging enable**

Default Value:	1
Access:	R/W
Format:	Enable

1 **Color/Z write partial write merging enable**

Access:	R/W
Format:	Enable

Value	Name	Description
0	**[Default]**	Partial write merging optimization (in SQDB) will be disabled for Color/Z bound cycles.

0 **Reserved**

Access:	RO
Format:	MBZ

TiledResources Invalid Tile Detection Register

TRINVTILEDETCT - TiledResources Invalid Tile Detection Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	04DECh
Name:	TiledResources Invalid Tile Detection Register
ShortName:	TRINVTILEDETCT

DWord	Bit	Description
0	31:0	**Invalid Tile Detection Value** Access: R/W _Custom_GTIReset: DEV **Value** / **Name** / **Description** 00000000h / **[Default]** / A 32-bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Invalid Tiles. Hardware will flag each entry and space behind it as Invalid Tile for matched entries.

TiledResources VA Detection Registers

TRVADR - TiledResources VA Detection Registers

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	04DF0h
Name:	TiledResources VA Detection Registers
ShortName:	TRVADR

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:4	**TR - VA Mask Value** Default Value: 0000b Access: R/W _Custom_GTIReset: DEV 4bit MASK value that is mapped to incoming address bits[47:44] MASK bits are used to identify which address bits need to be considered for compare. If particular mask bit is "1", mapping address bit needs to be compared to DATA value provided. If "0", corresponding address bit is masked which makes it don't care for compare. (This field defaults to "0000" to disable detection.). Note: The only usage model for GFX driver to set this field to "1111". Behavior of h/w for any other setting is not defined. Note: GFX driver shall use same TRVA MASK value for all contexts.
	3:0	**TR- VA Data Value** Access: R/W _Custom_GTIReset: DEV

Value	Name	Description
0000b	**[Default]**	4bit Data value that is mapped to incoming address bits[47:44]. Data bits are used to compare address values that are not filtered by the TRVAMV for match Note: GFX driver shall use same TRVA Data value for all contexts

Tiled Resources Wrapper Write Data Port arbitration

TRWRPARB - Tiled Resources Wrapper Write Data Port arbitration

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	04DF8h
Name:	Tiled Resources Wrapper Write Data Port arbitration
ShortName:	TRWRPARB

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ
	12:10	**L3 Max Write Request Limit Count** Default Value: 100b Access: R/W _Custom_GTIReset: DEV This is the MAX number of Allowed writes from L3 before switching the priority to Z Requests Count - Minimum count value must be 1
	9	**Reserved** Access: RO Format: MBZ
	8:6	**Z Max Write Request Limit Count** Default Value: 010b Access: R/W _Custom_GTIReset: DEV This is the MAX number of Allowed writes from Z before switching the priority to C Requests Count - Minimum count value must be = 1
	5	**Reserved** Access: RO Format: MBZ
	4:2	**C Max Write Request Limit Count** Default Value: 010b Access: R/W _Custom_GTIReset: DEV This is the MAX number of Allowed writes from C before switching to L3 Request Count - Minimum count value = 1

TRWRPARB - Tiled Resources Wrapper Write Data Port arbitration

	1	**Reserved** Access: RO Format: MBZ
	0	**Fixed Arbitration enable** Default Value: 1b Access: R/W _Custom_GTIReset: DEV Fixed Arbitration enable when 1'b1 Programmable arbitration when 1'b0

TIMESTAMP_CTR

TIMESTAMP_CTR	
Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	44070h-44073h
Name:	Time Stamp Counter
ShortName:	TIMESTAMP_CTR
Reset:	global

The register is not reset by a FLR.

DWord	Bit	Description
0	31:0	**TIMESTAMP Counter** Access: R/WC This field increments every microsecond. The value in this field is latched in the Pipe Flip TIMESTAMP registers when flips occur, and in the Pipe Frame TIMESTAMP registers at start of vertical blank. The register value will reset if any value is written to it. The register is not reset by a FLR.

TLB Inval Descriptor A

TLB_INV_DESC_A - TLB Inval Descriptor A

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CF7Ch

This register defines the TLB invalidation descriptor (first of the 3 parts) for driver initiated TLB invalidations. This part of the descriptor must be written after the other two parts, as writing [0] of this register triggers the invalidation flow.

DWord	Bit	Description
0	31:12	**Address Low** Default Value: 00000h Access: R/W This is the PPGTT Virtual Address[31:12] of the page or page range that needs to be invalidated in the TLBs for the context specified by PASID/VF on page selective invalidations. The address is a 4K aligned address. For non page-selective-invalidations, this field is ignored.
	11:10	**Reserved** Access: RO Format: MBZ
	9	**Invalidation Mode** Default Value: 0b Access: R/W Specifies Light or Heavy Invalidation mode. **0: Heavy Invalidation Mode:** This is the normal legacy invalidation mode. The pipeline of the engine(s) for which the invalidation is targeted to is blocked, and all the in-flight transactions are guaranteed to be Globally Observed before completing the TLB invalidation. **1: Light Invalidation Mode:** TLBs of the targeted engine(s) are immediately invalidated. In-flight transactions are NOT guaranteed to be Globally Observed before completing TLB invalidation. Light Invalidation Mode is to be used only when it can be guaranteed (by SW) that the address translations remain invariant for the in-flight transactions across the TLB invalidation. In other words, this mode can be used when the TLB invalidation is intended to clear out the stale cached translations that are no longer in use. Light Invalidation Mode is much faster than the Heavy Invalidation Mode, as it does not wait for the in-flight transactions to be GOd.
	8:3	**Address Mask** Default Value: 00h Access: R/W For page selective invalidations, this specifies the number of contiguous PPGTT pages that needs to be invalidated. The value in this field specifies the number of low order bits of the ADDR field that must be masked for the invalidation operation. This field enables SW to request invalidation

TLB_INV_DESC_A - TLB Inval Descriptor A

		of contiguous mappings for size-aligned regions. When invalidating a large-page translation, SW must use the appropriate Address Mask value (0 for 4KB page, 4 for 64KB page, 9 for 2M page). For non page selective invalidations, this field is ignored.
	2:1	**Granularity** Default Value: 00b Access: R/W This field indicates the requested invalidation granularity. HW implementations may perform coarser invalidation than the granularity requested. **00: All-mappings-within-all-PASID/VF:** All TLB entries for all PASIDs/VFs are invalidated. This essentially invalidates all the TLBs in GAM. **01: Reserved** **10: All-mappings-within-PASID/VF:** All TLB entries for the PASID/VF specified are invalidated. This results in invalidating all the TLB entries for one or more engines whose PASID/VF matches with than in the invalidation descriptor. **11: Page-Selective-within-PASID/VF:** TLB entries that fall in the address range specified by ADDR/AM fields for the specified PASID/VF are invalidated.
	0	**Valid** Default Value: 0b Access: R/W TLB Invalidation Descriptor (all 3 parts) are valid. This triggers the TLB invalidation flow This bit self clears.

TLB Inval Descriptor B

TLB_INV_DESC_B - TLB Inval Descriptor B

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CF80h

This register defines the TLB invalidation descriptor (Second of the 3 parts) for driver initiated TLB invalidations.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Address Hi** Default Value: 0000h Access: R/W This is the PPGTT Virtual Address[48:32] of the page or page range that needs to be invalidated in the TLBs for the context specified by PASID/VF on page selective invalidations. The address is a 4K aligned address. For non page-selective-invalidations, this field is ignored.

TLB Inval Descriptor C

TLB_INV_DESC_C - TLB Inval Descriptor C

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CF84h

This register defines the TLB invalidation descriptor (Third of the 3 parts) for driver initiated TLB invalidations.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:6	**PASID Hi** Default Value: 00000h Access: R/W This is used only with SIOV. When SIOV is enabled, PASID_Hi field holds the PASID[19:6] of the context for which the invalidation is intended for.
	5:0	**VF Number** Default Value: 00h Access: R/W When SRIOV is enabled, VF field holds the 6 bit VF number of the context for which the invalidation is intended for. Any engine that is currently running under the specified VF will go through the TLB invalidation, as specified in the invalidation descriptor. Any engine running under a different VF is not affected. When SIOV is enabled, this field holds the PASID[5:0] of the context for which the invalidation is intended for.

TLBInvalidationRegister_BLT

BLT_TLB_INV_CR - TLBInvalidationRegister_BLT	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CEE4h
Name:	BLT TLB Invalidation Register
ShortName:	BLT_TLB_INV_CR

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ

TLBInvalidationRegister_GFX

GFX_TLB_INV_CR - TLBInvalidationRegister_GFX

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CED8h
Name:	GFX TLB Invalidation Register
ShortName:	GFX_TLB_INV_CR

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

TLBInvalidationRegister_GUC

GUC_TLB_INV_CR - TLBInvalidationRegister_GUC

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
_Custom_GTIHardWiredEnable:	clr_reg_ga_cee8

Address:	0CEE8h
Name:	GUC TLB Invalidation Register
ShortName:	GUC_TLB_INV_CR
_Custom_GTIHardWiredEnable:	clr_reg_ga_cee8

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

TLBInvalidationRegister_OA

OA_TLB_INV_CR - TLBInvalidationRegister_OA

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CEECh
Name:	OA TLB Invalidation Register
ShortName:	OA_TLB_INV_CR

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Invalidate TLBs on the corresponding Engine** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated engine and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs. This bit is self clear.

Top of Low Usable DRAM Register

TOLUD_REG - Top of Low Usable DRAM Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	108000h

This 32 bit register defines the Top of Low Usable DRAM. GT uses this to ensure no GT memory accesses occur between 4GB and TOLUD.

DWord	Bit	Description
0	31:20	**TOLUD** Default Value: 001h Access: R/W _Custom_GTIReset: BUS This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. BIOS must set this value. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register.
	19:0	**Reserved** Access: RO Format: MBZ

Total Local Memory

TOTAL_LOCAL_MEMORY - Total Local Memory

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	108430h

Indicates the maximum PCIe LMEMBAR sizes in the PF and VF resize-able BAR capability structures.

DWord	Bit	Description
0	31:9	**Reserved** Access: RO Format: MBZ
	8	**Local memory 512GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Indicates 512GB
	7	**Local memory 256GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Indicates 256GB
	6	**Local memory 128GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Indicates 128GB
	5	**Local memory 64GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Indicates 64GB
	4	**Local memory 32GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS

TOTAL_LOCAL_MEMORY - Total Local Memory

		Indicates 32GB
	3	**Local memory 16GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Indicates 16GB
	2	**Local memory 8GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Indicates 8GB
	1	**Local memory 4GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Inidicates 4GB
	0	**Local memory 2GB** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Indicates 2GB

TOUUD_LSB_REG

TOUUD_LSB_REG - TOUUD_LSB_REG

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	108080h

This 64 bit register defines the Top of Upper Usable DRAM. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB. BIOS Restriction: Minimum value for TOUUD is 4GB.
All the bits in this register have SAI policy group protection.

DWord	Bit	Description
0	31:20	**TOUUD** Default Value: 001h Access: R/W _Custom_GTIReset: BUS This register contains the LSB portion (bits 31 to 20) of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB.
	19:1	**Reserved** Access: RO Format: MBZ
	0	**SPARE** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Was lock bit prior

TOUUD_MSB_REG

TOUUD_MSB_REG - TOUUD_MSB_REG		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	108084h	
This is the most significant 32 bits of a 64 bit register that defines the Top of Upper Usable DRAM. BIOS Restriction: Minimum value for TOUUD is 4GB.		
DWord	**Bit**	**Description**
0	31:0	**TOUUD** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS This register contains bits 63 to 32 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system.

TRANS_CLK_SEL

TRANS_CLK_SEL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	46140h-46143h
Name:	Transcoder A Clock Select
ShortName:	TRANS_CLK_SEL_A
Reset:	soft
Address:	46144h-46147h
Name:	Transcoder B Clock Select
ShortName:	TRANS_CLK_SEL_B
Reset:	soft
Address:	46148h-4614Bh
Name:	Transcoder C Clock Select
ShortName:	TRANS_CLK_SEL_C
Reset:	soft
Address:	4614Ch-4614Fh
Name:	Transcoder D Clock Select
ShortName:	TRANS_CLK_SEL_D
Reset:	soft

This register maps the port clock to the transcoder.

DWord	Bit	Description
0	31:28	**Trans Clock Select** Access: R/W Select which DDI clock to use for this transcoder. Restriction : This must not be changed while the transcoder is enabled.

Value	Name
0000b	None - Clock Disabled
0001b	DDI A
0010b	DDI B
0011b	DDI C
0100b	DDI D
0101b	DDI E
0110b	DDI USBC1

TRANS_CLK_SEL

		0111b	DDI USBC2
		1000b	DDI USBC3
		1001b	DDI USBC4
	27:0	**Reserved**	
		Access:	RO
		Format:	MBZ

TRANS_CONF

TRANS_CONF	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of vertical blank (WD cap sync) OR transcoder disabled
Address:	7E008h-7E00Bh
Name:	Transcoder WD0 Configuration
ShortName:	TRANS_CONF_WD0
Reset:	soft
Address:	7D008h-7D00Bh
Name:	Transcoder WD1 Configuration
ShortName:	TRANS_CONF_WD1
Reset:	soft
Address:	7B008h-7B00Bh
Name:	Transcoder DSI 0 Configuration
ShortName:	TRANS_CONF_DSI0
Reset:	soft
Address:	7B808h-7B80Bh
Name:	Transcoder DSI 1 Configuration
ShortName:	TRANS_CONF_DSI1
Reset:	soft
Address:	70008h-7000Bh
Name:	Transcoder Configuration
ShortName:	TRANS_CONF_A
Reset:	soft
Address:	71008h-7100Bh
Name:	Transcoder Configuration
ShortName:	TRANS_CONF_B
Reset:	soft
Address:	72008h-7200Bh
Name:	Transcoder Configuration
ShortName:	TRANS_CONF_C
Reset:	soft
Address:	73008h-7300Bh
Name:	Transcoder Configuration

TRANS_CONF

ShortName: TRANS_CONF_D

Reset: soft

DWord	Bit	Description
0	31	**Transcoder Enable** Access: Double Buffered Setting this bit to the value of one, turns on this transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Enabling the transcoder may be internally delayed for one frame while the display data buffers are re-configured. **Value** / **Name** 0b – Disable 1b – Enable **Restriction** Timing registers must contain valid values before this bit is enabled.
	30	**Transcoder State** Access: RO This read only bit indicates the actual state of the transcoder. **Value** / **Name** 0b – Disabled 1b – Enabled
	29:23	**Reserved** Access: RO Format: MBZ
	22:21	**Interlaced Mode** Access: Double Buffered These bits control the transcoder interlaced mode. This field is ignored by WD. **Value** / **Name** / **Description** 00b – PF-PD – Progressive Fetch with Progressive Display 01b – PF-ID – Progressive Fetch with Interlaced Display 11b – IF-ID – Interlaced Fetch with Interlaced Display Others – Reserved – Reserved **Programming Notes** Progressive Fetch with Interlaced Display requires pipe scaling. **Restriction** VGA display modes do not work while in interlaced fetch mode.

TRANS_CONF

		Progressive Fetch with Interlaced Display effectively down scales the vertical by 2X, which reduces the maximum supported pixel rate by half. Interlaced fetch mode is not supported with Y Tiling. Interlaced fetch mode is not supported with 90/270 rotation. Interlaced fetch mode is not supported with scaling. Interlaced fetch mode is not supported with YUV 420 hybrid planar source pixel formats. In Interlaced mode, the plane height must be a minimum of 2 scanlines.
	20:12	**Reserved** Access: RO Format: MBZ
	11:8	**Reserved** Access: Double Buffered
	7	**Reserved** Access: Double Buffered
	6:2	**Reserved** Access: RO Format: MBZ
	1:0	**Early pixel count scaling** Access: Double Buffered The hblank_early is generated on data timing (not the timing generator), so different factors such as the VDSC output bpp can shift the position of hblank_early relative to hblank. This 2-bit register field per transcoder within non-audio register space for early pixel count scaling provides guard bandwith to help insure that the actual position is at least greater than or equal to the value requested in AUD_CONFIG_BE.

Value	Name	Description
00b	Scale x2	Scale the AUD_CONFIG_BE early pixel count by x2
01b	Scale x4	Scale the AUD_CONFIG_BE early pixel count by x4
10b	Scale x8	Scale the AUD_CONFIG_BE early pixel count by x8
11b	Scale x1	Disable Scaling of AUD_CONFIG_BE early pixel count (x1)

TRANS_DDI_FUNC_CTL

TRANS_DDI_FUNC_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B400h-6B403h
Name:	Transcoder DSI 0 DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_DSI0
Reset:	soft
Address:	6BC00h-6BC03h
Name:	Transcoder DSI 1 DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_DSI1
Reset:	soft
Address:	60400h-60403h
Name:	Transcoder DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_A
Reset:	soft
Address:	61400h-61403h
Name:	Transcoder DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_B
Reset:	soft
Address:	62400h-62403h
Name:	Transcoder DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_C
Reset:	soft
Address:	63400h-63403h
Name:	Transcoder DDI Function Control
ShortName:	TRANS_DDI_FUNC_CTL_D
Reset:	soft

DWord	Bit	Description
0	31	**TRANS DDI Function Enable** Access: R/W This bit enables the transcoder DDI function. 0b: Disable 1b: Enable

TRANS_DDI_FUNC_CTL

30:27 **DDI Select**

Access:	R/W

These bits determine which DDI port this transcoder will connect to. It is not valid to enable and direct more than one transcoder to one DDI, except when using DisplayPort multistreaming.

This field is ignored by the DSI transcoders since they have a fixed DDI mapping.

Value	Name
0000b	None
0001b	DDI A
0010b	DDI B
0011b	DDI C
0100b	DDI USBC1
0101b	DDI USBC2
0110b	DDI USBC3
0111b	DDI USBC4
1000b	DDI D
1001b	DDI E

Restriction
This field must not be changed while the function is enabled.

26:24 **TRANS DDI Mode Select**

Access:	R/W

This field determines the mode of operation. HDMI mode enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1, and also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. DVI mode will function as HDMI if DIP packets or audio are enabled.

This field does not apply to the DSI transcoder.

Value	Name	Description
000b	HDMI	Function in HDMI mode
001b	DVI	Function in DVI mode
010b	DP SST	Function in DisplayPort SST mode
011b	DP MST	Function in DisplayPort MST mode
100b	DP2.0 32b symbol mode	Function is selected only in DisplayPort 2.0 128b/132b mode.
Others	Reserved	Reserved

TRANS_DDI_FUNC_CTL

Restriction
This field must not be changed while the function is enabled. The DisplayPort mode (SST or MST) selected here must match the mode selected in the DisplayPort Transport Control register for the transport attached to this transcoder.
Trans DDI mode select should be programmed to MST in the same register write as MST transport select (field [11:10] in this register).

23 **Reserved**

Access:	RO
Format:	MBZ

22:20 **Bits Per Color**

Access:	R/W

This field selects the number of bits per color output on the DDI connected to this transcoder. Dithering should be enabled when selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.
This field does not apply to the DSI transcoder. The Pixel Format for the DSI transcoder is defined within the TRANS_DSI_FUNC_CONF register.

Value	Name	Description
000b	8 bpc	
001b	10 bpc	
010b	6 bpc	
011b	12 bpc	
Others	Reserved	Reserved

Restriction
This field must not be changed while the function is enabled.
6bpc not supported with HDMI.
6bpc not supported with VDSC.

19:18 **Reserved**

Access:	RO
Format:	MBZ

17:16 **Sync Polarity**

Access:	R/W

This field indicates the polarity of Hsync and Vsync.
Field ignored by the DSI transcoder

TRANS_DDI_FUNC_CTL

Value	Name	Description
00b	Low	VS and HS are active low (inverted)
01b	VS Low, HS High	VS is active low (inverted), HS is active high
10b	VS High, HS Low	VS is active high, HS is active low (inverted)
11b	High **[Default]**	VS and HS are active high

15 **Reserved**

Access:	RO
Format:	MBZ

14:12 **DSI Input Select**

Access:	R/W

These bits determine the input to transcoder DSI. These bits are ignored by the other transcoders.

Value	Name
000b	Pipe A
101b	Pipe B
110b	Pipe C
111b	Pipe D
Others	Reserved

Restriction
This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.

11:10 **MST Transport Select**

Access:	R/W

Description
This field selects which DP transport the DP data from this transcoder is sent to for MST stream combining. This field is ignored when MST is disabled.
Restriction : MST transport select should be programmed in the same register write as Trans DDI mode select (field [26:24] in this register).
This field is required to be programmed in DP 2.0 128b/132b case as well.

Value	Name
00b	DPTP A
01b	DPTP B
10b	DPTP C
11b	DPTP D

TRANS_DDI_FUNC_CTL

Restriction
This field must not be changed while the function is enabled.

9 Reserved

Access:	R/W

8 DP VC Payload Allocate

Access:	R/W

Description
This bit enables DisplayPort Virtual Channel payload allocation. This bit is ignored by transcoder EDP since it does not support multistreaming.
This bit is ignored by transcoder DSI since it does not support multistreaming
This field is required to be programmed for DP2.0 128b/132b use case as well.

Value	Name
0b	Disable
1b	Enable

7 HDMI Scrambler CTS Enable

Access:	R/W

This bit enables Compliance Test Specification mode on the HDMI scrambler. This bit must be set before the scrambler is enabled.
This bit is ignored by transcoder DSI

Value	Name
0b	Disable
1b	True

6 HDMI Scrambler Reset frequency

Access:	R/W

This bit specifies the frequency at which the scrambler is reset when the HDMI Scrambler CTS Enable bit is set.
This bit must be set before or along with the HDMI Scrambler CTS Enable bit.

Value	Name	Description
0b	Every Line	SSCP sent on hsync of every line
1b	Every Other Line	SSCP sent on hsync of every other line

5 Reserved

Access:	R/W

4 High TMDS Char Rate

Access:	R/W

TRANS_DDI_FUNC_CTL

This field enables the high TMDS character rate. It must be enabled when the HDMI link symbol rate is greater than 340 MHz. It must be disabled when the HDMI link symbol rate is less than or equal to 340 MHz.

Value	Name	Description
0	Disable	TMDS Character Rate is less than or equal to 340 Mega-characters/second/channel
1	Enable	TMDS Character Rate is greater than 340 Mega-characters/second/channel

3:1 **Port Width Selection**

Access:	R/W

Description
This field selects the number of lanes to be enabled on the DDI link for DisplayPort and DSI. for DSI, this field specifies the number of Data lanes to use - the Clock lane is always enabled when the DSI function is enabled. This field is ignored for HDMI and DVI which always use all 4 lanes. The value selected here must match the value selected in the DDI Buffer Control register for the DDI attached to this pipe.

Value	Name	Description
000b	x1	x1 Mode
001b	x2	x2 Mode
010b	x3	[] x3 Mode (DSI only)
011b	x4	x4 Mode
Others	Reserved	Reserved

Restriction
This field must not be changed while the DDI is enabled.

0 **HDMI Scrambling Enabled**

Access:	R/W

Setting this bit enables scrambling over the HDMI link.
Scrambling must be enabled when the HDMI link symbol rate is greater than 340 MHz.
Scrambling should be enabled at lower frequencies if the receiver supports it at that speed.
This must not changed while the port is enabled.

Value	Name
0b	Disable
1b	Enable

TRANS_DDI_FUNC_CTL2

TRANS_DDI_FUNC_CTL2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B404h-6B407h
Name:	Transcoder DSI 0 DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_DSI0
Reset:	soft
Address:	6BC04h-6BC07h
Name:	Transcoder DSI 1 DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_DSI1
Reset:	soft
Address:	60404h-60407h
Name:	Transcoder DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_A
Reset:	soft
Address:	61404h-61407h
Name:	Transcoder DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_B
Reset:	soft
Address:	62404h-62407h
Name:	Transcoder DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_C
Reset:	soft
Address:	63404h-63407h
Name:	Transcoder DDI Function Control2
ShortName:	TRANS_DDI_FUNC_CTL2_D
Reset:	soft

DWord	Bit	Description
0	31	**Genlock Enable** Access: R/W Value: 1b — Name: Enable Value: 0b — Name: Disable

TRANS_DDI_FUNC_CTL2

30:29 **Genlock Mode**

Access:	R/W

Value	Name	Description
10b	Primary	Primary transcoder outputs frame sync for other transcoders to secondary to.
00b	Local Secondary	Local secondary transcoder secondaries to frame sync from a primary transcoder in the same device. The primary transcoder is selected by Port Sync Mode Primary Select.
01b	Remote Secondary	Remote secondary transcoder secondaries to frame sync from a primary transcoder in a different device.
11b	Reserved	

28 **DDI clock squash**

Access:	R/W

This field must not be set when DE Shim register SNPS_PHY_MPLLB_DIV[dp_shim_div32_clk_sel] is set.
SW must ensure that both DDI clock squashing and DIV32 setting at DE Shim level match MPLLB programming.
This bit should be set only for DP v2.0 mode.

Value	Name	Description
0b	DDI clock squashing disabled	Do not throttle forwarded clock at 8:5 ratio to match drain rate to PHY.
1b	DDI clock squashing enabled	Throttle forwarded clock at 8:5 ratio to match drain rate to PHY .

27:9 **Reserved**

Access:	RO
Format:	MBZ

8 **Double Buffer Vactive**

Access:	R/W

Value	Name
0b	Normal Vactive
1b	Double Buffer Vactive

7:6 **Audio Mute Override**

Access:	R/W

This field overrides audio mute signal in VBID.

Value	Name	Description
00b,01b	Do not override	
10b	Override and reset	Override audio mute bit to '0'.

11b	Override and set	Override audio mute bit to '1'.

5 Dual Pipe Sync Enable

Access:	R/W

This bit informs the DSI transcoder that while it is synchronized with another DSI transcoder, it will also be driven by a separate Pipe

Value	Name	Description
0b	Disabled	Both transcoders are being driven by a single Pipe (Dual Link - Single Pipe)
1b	Enabled	Each transcoder is being driven by a separate Pipe (Dual Link - Dual Pipe)

4 Port Sync Mode Enable

Access:	R/W

This field enables the DisplayPort port sync mode on this transcoder. This mode forces two or more transcoders to be in sync; with one transcoder primary and one or more transcoder secondaries. The primary is unaware that it is operating in this mode. Only the secondary is aware that it is operating in this mode. Port sync mode is only enabled in the secondary transcoder.

For DSI, this bit enables DSI Transcoder 1 to be a secondary to DSI Transcoder 0. DSI Transcoder 0 is unaware that it is the primary of DSI Transcoder 1

Value	Name
0b	Disable
1b	Enable

Restriction
Follow the instructions for enabling and disabling Sync Mode in the Display Mode Set Sequence - Sequence for DisplayPort. Port Sync Mode Primary Select must be programmed with a valid value when Port sync Mode is enabled. The secondary and primary transcoders and associated ports must have identical parameters and properties; same color format, link width (number of lanes enabled), resolution, refresh rate, PLL configuration, dot clock, TU size, M and N programming, etc .Spread spectrum clocking cannot be used when the ports use separate PLLs.
Port Sync Mode can be enabled with DisplayPort SST and with DisplayPort MST.

3 Reserved

Access:	RO
Format:	MBZ

2:0 Port Sync Mode Primary Select

Access:	R/W

TRANS_DDI_FUNC_CTL2

Description
This field indicates which transcoder will be the primary to this transcoder when in port sync mode.
This field is ignored by the DSI transcoders since only DSI 0 can be the primary.
This field is also used for genlock for the local secondary transcoder to select a primary transcoder.

Value	Name
001b	Transcoder A
010b	Transcoder B
011b	Transcoder C
100b	Transcoder D

Restriction
A port cannot be secondaried to itself.
The DSI transcoders cannot be secondaried to a non-DSI transcoder - field ignored by the DSI transcoder.

TRANS_DP2_CTL

TRANS_DP2_CTL - TRANS_DP2_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	600A0h-600A3h
Name:	Transcoder DP2 control
ShortName:	TRANS_DP2_CTL_A
Reset:	soft
Address:	610A0h-610A3h
Name:	Transcoder DP2 control
ShortName:	TRANS_DP2_CTL_B
Reset:	soft
Address:	620A0h-620A3h
Name:	Transcoder DP2 control
ShortName:	TRANS_DP2_CTL_C
Reset:	soft
Address:	630A0h-630A3h
Name:	Transcoder DP2 control
ShortName:	TRANS_DP2_CTL_D
Reset:	soft

This register controls DP2.0 datapath.

DWord	Bit	Description
0	31	**128b_132b_channel_coding** Access: R/W Assertion of this register field to "1"enables DP v2.0 128b/132bchannel coding and associated DP v2.0 datapath. Value: 0b — disable; 1b — enable
	30	**Panel Replay enable** Access: R/W Assertion of this register field to "1" enables panel replay feature on external DP ports. Value: 0b — disable; 1b — enable

TRANS_DP2_CTL - TRANS_DP2_CTL		
	29:27	**Reserved** Access: RO Format: MBZ
	26	**Reserved** Access: RO Format: MBZ
	25:24	**Reserved** Access: RO Format: MBZ
	23	**Reserved** Access: R/W
	22:0	**Reserved** Access: RO Format: MBZ

TRANS_DP2_VFREQHIGH

TRANS_DP2_VFREQHIGH - TRANS_DP2_VFREQHIGH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	600A4h-600A7h
Name:	Transcoder DP2 VFREQ high
ShortName:	TRANS_DP2_VFREQHIGH_A
Reset:	soft
Address:	610A4h-610A7h
Name:	Transcoder DP2 VFREQ high
ShortName:	TRANS_DP2_VFREQHIGH_B
Reset:	soft
Address:	620A4h-620A7h
Name:	Transcoder DP2 VFREQ high
ShortName:	TRANS_DP2_VFREQHIGH_C
Reset:	soft
Address:	630A4h-630A7h
Name:	Transcoder DP2 VFREQ high
ShortName:	TRANS_DP2_VFREQHIGH_D
Reset:	soft

This register specifies upper 24-bits of DP v2.0 pixel clock frequency in Hz.

DWord	Bit	Description
0	31:8	**PIXELCLOCK_HIGH** Access: R/W Higher 24-bits of DP v2.0 Pixel clock frequency in Hz.
	7:0	**Reserved** Access: R/W

TRANS_DP2_VFREQLOW

TRANS_DP2_VFREQLOW - TRANS_DP2_VFREQLOW

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	600A8h-600ABh
Name:	Transcoder DP2 VFREQ low
ShortName:	TRANS_DP2_VFREQLOW_A
Reset:	soft

Address:	610A8h-610ABh
Name:	Transcoder DP2 VFREQ low
ShortName:	TRANS_DP2_VFREQLOW_B
Reset:	soft

Address:	620A8h-620ABh
Name:	Transcoder DP2 VFREQ low
ShortName:	TRANS_DP2_VFREQLOW_C
Reset:	soft

Address:	630A8h-630ABh
Name:	Transcoder DP2 VFREQ low
ShortName:	TRANS_DP2_VFREQLOW_D
Reset:	soft

This register specifies lower 24-bits of DP v2.0pixel clock frequency in Hz.

DWord	Bit	Description
0	31:8	**PIXELCLOCK_LOW** Access: R/W Lower 24-bits of DP v2.0 Pixel clock frequency in Hz.
	7:0	**Reserved** Access: R/W

TRANS_DSI_FUNC_CONF

TRANS_DSI_FUNC_CONF

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B030h-6B033h
Name:	Transcoder DSI 0 Function Configuration
ShortName:	TRANS_DSI_FUNC_CONF_0
Reset:	soft
Address:	6B830h-6B833h
Name:	Transcoder DSI 1 Function Configuration
ShortName:	TRANS_DSI_FUNC_CONF_1
Reset:	soft

This register defines the functional transcoder configuration that is specific to the DSI transcoders.

Restriction :
This register must be programmed before the DSI Transcoder function is enabled (i.e. TRANS DDI Function Enable)
The contents of this register must not be changed while the DSI Transcoder function is enabled

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:28	**Mode of Operation** Access: R/W This defines whether the DSI transcoder is in Video or Command mode. In addition to the main modes, there are two sub-modes per main mode. For the Command sub-modes, when in the "No Gate" mode, the transcoder will begin transmitting the frame pixels as soon as they are received from the Display Engine. When in the "TE Gate" mode, the transcoder will only start transmitting the frame pixels after a TE event is received. For the Video sub-modes, when in the Sync Event mode only Sync Start packets (VSS/HSS) are sent to the Periphery. When in the Sync Pulse mode, both Sync Start (VSS/HSS) and Sync End (VSE/HSE) packets are sent to the Periphery. Note that regardless of the programming of this field, until the Transcoder Enable bit is set within the TRANS_CONF_DSI register, the DSI transcoder will not generate any timing information to the Display Engine or timing packets to the Peripheral Value / Name: 00b — Command Mode (No Gate) 01b — Command Mode (TE Gate)

10b	Video Mode (Sync Event)
11b	Video Mode (Sync Pulse)

27 **TE Source**

Access:	R/W

This bit defines the source of the TE events from the Peripheral when the Transcoder is operating in Command Mode

Value	Name
0	In-band TE event source
1	Out-of-band TE event source (i.e. GPIO)

26 **TE Deglitch Enable**

Access:	R/W

When using the GPIO as the source of TE events in Command Mode, this bit will control whether the signaling from the GPIO pin is debounced or not.

Value	Name
0b	Disabled
1b	Enabled

25 **TE Accumulation**

Access:	R/W

This bit controls whether the TE events from two Panels are accumulated into a single event (usage would be for a Dual Link mode). The accumulated event will feed into the interrupt registers for each DSI transcoder pair (e.g. DSI0 and DSI1).

Value	Name
0b	Disabled
1b	Enabled

Programming Notes

1. This bit only affects the operation of the transcoder when it is operating in the Command Mode
2. It is the responsibility of Software to set this bit accordingly (i.e. it must ensure TE events are being received from both ports)
3. Even though the accumulated event is being fed to the interrupt registers of both transcoders, it is ultimately up to Software on how it enables the TE Interrupt across both transcoders
4. Hardware will automatically enable this feature (i.e. it will override the bit programming) when Periodic Frame Update and Port Sync Mode are enabled for both transcoders. Hardware will use the accumulated TE events to spawn the Frame Update Requests to each transcoder

TRANS_DSI_FUNC_CONF

24:21	**Reserved** Access: RO Format: MBZ
20	**Link Ready** Access: RO This bit advertises whether the Link is ready to receive traffic from the DSI transcoder

Value	Name
0	Link is not ready to accept traffic
1	Link is ready to accept traffic

19	**Reserved** Access: RO Format: MBZ
18:16	**Pixel Format** Access: R/W This field defines the pixel format the DSI Transcoder will be operating in

Value	Name
000b	16-bit RGB, 5-6-5
001b	18-bit RGB, 6-6-6 (Packed)
010b	18-bit RGB, 6-6-6 (Loose)
011b	24-bit RGB, 8-8-8
100b	30-bit RGB, 10-10-10
101b	36-bit RGB, 12-12-12
110b	Compressed
Others	Reserved

Restriction
When in the 18-bit RGB (Packed) pixel format, the H. Active Size must be a multiple of 4 pixels

15	**BGR Transmission** Access: R/W This field will reverse the order of the RGB channels within the pixels received from the Display Engine

Value	Name
0	Transmit order is R-G-B
1	Transmit order is B-G-R

14	**Reserved** Access: RO Format: MBZ

TRANS_DSI_FUNC_CONF

13:12 Pixel Virtual Channel

Access:	R/W

This field defines the Virtual Channel that HW will bind to all DSI packets carrying pixel data

11:10 Pixel Buffer Threshold

Access:	R/W

This field defines the threshold of buffering needed within the Pixel Buffer before the transcoder will start internally processing the pixel stream.

Value	Name
00b	The Pixel Buffer will have to be 1/4 full
01b	The Pixel Buffer will have to be 1/2 full
10b	The Pixel Buffer will have to be 3/4 full
11b	The Pixel Buffer will have to be full

9:8 Continuous Clock

Access:	R/W

This field will control the behavior of the Clock Lane and whether it is allowed to enter the LP state.
Keeping the Clock Lane running while letting the Data Lanes go in and out of the LP state keeps the LP to HS turnaround latency to a minimum, but consumes more power.
Certain panels may also require the Clock Lane to continuously run

Value	Name
00b	Always enter LP after Data Lanes
10b	Opportunistically keep Clock in HS or LP
11b	Continuous HS Clock
Others	Reserved

7 LP Clock during LPM

Access:	R/W

When the Clock Lane is configured for Continuous HS Clock, this bit will control whether the DSI transcoder places the Clock Lane into the LP state along with the Data Lanes when the per frame LP mode (LPM) is performed.
This bit has no effect ont the Clock Lane for the other Continuous Clock settings.

Value	Name	Description
0b	Disabled	Clock Lane does not follow the Data Lanes
1b	Enable	Clock Lane follows the Data Lanes

6 Reserved

Access:	RO
Format:	MBZ

TRANS_DSI_FUNC_CONF

5:4 Link Calibration

Access:	R/W

This field will control the Link calibration of the DSI Transcoder

Value	Name
00b	Calibration Disabled
10b	Calibration Enabled - Initial only
11b	Calibration Enabled - Initial and Periodic
Others	Reserved

Restriction
Calibration can be enabled for any Link frequency, but it must be enabled when the Link frequency is operating above 1.5 Gbps

3 Reserved

Access:	RO
Format:	MBZ

2 Blanking Packet during BLLP

Access:	R/W

This bit will control whether the transcoder allows the link to enter the LP state during BLLP regions (assuming there is enough time), or whether it will keep the link in the HS state with a Blanking Packet

Value	Name	Description
0b	Disabled	LP allowed in BLLP regions
1b	Enabled	Blanking packets transmitted in BLLP regions

Programming Notes
1. This bit is only applicable when the transcoder is operating in the Video Mode 2. When this bit is set, then all BLLP regions will be filled with Blanking Packets regardless of where those regions are located (i.e. Vertical active or blank) 3. Regardless of the setting of this bit, if HW determines it cannot allow the link to enter the LP state between HS bursts, then it will automatically fill the region with a Blanking Packet 4. Regardless of the setting of this bit, HW will still ensure the link enters the LP state once per frame per the DSI spec

1 S3D Orientation

Access:	R/W

This bit controls the orientation encoding of the 3DMODE field of the Stereoscopic 3D control function sent to a Panel via the Vertical Source Sync (VSS) packet when in Video Mode.

Value	Name
0b	Portrait Orientation

TRANS_DSI_FUNC_CONF

		1b: Landscape Orientation
		Programming Notes This bit will only be sampled by the transcoder when Stereoscopic 3D is enabled for the transcoder This bit should be programmed before enabling Stereoscopic 3D for the transcoder (TRANS_STEREO3D_CTL) If Software changes this bit, it must also perform a write to the TRANS_STEREO3D_CTL for the change to be sent within the next VSS This bit is only applicable when the transcoder is operating in Video Mode. If the transcoder is operating in Command Mode, then Software will have to communicate the Stereoscopic 3D function information to the Panel through a set_3D_control DCS command using the DCS Long Write DSI packet type.
	0	**EoTp Disabled** Access: R/W When set, the DSI transcoder will not transmit an End of Transmission packet at the end of High Speed bursts

Value	Name
0	EoTp Enabled
1	EoTp Disabled

TRANS_EXITLINE

TRANS_EXITLINE	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60018h-6001Bh
Name:	Transcoder DC3CO Exit Line
ShortName:	TRANS_EXITLINE_A
Reset:	soft
Address:	61018h-6101Bh
Name:	Transcoder DC3CO Exit Line
ShortName:	TRANS_EXITLINE_B
Reset:	soft
Address:	62018h-6201Bh
Name:	Transcoder DC3CO Exit Line
ShortName:	TRANS_EXITLINE_C
Reset:	soft
Address:	63018h-6301Bh
Name:	Transcoder DC3CO Exit Line
ShortName:	TRANS_EXITLINE_D
Reset:	soft

Restriction
This register should be programmed following the sequence to allow DC3co (i.e., any time before DC3co is enabled).

DWord	Bit	Description
0	31	**Enable Exit Line** Access: R/W Enable indicates idle frame reset should be applied at exit line 0b: Disable 1b: Enable
	30:13	**Reserved** Access: RO Format: MBZ

TRANS_EXITLINE		
	12:0	**Exit Line** Access: R/W This field represents the scanline at which DC3CO Exit happens. Example: DC3CO Exit time per calculation is10 scanlines SW needs to program this field as (VACTIVE - 10).

TRANS_HBLANK

TRANS_HBLANK	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60004h-60007h
Name:	Transcoder Horizontal Blank
ShortName:	TRANS_HBLANK_A
Reset:	soft
Address:	61004h-61007h
Name:	Transcoder Horizontal Blank
ShortName:	TRANS_HBLANK_B
Reset:	soft
Address:	62004h-62007h
Name:	Transcoder Horizontal Blank
ShortName:	TRANS_HBLANK_C
Reset:	soft
Address:	63004h-63007h
Name:	Transcoder Horizontal Blank
ShortName:	TRANS_HBLANK_D
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**Horizontal Blank End** Access: R/W This field specifies Horizontal Blank End position relative to the horizontal active display start. **Restriction** The minimum horizontal blank size is 32 pixels. For HDMI Audio transmission the minimum is 138 pixels. This register must always be programmed to the same value as the Horizontal Total.
	15:14	**Reserved** Access: RO Format: MBZ

TRANS_HBLANK		
	13:0	**Horizontal Blank Start** Access: R/W This field specifies the Horizontal Blank Start position relative to the horizontal active display start. **Restriction** This register must always be programmed to the same value as the Horizontal Active.

TRANS_HSYNC

TRANS_HSYNC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B008h-6B00Bh
Name:	Transcoder DSI 0 Horizontal Sync
ShortName:	TRANS_HSYNC_DSI0
Reset:	soft
Address:	6B808h-6B80Bh
Name:	Transcoder DSI 1 Horizontal Sync
ShortName:	TRANS_HSYNC_DSI1
Reset:	soft
Address:	60008h-6000Bh
Name:	Transcoder Horizontal Sync
ShortName:	TRANS_HSYNC_A
Reset:	soft
Address:	61008h-6100Bh
Name:	Transcoder Horizontal Sync
ShortName:	TRANS_HSYNC_B
Reset:	soft
Address:	62008h-6200Bh
Name:	Transcoder Horizontal Sync
ShortName:	TRANS_HSYNC_C
Reset:	soft
Address:	63008h-6300Bh
Name:	Transcoder Horizontal Sync
ShortName:	TRANS_HSYNC_D
Reset:	soft

Restriction

This register should not be changed while the transcoder or port are enabled.
HSYNC is always programmed to an even number of pixel clock cycles for YUV 4:2:0 pixel format with 10bpc and 12bpc.
HSYNC timings must be even for HDMI operating on 10bpc (regardless of format)

DWord	Bit	Description
0	31:30	**Reserved** Access: RO

TRANS_HSYNC

	Format:	MBZ

29:16 Horizontal Sync End

Access:	R/W

This field specifies the Horizontal Sync End position relative to the horizontal active display start.It is programmed with HorizontalActive+FrontPorch+Sync-1

Restriction
This value must be greater than the horizontal sync start and less than Horizontal Total.
For the DSI transcoder this field is only relevant if the transcoder is operating in Video Mode (it is ignored in Command Mode). As such, please refer to the "Determining Minimum Horizontal Blanking Regions" section of the Transcoder DSI Function page for minimum programming allowed

15:14 Reserved

Access:	RO
Format:	MBZ

13:0 Horizontal Sync Start

Access:	R/W

This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive + FrontPorch - 1

Restriction
This value must be greater than Horizontal Active for all non-DSI transcoders, or for DSI transcoders operating with non-compressed pixels in Video Mode. For DSI transcoders operating on a compressed pixel stream in Video Mode, this value should be greater than the Horizontal Active size divided by the Compression Ratio (H. Blank Start = H. Active / Compression Ratio). In HDMI modes the minimum gap between horizontal blank start and horizontal sync start is 16 pixels. For DSI transcoders, this field is only relevant if the transcoder is operating in Video Mode (it is ignored in Command Mode). When the DSI transcoder is in Video Mode, then please refer to the "Determining Minimum Horizontal Blanking Regions" section of the Transcoder DSI Function page for minimum programming allowed.

TRANS_HTOTAL

TRANS_HTOTAL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6E000h-6E003h
Name:	Transcoder WD0 Horizontal Total
ShortName:	TRANS_HTOTAL_WD0
Reset:	soft
Address:	6E800h-6E803h
Name:	Transcoder WD1 Horizontal Total
ShortName:	TRANS_HTOTAL_WD1
Reset:	soft
Address:	6B000h-6B003h
Name:	Transcoder DSI 0 Horizontal Total
ShortName:	TRANS_HTOTAL_DSI0
Reset:	soft
Address:	6B800h-6B803h
Name:	Transcoder DSI 1 Horizontal Total
ShortName:	TRANS_HTOTAL_DSI1
Reset:	soft
Address:	60000h-60003h
Name:	Transcoder Horizontal Total
ShortName:	TRANS_HTOTAL_A
Reset:	soft
Address:	61000h-61003h
Name:	Transcoder Horizontal Total
ShortName:	TRANS_HTOTAL_B
Reset:	soft
Address:	62000h-62003h
Name:	Transcoder Horizontal Total
ShortName:	TRANS_HTOTAL_C
Reset:	soft
Address:	63000h-63003h
Name:	Transcoder Horizontal Total
ShortName:	TRANS_HTOTAL_D

TRANS_HTOTAL

Reset: soft

Programming Notes

For eDP CoG: $Htotal_{COG}$ = (active pixels per segment) + (overlap pixels * number of segments/2) + Original Horizontal Blanking

Restriction

This register should not be changed while the transcoder or port are enabled.

For HDMI with YUV 4:2:0 all horizontal timings must be a multiple of 4 for 8/12/16 bpc cases and multiple of 8 for 10 bpc case.
All horizontal timings must be even for HDMI operating on 10bpc (regardless of format)

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**Horizontal Total** Access: R/W **Description** This field specifies Horizontal Total size. This field is programmed to the number of pixels desired minus one. This field is ignored by WD transcoders. This should be equal to the sum of the horizontal active and the horizontal blank sizes for all non-DSI transcoders, or for DSI transcoders operating with non-compressed pixels in Video Mode. For DSI transcoders operating with compressed pixels in Video Mode, this field should be equal to the sum of the compressed horizontal active size and the horizontal blank size (H. Total = (H. Active + H. Blank size) / Compression Ratio) For DSI transcoders operating in Command Mode, there are no restrictions on the programming of this field. **Restriction** This register must always be programmed to the same value as the Horizontal Blank End.
	15:14	**Reserved** Access: RO Format: MBZ
	13:0	**Horizontal Active** Access: R/W This field specifies Horizontal Active Display size. The first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one.

TRANS_HTOTAL		
		Restriction
		The minimum horizontal active display size is 64 pixels. In HDMI modes the minimum is 256 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.
		DSI requires a minimum Horizontal Active Display of, 256 pixels. Also, when transmitting an 18-bit RGB pixel format, the one-based size must be a multiple of 4 pixels

TRANS_MSA_MISC

TRANS_MSA_MISC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60410h-60413h
Name:	Transcoder MSA Misc
ShortName:	TRANS_MSA_MISC_A
Reset:	soft
Address:	61410h-61413h
Name:	Transcoder MSA Misc
ShortName:	TRANS_MSA_MISC_B
Reset:	soft
Address:	62410h-62413h
Name:	Transcoder MSA Misc
ShortName:	TRANS_MSA_MISC_C
Reset:	soft
Address:	63410h-63413h
Name:	Transcoder MSA Misc
ShortName:	TRANS_MSA_MISC_D
Reset:	soft

This register selects what value will be sent in the DisplayPort Main Stream Attribute (MSA) Miscellaneous (MISC) fields. The MSA MISC fields are mostly used to indicate the color encoding format and need to be programmed to indicate color space, bits per color, etc.

Programming Notes

See the DisplayPort specification for the details on what to program in these fields.

DWord	Bit	Description
0	31:16	**MSA Unused** Access: R/W This field selects the value that will be sent in the DisplayPort MSA unused fields. **Programming Notes** This should be usually programmed with all 0s.
	15:8	**MSA MISC1** Access: R/W This field selects the value that will be sent in the DisplayPort MSA MISC1 field. When TRANS_STEREO3D_CTL bit FS_MSA_MISC1_Drive_En is enabled, hardware will drive MISC1 bits 2:1 (bits 10:9 of this register) with the field sequential stereo 3D left or right eye indication, and any value written to those bits here will be ignored.

TRANS_MSA_MISC		
	7:0	**MSA MISC0** Access: R/W This field selects the value that will be sent in the DisplayPort MSA MISC0 field. **Restriction** Before enabling DisplayPort, bit 0 should always be set to 1 to indicate link clock and stream clock are synchronous.

TRANS_MULT

TRANS_MULT	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6002Ch-6002Fh
Name:	Transcoder Multiply
ShortName:	TRANS_MULT_A
Reset:	soft
Address:	6102Ch-6102Fh
Name:	Transcoder Multiply
ShortName:	TRANS_MULT_B
Reset:	soft
Address:	6202Ch-6202Fh
Name:	Transcoder Multiply
ShortName:	TRANS_MULT_C
Reset:	soft
Address:	6302Ch-6302Fh
Name:	Transcoder Multiply
ShortName:	TRANS_MULT_D
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:3	**Reserved** Access: RO Format: MBZ
	2:0	**Multiplier** Access: R/W This field specifies the data multiplier value used by HDMI and DVI.

Value	Name	Description
000b	X1	Multiply by 1
001b	X2	Multiply by 2
011b	X4	Multiply by 4
Others	Reserved	Reserved

TRANS_PUSH

TRANS_PUSH	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60A70h-60A73h
Name:	Transcoder ASFU VRR Push
ShortName:	TRANS_PUSH_A
Reset:	soft
Address:	61A70h-61A73h
Name:	Transcoder ASFU VRR Push
ShortName:	TRANS_PUSH_B
Reset:	soft
Address:	62A70h-62A73h
Name:	Transcoder ASFU VRR Push
ShortName:	TRANS_PUSH_C
Reset:	soft
Address:	63A70h-63A73h
Name:	Transcoder ASFU VRR Push
ShortName:	TRANS_PUSH_D
Reset:	soft

After programming any pipe registers in ASFU/VRR cases, Software can set push bit. H/W will sync all those updates for that frame.

DWord	Bit	Description
0	31	**Push Enable** Access: R/W This bit enables Push frame functionality. This bit should be set before ASFU/VRR enable. 0b: Disable 1b: Enable
	30	**Send Push** Access: R/W Set Writing a 1b to this field hints that Frame update is desired. Vblank is asserted at the next decision boundary. This is a sticky bit. The bit will be cleared by hardware after double buffer update. Writing a 0b has no effect.

TRANS_PUSH		
	29:0	**Reserved** Access: RO Format: MBZ

TRANS_SET_CONTEXT_LATENCY

TRANS_SET_CONTEXT_LATENCY

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6007Ch-6007Fh
Name:	Transcoder Set Context Latency
ShortName:	TRANS_SET_CONTEXT_LATENCY_A
Reset:	soft
Address:	6107Ch-6107Fh
Name:	Transcoder Set Context Latency
ShortName:	TRANS_SET_CONTEXT_LATENCY_B
Reset:	soft
Address:	6207Ch-6207Fh
Name:	Transcoder Set Context Latency
ShortName:	TRANS_SET_CONTEXT_LATENCY_C
Reset:	soft
Address:	6307Ch-6307Fh
Name:	Transcoder Set Context Latency
ShortName:	TRANS_SET_CONTEXT_LATENCY_D
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Context Latency** Access: R/W **Description** This bit field is used to specify the size of window2 (minimum delay between transcoder vblank start and the delayed vblank start) in number of scan lines. Refer to the High Refresh Rate and Small Vblank Support page for details on features that are impacted when the vblank is reduced. Use cases with DSB programming in window 2 must configure the register to enough time for the DSB to complete, in scan lines. Refer to VRR page for details. Recommendation: If DSB time will not be calculated to match the number of registers DSB programs, program this field to a value of 100 us worth of scan lines. **NOTE**: This latency register should always be programmed in conjunction with the following register field to delay vblank and create window 2.

TRANS_SET_CONTEXT_LATENCY		
		0x420C0[31] for transcoder A. 0x420C4[31] for transcoder B. 0x420C8[31] for transcoder C. 0x420D8[31] for transcoder D.

TRANS_SPACE

TRANS_SPACE	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B024h-6B027h
Name:	Transcoder DSI 0 Space
ShortName:	TRANS_SPACE_DSI0
Reset:	soft
Address:	6B824h-6B827h
Name:	Transcoder DSI 1 Space
ShortName:	TRANS_SPACE_DSI1
Reset:	soft
Address:	60024h-60027h
Name:	Transcoder Space
ShortName:	TRANS_SPACE_A
Reset:	soft
Address:	61024h-61027h
Name:	Transcoder Space
ShortName:	TRANS_SPACE_B
Reset:	soft
Address:	62024h-62027h
Name:	Transcoder Space
ShortName:	TRANS_SPACE_C
Reset:	soft
Address:	63024h-63027h
Name:	Transcoder Space
ShortName:	TRANS_SPACE_D
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:12	**Reserved** Access: RO Format: MBZ

TRANS_SPACE		
	11:0	**Vertical Active Space** Access: R/W **Description** Stereo 3D is no longer supported.

TRANS_STEREO3D_CTL

TRANS_STEREO3D_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	7B020h-7B023h
Name:	Transcoder DSI 0 Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_DSI0
Reset:	soft
Address:	7B820h-7B823h
Name:	Transcoder DSI 1 Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_DSI1
Reset:	soft
Address:	70020h-70023h
Name:	Transcoder Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_A
Reset:	soft
Address:	71020h-71023h
Name:	Transcoder Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_B
Reset:	soft
Address:	72020h-72023h
Name:	Transcoder Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_C
Reset:	soft
Address:	73020h-73023h
Name:	Transcoder Stereo 3D Control
ShortName:	TRANS_STEREO3D_CTL_D
Reset:	soft

This register is sampled one line before vertical blank.

DWord	Bit	Description
0	31	**Transcoder S3D Enable** Access: R/W **Description** Stereo 3D is no longer supported. Do not enable this field.

TRANS_STEREO3D_CTL

Value	Name
0b	Disable

30:29 **Reserved**

Access:	RO
Format:	MBZ

28:27 **S3D Mode**

Access:	R/W

This field selects between the stereo 3D modes.
The stacked buffer mode combines both stereo 3D fields (left and right eye images) into a single tall frame with the left eye image on top, then a programmable space of black lines, then the right eye image on the bottom.
The field sequential mode sends one stereo 3D field (left or right eye image) out per frame. This mode is only for use with DisplayPort. Field sequential hardware controlled mode automatically toggles between left and right eye at the start of each vertical blank. The starting field is selected using the FS_Field_Ctl register bit. Field sequential software controlled mode will manually select left or right eye using the FS_Field_Ctl register bit.

Value	Name	Description
00b	FS HW Auto	Hardware controlled auto-toggle between left and right eye on each vertical blank.
01b	FS SW Manual	Software controlled selection between left and right eye
10b	Stacked	Stacked frame mode with both left and right eye images combined in a single tall frame
Others	Reserved	Reserved

Programming Notes
In the stacked frame mode, a vertical sync is not generated in the gap between left and right eye images, and the scan line count increments across the entire tall frame.

Restriction
This field should only be changed when stereo 3D is disabled.

26 **FS Field Ctl**

Access:	R/W

The operation of this bit depends on the S3D Mode setting. This field is ignored in the S3D stacked mode.In the field sequential software controlled mode this bit selects the field sequential stereo 3D field (left or right eye).In the field sequential hardware controlled mode this bit selects the field sequential stereo 3D starting field, the field used on the frame when field sequential stereo 3D is enabled. Hardware does not wait for a specific eye when disabling.

TRANS_STEREO3D_CTL

Value	Name
0b	Right Eye
1b	Left Eye **[Default]**

Restriction
The starting field must be set to the left eye for FS HW Auto usage.

25 **Reserved**

Access:	RO
Format:	MBZ

24 **S3D Current Field**

Access:	RO

This read only bit indicates the current stereo 3D field (left or right eye).This bit should be ignored when stereo 3D is not enabled.

Value	Name
0b	Right Eye
1b	Left Eye

23 **FS MSA MISC1 Drive En**

Access:	R/W

This bit enables hardware to drive the MSA MISC1 bits 2:1 with the internal field sequential stereo 3D left/right eye field indication. Hardware will drive 00 when field sequential 3D stereo mode is not enabled, 01 when enabled and the upcoming video frame is the right eye, 11 when enabled and the upcoming video frame is the left eye. This is based on the internal left/right indication which could be either generated by hardware in the HW auto mode or by software in the SW manual mode. FS_MSA_Drive_Invert can be programmed to invert the left and right eye selection in the MSA. When this bit is disabled, software may manually program TRANS_MSA_MISC to set MISC1 bits 2:1.

Value	Name	Description
0b	Disable	Disable hardware driving MSA MISC1 bits 2:1. Allow software to manually program MSA MISC1 bits 2:1 through TRANS_MSA_MISC.
1b	Enable	Enable hardware to drive MSA MISC1 bits 2:1 for stereo 3D.

Restriction
This field should only be changed when stereo 3D is disabled and should not be enabled for the stacked frame mode.

22 **Reserved**

Access:	R/W

21:0 **Reserved**

Access:	RO
Format:	MBZ

TRANS_VBLANK

TRANS_VBLANK	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B010h-6B013h
Name:	Transcoder DSI 0 Vertical Blank
ShortName:	TRANS_VBLANK_DSI0
Reset:	soft
Address:	6B810h-6B813h
Name:	Transcoder DSI 1 Vertical Blank
ShortName:	TRANS_VBLANK_DSI1
Reset:	soft
Address:	60010h-60013h
Name:	Transcoder Vertical Blank
ShortName:	TRANS_VBLANK_A
Reset:	soft
Address:	61010h-61013h
Name:	Transcoder Vertical Blank
ShortName:	TRANS_VBLANK_B
Reset:	soft
Address:	62010h-62013h
Name:	Transcoder Vertical Blank
ShortName:	TRANS_VBLANK_C
Reset:	soft
Address:	63010h-63013h
Name:	Transcoder Vertical Blank
ShortName:	TRANS_VBLANK_D
Reset:	soft

Description
PSR ASU: This register is double buffered when Vactive double buffer bit (bit[8])is asserted in TRANS_DDI_FUNC_CTL2.
The transcoder will generate two Vertical Blanks to the Display Engine. A raw (or unmodified) V. Blank will be generated based off of the vertical timings defined within the TRANS_VTOTAL register (the raw V. Blank will assert after V.Active and de-asserted after V. Total). A delayed V. Blank will be generated from the vertical timings of this register. The delay is in terms of lines, and if this register is programmed with the same value as the TRANS_VTOTAL register (i.e. V. Blank Start = V. Active), then the delay will be zero.

TRANS_VBLANK

Programming Notes

This register is programmed in terms of lines and the values programmed should be zero-based (e.g. for the vertical blank to start on line 10, the Vertical Blank Start will be programmed to 9)

Restriction

This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Vertical Blank End** Access: R/W This field specifies Vertical Blank End position relative to the vertical active display start. **Restriction** 1. The minimum vertical blank size is 5 lines. With SRD/PSR and/or DisplayPort VDIP GMP the minimum is 8 lines 2. The V. Blank End must be programmed to the same value as V. Total in the TRANS_VTOTAL register 3. The V. Blank End must be greater than the V. Blank Start
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Vertical Blank Start** Access: R/W This field specifies the Vertical Blank Start position relative to the vertical active display start. **Restriction** The V. Blank Start must be greater than or equal to the Vertical Active programming in TRANS_VTOTAL

TRANS_VRR_CTL

TRANS_VRR_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60420h-60423h
Name:	VRR Control Register Transcoder
ShortName:	TRANS_VRR_CTL_A
Reset:	soft
Address:	61420h-61423h
Name:	VRR Control Register Transcoder
ShortName:	TRANS_VRR_CTL_B
Reset:	soft
Address:	62420h-62423h
Name:	VRR Control Register Transcoder
ShortName:	TRANS_VRR_CTL_C
Reset:	soft
Address:	63420h-63423h
Name:	VRR Control Register Transcoder
ShortName:	TRANS_VRR_CTL_D
Reset:	soft

DWord	Bit	Description
0	31	**VRR Enable** Access: R/W This bit enables/disables VRR feature on the fly, no modeset required. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30	**Ignore Max Shift** Access: R/W This bit when set to '1' will ignore programmed Vblank max shift values (both INC and DEC), allowing Vblank to freely swing between Vmin and Vmax. Value: 1b — Name: IGNORE Value: 0b — Name: DO NOT IGNORE

TRANS_VRR_CTL

	29	**Flip Line Enable** Access: R/W **Description** This bit enables/disables Flip Line feature where framestart will be generated at flip line value for VRR. Updates to this field will take effect at the next vertical blank. This field must be enabled before VRR enable. Ignore Max Shift must be set to 1 when Flip Line is enabled 0b: Disable 1b: Enable
	28:16	**Reserved** Access: RO Format: MBZ
	15:0	**VRR Guardband** Access: R/W This 16-bit line count allows a maximum of 2^16 scanlines (programming 255 gives 255 scanlines duration to fill the pipeline etc.). Restriction : Guardband = Vmin - Vactive - Window2 Refer to VRR page for details.

TRANS_VRR_FLIPLINE

TRANS_VRR_FLIPLINE	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60438h-6043Bh
Name:	VRR Flipline Trans
ShortName:	TRANS_VRR_FLIPLINE_A
Reset:	soft
Address:	61438h-6143Bh
Name:	VRR Flipline Trans
ShortName:	TRANS_VRR_FLIPLINE_B
Reset:	soft
Address:	62438h-6243Bh
Name:	VRR Flipline Trans
ShortName:	TRANS_VRR_FLIPLINE_C
Reset:	soft
Address:	63438h-6343Bh
Name:	VRR Flipline Trans
ShortName:	TRANS_VRR_FLIPLINE_D
Reset:	soft

This register defines vertical total size to execute a flip for VRR.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**VRR FLIPLINE** Access: R/W This field provides the vertical total size to execute flip for VRR. This is 0-based. So, value should be programmed as N-1.

TRANS_VRR_STATUS

TRANS_VRR_STATUS

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6042Ch-6042Fh
Name:	VRR Status Trans
ShortName:	TRANS_VRR_STATUS_A
Reset:	soft
Address:	6142Ch-6142Fh
Name:	VRR Status Trans
ShortName:	TRANS_VRR_STATUS_B
Reset:	soft
Address:	6242Ch-6242Fh
Name:	VRR Status Trans
ShortName:	TRANS_VRR_STATUS_C
Reset:	soft
Address:	6342Ch-6342Fh
Name:	VRR Status Trans
ShortName:	TRANS_VRR_STATUS_D
Reset:	soft

This register provides VRR status.

DWord	Bit	Description
0	31	**Vmax Reached** Access: R/WC Sticky bit is set indicating no flip has occurred when Vmax is reached. This bit needs to be polled and cleared by software. Setting of this sticky bit will not result in any interrupt. 0b – Not Reached 1b – Reached
	30:28	**Reserved** Access: RO Format: MBZ
	27	**VRR Enable Live** Access: RO This bit is asserted whenever pipe/plane logic is running with VRR enabled.

TRANS_VRR_STATUS

Value	Name
0b	
1b	

26	**Reserved**
Access:	RO
Format:	MBZ
25:23	**Reserved**
Access:	RO
Format:	MBZ
22:20	**Current Region in Vblank**
Access:	RO

This field indicates current status of VRR FSM.

Value	Name	Description
000b	IDLE	Timing generator disabled.
001b	SafeWindow	Wait till Push, this is also known as Window1.
010b	Guardband	This is also known as Pipeline Fill.
011b	Context Latency Delay	This is also known as Window2.
110b	Active Region	
111b	Non-VRR Vblank	No VRR

19:0	**Reserved**
Access:	RO
Format:	MBZ

TRANS_VRR_STATUS2

TRANS_VRR_STATUS2	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6043Ch-6043Fh
Name:	VRR Status2 Trans
ShortName:	TRANS_VRR_STATUS2_A
Reset:	soft
Address:	6143Ch-6143Fh
Name:	VRR Status2 Trans
ShortName:	TRANS_VRR_STATUS2_B
Reset:	soft
Address:	6243Ch-6243Fh
Name:	VRR Status2 Trans
ShortName:	TRANS_VRR_STATUS2_C
Reset:	soft
Address:	6343Ch-6343Fh
Name:	VRR Status2 Trans
ShortName:	TRANS_VRR_STATUS2_D
Reset:	soft

This register provides the live status of vertical line counter. This field should be used to issue flip during VRR Flip Line mode.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**Vertical Line Counter Status** Access: RO This field provides the live status of vertical line counter. This field should be used to issue flip during VRR Flip Line mode.

TRANS_VRR_VMAX

TRANS_VRR_VMAX	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60424h-60427h
Name:	VRR Vmax Transcoder
ShortName:	TRANS_VRR_VMAX_A
Reset:	soft
Address:	61424h-61427h
Name:	VRR Vmax Transcoder
ShortName:	TRANS_VRR_VMAX_B
Reset:	soft
Address:	62424h-62427h
Name:	VRR Vmax Transcoder
ShortName:	TRANS_VRR_VMAX_C
Reset:	soft
Address:	63424h-63427h
Name:	VRR Vmax Transcoder
ShortName:	TRANS_VRR_VMAX_D
Reset:	soft

Programming Notes

This register is not double buffered and the changed values are reflected immediately in VRR logic.
This register should not be updated while VRR mode is running.

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**VRR Vmax** Access: R/W This field provides the maximum vertical total size for VRR. This is a 0-based counter (that is, counted 0 to N-1). This field cannot be zero when VRR is enabled. Vmax= ROUNDDOWN(Dot clock / (Htotal * Min Refresh rate))

TRANS_VRR_VMAXSHIFT

TRANS_VRR_VMAXSHIFT

Register Space: MMIO: 0/2/0
Access: R/W
Size (in bits): 32

This register defines VBLANK maximum shift allowed between successive frames.

Programming Notes

This register is not double buffered and the changed values are reflected immediately in VRR logic.
This register should not be updated while VRR mode is running.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**Decrement** Access: R/W This register represents the maximum reduction.Smallest Vblank = Previous Frame Vblank End - Vblank Max Shift Decrement.
	15:14	**Reserved** Access: RO Format: MBZ
	13:0	**Increment** Access: R/W This register represents the maximum increase.Largest Vblank = Previous Frame Vblank End + Vblank Max Shift Increment.

TRANS_VRR_VMIN

TRANS_VRR_VMIN	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60434h-60437h
Name:	VRR Vmin Transcoder
ShortName:	TRANS_VRR_VMIN_A
Reset:	soft
Address:	61434h-61437h
Name:	VRR Vmin Transcoder
ShortName:	TRANS_VRR_VMIN_B
Reset:	soft
Address:	62434h-62437h
Name:	VRR Vmin Transcoder
ShortName:	TRANS_VRR_VMIN_C
Reset:	soft
Address:	63434h-63437h
Name:	VRR Vmin Transcoder
ShortName:	TRANS_VRR_VMIN_D
Reset:	soft

Programming Notes

This register is not double buffered and the changed values are reflected immediately in VRR logic.
This register should not be updated while VRR mode is running.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**VRR Vmin** Access: R/W This field provides the minimum vertical total size for VRR. This is a 0-based counter (that is, counted0 to N-1). This field cannot be zero when VRR is enabled. Vmin = ROUNDUP(Dot clock / (Htotal * Max Refresh rate))

TRANS_VRR_VSYNC

TRANS_VRR_VSYNC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60078h-6007Bh
Name:	Transcoder VRR Vertical Sync
ShortName:	TRANS_VRR_VSYNC_A
Reset:	soft
Address:	61078h-6107Bh
Name:	Transcoder VRR Vertical Sync
ShortName:	TRANS_VRR_VSYNC_B
Reset:	soft
Address:	62078h-6207Bh
Name:	Transcoder VRR Vertical Sync
ShortName:	TRANS_VRR_VSYNC_C
Reset:	soft
Address:	63078h-6307Bh
Name:	Transcoder VRR Vertical Sync
ShortName:	TRANS_VRR_VSYNC_D
Reset:	soft

Description

This register sets the position for hardware to send the adaptive sync secondary data packet (SDP). That SDP defines the position of Vsync for DP to HDMI adaptive sync (VRR) supporting protocol converters. The HDMI requirement is for Vsync to be at a fixed position from the end of the Vblank (back porch). The TRANS_VSYNC register is not used for adaptive sync SDP because it provides Vsync position relative to the start of vertical active, which changes as adaptive sync shrinks or grows the initial portion of Vblank (front porch for HDMI).

DWord	Bit	Description
0 **Programming Notes:** This register should not be changed while VRR with adaptive sync is enabled on this transcoder.	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Vertical Sync End** Access: R/W This field specifies the Vertical Sync End position relative to Vtotal. It is programmed with BackPorch.

TRANS_VRR_VSYNC		
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Vertical Sync Start** Access: R/W This field specifies the Vertical Sync Start position relative to Vtotal. It is programmed with Vsync_width+BackPorch.

TRANS_VRR_VTOTAL_PREV

TRANS_VRR_VTOTAL_PREV

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60480h-60483h
Name:	VRR Vtotal Previous Transcoder
ShortName:	TRANS_VRR_VTOTAL_PREV_A
Reset:	soft
Address:	61480h-61483h
Name:	VRR Vtotal Previous Transcoder
ShortName:	TRANS_VRR_VTOTAL_PREV_B
Reset:	soft
Address:	62480h-62483h
Name:	VRR Vtotal Previous Transcoder
ShortName:	TRANS_VRR_VTOTAL_PREV_C
Reset:	soft
Address:	63480h-63483h
Name:	VRR Vtotal Previous Transcoder
ShortName:	TRANS_VRR_VTOTAL_PREV_D
Reset:	soft

This register holds the Vtotal from previous frame and other VRR status bits. If VRR is not enabled, this register will hold software programmed Vtotal.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:20	**Reserved** Access: RO Format: MBZ
	19:0	**Vtotal Previous** Access: RO Vtotal from previous frame.

TRANS_VSYNC

TRANS_VSYNC	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B014h-6B017h
Name:	Transcoder DSI 0 Vertical Sync
ShortName:	TRANS_VSYNC_DSI0
Reset:	soft
Address:	6B814h-6B817h
Name:	Transcoder DSI 1 Vertical Sync
ShortName:	TRANS_VSYNC_DSI1
Reset:	soft
Address:	60014h-60017h
Name:	Transcoder Vertical Sync
ShortName:	TRANS_VSYNC_A
Reset:	soft
Address:	61014h-61017h
Name:	Transcoder Vertical Sync
ShortName:	TRANS_VSYNC_B
Reset:	soft
Address:	62014h-62017h
Name:	Transcoder Vertical Sync
ShortName:	TRANS_VSYNC_C
Reset:	soft
Address:	63014h-63017h
Name:	Transcoder Vertical Sync
ShortName:	TRANS_VSYNC_D
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ

TRANS_VSYNC

	28:16	**Vertical Sync End** Access: R/W This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1 **Restriction** This value must be greater than the vertical sync start and less than Vertical Total.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Vertical Sync Start** Access: R/W This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1 **Restriction** This value must be greater than Vertical Active.

TRANS_VSYNCSHIFT

TRANS_VSYNCSHIFT	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6B028h-6B02Bh
Name:	Transcoder DSI 0 Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_DSI0
Reset:	soft
Address:	6B828h-6B82Bh
Name:	Transcoder DSI 1 Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_DSI1
Reset:	soft
Address:	60028h-6002Bh
Name:	Transcoder Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_A
Reset:	soft
Address:	61028h-6102Bh
Name:	Transcoder Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_B
Reset:	soft
Address:	62028h-6202Bh
Name:	Transcoder Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_C
Reset:	soft
Address:	63028h-6302Bh
Name:	Transcoder Vertical Sync Shift
ShortName:	TRANS_VSYNCSHIFT_D
Reset:	soft

Restriction
This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:13	**Reserved** Access: RO Format: MBZ

TRANS_VSYNCSHIFT		
	12:0	**Second Field VSync Shift** Access: R/W This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is programmed to an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed = horizontal sync start - floor[horizontal total / 2]Calculate using the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers. This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

TRANS_VTOTAL

TRANS_VTOTAL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6E00Ch-6E00Fh
Name:	Transcoder WD0 Vertical Total
ShortName:	TRANS_VTOTAL_WD0
Reset:	soft
Address:	6E80Ch-6E80Fh
Name:	Transcoder WD1 Vertical Total
ShortName:	TRANS_VTOTAL_WD1
Reset:	soft
Address:	6B00Ch-6B00Fh
Name:	Transcoder DSI 0 Vertical Total
ShortName:	TRANS_VTOTAL_DSI0
Reset:	soft
Address:	6B80Ch-6B80Fh
Name:	Transcoder DSI 1 Vertical Total
ShortName:	TRANS_VTOTAL_DSI1
Reset:	soft
Address:	6000Ch-6000Fh
Name:	Transcoder Vertical Total
ShortName:	TRANS_VTOTAL_A
Reset:	soft
Address:	6100Ch-6100Fh
Name:	Transcoder Vertical Total
ShortName:	TRANS_VTOTAL_B
Reset:	soft
Address:	6200Ch-6200Fh
Name:	Transcoder Vertical Total
ShortName:	TRANS_VTOTAL_C
Reset:	soft
Address:	6300Ch-6300Fh
Name:	Transcoder Vertical Total
ShortName:	TRANS_VTOTAL_D

TRANS_VTOTAL

Reset: soft

Programming Notes

PSR ASU: This register is double buffered when Vactive double buffer bit (bit[8])is asserted in TRANS_DDI_FUNC_CTL2.

Restriction

This register should not be changed while the transcoder or port are enabled.

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:16	**Vertical Total** Access: R/W **Description** This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. Both even and odd vertical totals are supported. This field is ignored by WD transcoders. Vertical total is double buffered. It updates immediately when transcoder is off. Otherwise, it updates at VBLANK rising edge. **Restriction** This register must always be programmed to the same value as the Vertical Blank End.
	15:13	**Reserved** Access: RO Format: MBZ
	12:0	**Vertical Active** Access: R/W This field specifies Vertical Active Display size. The first vertical active display line is considered line number# 0. This field is always programmed to the number of lines desired minus one. Restriction : When using the internal panel fitting logic, the minimum vertical active area must be seven lines. This register must always be programmed to the same value as the Vertical Blank Start.

TRANS_WD_FUNC_CTL

TRANS_WD_FUNC_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6E400h-6E403h
Name:	Transcoder WD0 Function Control
ShortName:	TRANS_WD_FUNC_CTL_0
Reset:	soft
Address:	6EC00h-6EC03h
Name:	Transcoder WD1 Function Control
ShortName:	TRANS_WD_FUNC_CTL_1
Reset:	soft

DWord	Bit	Description
0	31	**WD Function Enable** Access: R/W This bit enables the WD function. Value: 0b – Disable; 1b – Enable
	30	**Triggered Capture Mode Enable** Access: R/W This field enables the triggered capture mode where a frame is only captured after the Start Trigger Frame bit is written with 1, and hardware will ignore the transcoder frame time. This must be set before or when WD Function Enable is set. When triggered capture mode is disabled hardware will periodically capture frames following the transcoder frame time. Value: 0b – Disable; 1b – Enable
	29	**Start Trigger Frame** Access: R/W Set Write a 1 to this field to start a software triggered frame capture when Triggered Capture Mode Enable is 1. Hardware will clear the field when the frame starts.
	28	**Stop Trigger Frame** Access: R/W Set Write a 1 to this field to stop a software triggered frame capture when Triggered Capture Mode Enable is 1. Hardware will clear the field when the frame stops. This is only intended for use in case of an error where capture is never completing and software times out.

TRANS_WD_FUNC_CTL

It must not be set at the same time as Start Trigger Frame.

27 Reserved

Access:	R/W

26 Chroma Filtering Enable

Access:	R/W

This field selects how U and V are downsampled from YUV 444 to 422. This field only applies to the YUV 422 formats.

Value	Name	Description
0	Drop	Drop U2 and V2
1	Filter **[Default]**	Use a 15-34-15 three tap filter

25:23 Reserved

Access:	RO
Format:	MBZ

22:20 WD Color Mode

Access:	R/W

This field selects the capture color format.

Value	Name	Description
000b	YUV 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-Y:U:X:V)
001b	YUV 4:2:2	YUV 16-bit 4:2:2 packed (8:8:8:8 MSB- Y1:U:Y2:V) Chroma downsampling is programmable according to the Chroma Filtering field.
010b	XYUV 4:4:4	YUV 32-bit 4:4:4 packed (8:8:8:8 MSB-X:Y:U:V)
011b	RGBX	RGBX 32-bit (8:8:8:8 MSB-X:B:G:R)
100b	Y410	YUV 444 10bpc (MSB-X:V:Y:U)
101b	YUY2 8b	8 bit YUV 422 (MSB-V:Y2:U:Y1) Chroma downsampling is programmable according to the Chroma Filtering field.
110b	RGB10	RGB1010102 (MSB-X:B:G:R)

Restriction
This field must not be changed while the function is enabled.

19:18 Control Pointers

Access:	R/W

This field controls which pointers are sent and followed. If the head pointer is ignored, then the transcoder captures frames without any pointer comparison to stall the capture.

Value	Name	Description
00b	Enable Tail and Head	Send tail pointer to GT. Follow head pointer from GT.
01b	Enable Tail, Disable	Send tail pointer to GT. Ignore head pointer from GT. Non-

TRANS_WD_FUNC_CTL

	Head	cacheable.
11b	Disable Tail and Head	Do not send tail pointer to GT. Ignore head pointer from GT. Non-cacheable.

17:16 Reserved

15 Reserved

Access:	RO
Format:	MBZ

14:12 WD Input Select

Access:	R/W

These bits determine the input to WD.

Value	Name
000b	Pipe A
101b	Pipe B
110b	Pipe C
111b	Pipe D
Others	Reserved

Restriction
This field must not be changed while the function is enabled. It is not valid to have the same pipes driving multiple enabled transcoders.

11:4 Reserved

Access:	R/W

3:0 Frame Number

Access:	R/W

SW provided frame number. This is sent in the tail pointer message to media, to be used for synchronizing the encode with the display frame.

TRNULLDETCT

REG_TEMPLATE - TRNULLDETCT	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	04DE8h
Name:	TiledResources Null Tile Detection Register
ShortName:	TRNULLDETCT

DWord	Bit	Description
0	31:0	**Null Tile Detection Value** Access: R/W _Custom_GTIReset: DEV **Value** / **Name** / **Description** 00000000h / **[Default]** / A 32bit value programmed to enable h/w to perform a match of TR-VA TT entries to detect Null Tiles. Hardware will flag each entry and space behind it as Null Tile for matched entries.

TSEG Base Memory

TSEGMB - TSEG Base Memory

Register Space: MMIO: 0/2/0
Size (in bits): 64

Address: 108400h

This 64 bit register defines the TSEG Base.

DWord	Bit	Description
0..1	63:32	**TSEG Memory Base MSB** Access: R/W _Custom_GTIReset: BUS This register contains the base address of TSEG DRAM memory. Bios must program the value of TSEGMB to be the same as BGSM when TSEG is disabled. Value: FFFFFFFFh — Name: **[Default]**
	31:20	**TSEG Memory Base LSB** Access: R/W _Custom_GTIReset: BUS This register contains the base address of TSEG DRAM memory. Bios must program the value of TSEGMB to be the same as BGSM when TSEG is disabled. Value: FFFh — Name: **[Default]**
	19:0	**Reserved** Access: RO Format: MBZ

Ungated Clock Counter for DFR Testability

SAMPLER_DFR_UNGATED_COUNT - Ungated Clock Counter for DFR Testability

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV

Address: 0E148h

For testability of DFR feature

DWord	Bit	Description
0	31:0	**Counter Bits** Access: RO Format: U32 Count of full-speed sampler clocks

Unslice unit Level Clock Gating Control 943C

UNSLCGCTL943C - Unslice unit Level Clock Gating Control 943C

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0943Ch

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**hprunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hprunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**hucunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hucunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	28	**CSBE Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CSBE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**CSFE Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CSFE Clock Gating Disable Control:

UNSLCGCTL943C - Unslice unit Level Clock Gating Control 943C

	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
26	**CS Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
25	**mmcdunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS mmcdunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
24:5	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
4	**hedunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hedunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
3	**hlfunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

UNSLCGCTL943C - Unslice unit Level Clock Gating Control 943C

	2	**hmcunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hmcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**hmxunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hmxunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**hppunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hppunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9430

UNSLCGCTL9430 - Unslice unit Level Clock Gating Control 9430

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 09430h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:30	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	29	**oaal2 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS oaal2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	28	**oaal3 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS oaal3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	27	**mertgart Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS mertgart Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

UNSLCGCTL9430 - Unslice unit Level Clock Gating Control 9430

26	**RCPBLAT Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

RCPBLAT Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

25	**RCPBARB Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

RCPBARB Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

24	**LNIC Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

LNIC Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

23	**LNIB Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

LNIB Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

22:21	**Reserved**

Access:	R/W
_Custom_GTIReset:	BUS

Reserved

UNSLCGCTL9430 - Unslice unit Level Clock Gating Control 9430

20	**SARB Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SARB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
19	**DAP Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DAP Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
18	**RCC Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RCC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
17	**RAMRCC Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RAMRCC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
16	**OAC Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS OAC Clock Gating Disable Control '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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15	**SRCPBPIX Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SRCPBPIX Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

14	**SCFE Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SCFE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

13	**LNEP Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

LNEP Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

12	**LNGP Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

LNGP Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

11	**Reserved**

Access:	R/W
_Custom_GTIReset:	BUS

Reserved

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	10	**GCPunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**SPARE6 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**SPARE5 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**SPARE4 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**GPMunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS GPMunit Clock Gating Disable Control:

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		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	5	**MBGFunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS MBGFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**cg3ddismertg Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS cg3ddismertg Clock Gating Disable **Workaround** SW is required to disable clock gating to converge timing.
	3	**MSQDunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS MSQDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**MERTXG Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS MERTXG Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

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	1	**MISDunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS MISDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	0	**MCRunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS MCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

Unslice unit Level Clock Gating Control 9434

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Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09434h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**GTIunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS GTIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**MBCunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS MBCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	28	**GABunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS GABunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

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27	**DTunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS DTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
26	**cg3ddisvfg Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS cg3ddisvfg Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
25	**BLSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BLSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
24	**BLBunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
23	**BFunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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22 **BDunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

BDunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

21 **BCSunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

BCSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

20 **gamtlbhitarb Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbhitarb Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

19 **Reserved**

Access:	R/W
_Custom_GTIReset:	BUS

Reserved

18 **gamtlbmisarb Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbmisarb Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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17	**cg3ddiscfeg Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

cg3ddiscfeg Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

16	**POCS Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

POCS Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

15	**POCSFE Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

POCSFE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14	**POCSBE Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

POCSBE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

13:12	**Reserved**

Access:	R/W
_Custom_GTIReset:	BUS

Reserved

11	**gamedia Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

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		gamedia Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**gamid Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS gamid Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**gacs Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS gacs Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**cg3ddisbsc Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS cg3ddisbsc Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**cg3ddisvfgr Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS cg3ddisvfgr Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**SUCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SUCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for

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		functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**OACSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS OACSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	4	**NOAunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS NOAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**OARUNIT Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS OARUNIT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	1	**BCS BE Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BCS BE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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	0	**BCS FE Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BCS FE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9438

UNSLCGCTL9438 - Unslice unit Level Clock Gating Control 9438

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 09438h

Unit Level Clock Gating Disable bits.

DWord	Bit	Description
0	31	**maxf Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS MSQCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30:29	**MSQCunit Clock Gating Disable** Default Value: 11b Access: R/W _Custom_GTIReset: BUS MSQCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28:27	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	26	**LNEUNIT Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LNEUNIT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

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	25	**GAMXBL Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS GAMXLB Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**mgsx Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS mgsx Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**ccs3be Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccs3be Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**ccs2be Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccs2be Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**ccs1be Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccs1be Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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20	**ccs0be Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccs0be Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
19:9	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
8	**GUC Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GUC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
7	**ccs3fe Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccs3fe Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
6	**ccs2fe Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccs2fe Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
5	**ccs1fe Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccs1fe Clock Gating Disable Control:

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		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**ccs0fe Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccs0fe Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**ccsunit3 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccsunit3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**ccsunit2 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccsunit2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**ccsunit1 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccsunit1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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	0	**ccsunit0 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ccsunit0 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9440

UNSLCGCTL9440 - Unslice unit Level Clock Gating Control 9440

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09440h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	30	**RAM_RXBAR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RAM_RXBAR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**RXBAR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS RXBAR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**gamtlboacs Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlboacs Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**gamtlbvdbox5 Clock Gating Disable** Default Value: 1b Access: R/W

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	_Custom_GTIReset:	BUS

gamtlbvdbox5 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

26 **gamtlbvdbox6 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvdbox6 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

25 **gamdrtnunit Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamdrtnunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

24 **gamtlbvdbox3 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvdbox3 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

23 **gamtlbvdbox4 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvdbox4 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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22	**gamtlbvdbox7 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvdbox7 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : lock Gating Disabled. (i.e., clocks are toggling, always)

21	**gamtlbvdbox2 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvdbox2 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

20	**SPARE Clock Gating Disable2**

Access:	R/W
_Custom_GTIReset:	BUS

SPARE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**SPARE Clock Gating Disable1**

Access:	R/W
_Custom_GTIReset:	BUS

SPARE Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**Reserved**

Access:	R/W
_Custom_GTIReset:	BUS

Reserved

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17	**gamtlbvdbox0 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvdbox0 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**gamtlbkcr Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbkcr Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

15	**gamtlbguc Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbguc Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14	**gamtlbblt Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbblt Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

13	**gamtrtlb Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtrtlb Clock Gating Disable Control:

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	'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
12	**gamstlb Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamstlb Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
11	**gamccs Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamstlb Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
10:9	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
8	**gamctrl Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamctrl Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
7	**gamcmdi Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamcmdi Clock Gating Disable Control:

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		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**gamtlbvdbox1 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlbvdbox1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**gamwkrs Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamwkrs Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**gamdati Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamdati Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**L3_CR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS L3_CR Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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	2	**gamreqstrm Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamreqstrm Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**ramdft Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ramdft Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**hwmunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hwmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Unslice unit Level Clock Gating Control 9444

UNSLCGCTL9444 - Unslice unit Level Clock Gating Control 9444

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09444h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	30	**gamtlbgfxa0 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlbgfxa0 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	29	**gamtlbgfxa1 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlbgfxa1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

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28 **gamtlbcompa0 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbcompa0 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

27 **gamtlbcompa1 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbcompa1 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

26 **gamtlbcompb0 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbcompb0 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

25 **gamtlbcompb1 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbcompb1 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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	24	**gamtlbcompc0 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlbcompc0 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**gamtlbcompc1 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlbcompc1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**gamtlbcompd0 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlbcompd0 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**gamtlbcompd1 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlbcompd1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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20 **gamtlbmert Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbmert Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

19 **gamtlbvebox3 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvebox3 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18 **gamtlbvebox2 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvebox2 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17 **gamtlbvebox1 Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

gamtlbvebox1 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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	16	**gamtlbvebox0 Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS gamtlbvebox0 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	15	**LBCF Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LBCF Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**LBI Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LBI Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**LSQC Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LSQC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**LSQD Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LSQD Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

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	11	**LTCC Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LTCC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**LTCDD Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LTCDD Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	9	**LTCDT Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LTCDT Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	8	**SMCR Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	7	**Reserved**

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	6	**LDunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**LCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS LCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**CSCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS CSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	3	**KCRunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS KCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

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	2	**rcuunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS rcuunit Clock Gating Disable '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**lsnunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS lsnunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	0	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved

Unslice unit Level Clock Gating Control 9448

UNSLCGCTL9448 - Unslice unit Level Clock Gating Control 9448		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	09448h	
Unslice unit Level Clock Gating Control 9448 Unit Level Clock Gating Disable bits		
DWord	**Bit**	**Description**
0	31:0	**ECO Spare Bits** Access: R/W _Custom_GTIReset: BUS Reserved

Unslice unit Level Clock Gating Control 9450

UNSLCGCTL9450 - Unslice unit Level Clock Gating Control 9450

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 09450h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:23	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	22	**BLBunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BLBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**BFunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS BFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20:11	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	10	**GUC Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GUC Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.

UNSLCGCTL9450 - Unslice unit Level Clock Gating Control 9450

	9:5	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	4	**vhmeunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3:0	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved

Unslice unit Level Clock Gating Control 9454

UNSLCGCTL9454 - Unslice unit Level Clock Gating Control 9454

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	09454h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:22	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved
	21	**SPARE Clock Gating Disable2** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20:0	**Reserved** Access: R/W _Custom_GTIReset: BUS Reserved

uOS Full Hash

UOS_FULL_HASH - uOS Full Hash

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	512

The Full Hash being generated for the uOS. This register is written by Shim hardware. The update happens as the Full Hash is being generated and compared during the GfxMem --> WOPCM DMA operation. IA Writes have no effect.

Programming Notes
This register is saved in the power context
Bits [383:0] of the "Hash" field contains valid values, bits[511:384] are reserved for future expansion.

DWord	Bit	Description
0..15	511:0	**Hash** Access: RO

UTIL_PIN_BUF_CTL

UTIL_PIN_BUF_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	48404h-48407h
Name:	Utility Pin Buffer Control
ShortName:	UTIL_PIN_BUF_CTL
Reset:	soft

This register controls the display utility pin I/O buffer.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:28	**Hysteresis** Access: R/W
	27	**Reserved** Access: RO Format: MBZ
	26:24	**Spare** Access: R/W
	23:21	**Reserved** Access: RO Format: MBZ
	20:16	**Pulldown Strength** Access: R/W
	15:12	**Pulldown Slew** Access: R/W
	11:9	**Reserved** Access: RO Format: MBZ
	8:4	**Pullup Strength** Access: R/W
	3:0	**Pullup Slew** Access: R/W

UTIL_PIN_CTL

UTIL_PIN_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	48400h-48403h
Name:	Utility Pin Control
ShortName:	UTIL_PIN_CTL
Reset:	soft

This register controls the display utility pin. The maximum switching frequency is 100 KHz.

DWord	Bit	Description
0	31	**Util Pin Enable** Access: R/W This bit enables the utility pin. Value / Name: 0b – Disable 1b – Enable
	30:29	**Pipe Select** Access: R/W This bit selects which pipe will be used when the utility pin is outputting timing related signals. Value / Name: 00b – Pipe A 01b – Pipe B 10b – Pipe C 11b – Pipe D Restriction: The field should only be changed when the utility pin is disabled or not configured to use any timing signals.
	28	**Reserved** Access: RO Format: MBZ

UTIL_PIN_CTL

27:24 Util Pin Mode

Access:	R/W

This bit configures the utility pin mode of operation for output.

Value	Name	Description
0000b	Data	Output the Util_Pin_Output_Data value.
0001b	PWM	Output from the backlight PWM circuit.
0100b	Vblank	Output the vertical blank. [] This is the pipe delayed vblank.
0101b	Vsync	Output the vertical sync.
0110b	framestart	Output the framestart
Others	Reserved	Reserved

Restriction
The field should only be changed when the utility pin is disabled.

23 Util Pin Output Data

Access:	R/W

This bit selects what the value to drive as an output when in the data mode.

Value	Name
0b	0
1b	1

22 Util Pin Output Polarity

Access:	R/W

This bit inverts the polarity of the pin output.

Value	Name
0b	Not inverted
1b	Inverted

21:20 Reserved

Access:	RO
Format:	MBZ

19 Util Pin Direction

Access:	R/W

This bit selects whether the pin is used as an output or an input.

Value	Name
0b	Output
1b	Input

Restriction
The field should only be changed when the utility pin is disabled.

UTIL_PIN_CTL		
	18:17	**Reserved** Access: RO Format: MBZ
	16	**Util Pin Input Data** Access: RO This bit gives the value received on the pin. This is only valid when the utility pin is enabled and the direction is input.
	15:0	**Reserved** Access: RO Format: MBZ

UTIL2_PIN_BUF_CTL

UTIL2_PIN_BUF_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	4840Ch-4840Fh
Name:	Utility2 Pin Buffer Control
ShortName:	UTIL2_PIN_BUF_CTL
Reset:	soft

This register controls the display utility2 pin I/O buffer.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:28	**Hysteresis** Access: R/W
	27	**Reserved** Access: RO Format: MBZ
	26:24	**Spare** Access: R/W
	23:21	**Reserved** Access: RO Format: MBZ
	20:16	**Pulldown Strength** Access: R/W
	15:12	**Pulldown Slew** Access: R/W
	11:9	**Reserved** Access: RO Format: MBZ
	8:4	**Pullup Strength** Access: R/W
	3:0	**Pullup Slew** Access: R/W

UTIL2_PIN_CTL

UTIL2_PIN_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	48408h-4840Bh
Name:	Utility2 Pin Control
ShortName:	UTIL2_PIN_CTL
Reset:	soft

This register controls the display utility2 pin.

DWord	Bit	Description
0	31	**Util Pin Enable** Access: R/W This bit enables the utility pin. 0b: Disable 1b: Enable
	30	**Util Pin Direction** Access: R/W This bit selects whether the pin is used as an output or an input. 0b: Output 1b: Input Restriction: The field should only be changed when the utility pin is disabled.
	29:0	**Reserved** Access: RO Format: MBZ

Valid Bit Vector 3 for RCC Register

RCCTLB_VLD_3 - Valid Bit Vector 3 for RCC Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
Address:	04DACh	
This register contains the valid bits for entries 0-31 of RCCTLB.		
DWord	**Bit**	**Description**
0	31:0	**Valid Bit Vector 3 for RCC** Default Value: 00000000h Access: RO _Custom_GTIReset: DEV Valid Bits per Entry.

VCS CSB

VCS_CSB - VCS CSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SW reads this offset to read the CSB entry at the top of the CSB fifo. Reads must occur in pairs to obtain a single 64 bit CSB entry. The second read pops the entry off the CSB fifo.		
DWord	**Bit**	**Description**
0	31:0	**Context Status Buffer DW** Access: RO This DW holds CSB bits[31:0] for the first read and CSB bits[63:32] for the second read.

VCS CSB Fifo Status Register

VCS_CSB_FSR - VCS CSB Fifo Status Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
This RO register holds status of the CSB fifo.		
DWord	**Bit**	**Description**
0	31	**Not Empty** Default Value: 0000000000000000b Access: RO
	30:16	**Reserved** Access: RO Format: MBZ
	15:8	**FIFO Maximum Occupancy Count** This field is a read-only field. It reflects the depth of the FIFO, which is a static value for each product.
	7:0	**Fifo Occupancy Count** Access: RO

VDBox TLB Invalidation Register

VD_TLB_INV_CR - VDBox TLB Invalidation Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0CEDCh

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000000000000000b Access: R/W
	15:8	**Reserved** Access: RO Format: MBZ
	7	**Invalidate VDBox TLBs bit7** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.
	6	**Invalidate VDBox TLBs bit6** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.
	5	**Invalidate VDBox TLBs bit5** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0]

VD_TLB_INV_CR - VDBox TLB Invalidation Register

		TLBs. No Effect on non-existent VDBoxs. These bits self clear.
	4	**Invalidate VDBox TLBs bit4** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.
	3	**Invalidate VDBox TLBs bit3** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.
	2	**Invalidate VDBox TLBs bit2** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.
	1	**Invalidate VDBox TLBs bit1** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.

VD_TLB_INV_CR - VDBox TLB Invalidation Register

	0	**Invalidate VDBox TLBs bit0** Default Value: 0b Access: R/W SW writes 1 to invalidate the TLBs for the associated VDBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[7:0] invalidates VDBox[7:0] TLBs. No Effect on non-existent VDBoxs. These bits self clear.

Vdbox unit Level Clock Gating Control 3F0C

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1C3F0Ch-1C3F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX0
Address:	1C7F0Ch-1C7F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX1
Address:	1D3F0Ch-1D3F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX2
Address:	1D7F0Ch-1D7F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX3
Address:	1E3F0Ch-1E3F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX4
Address:	1E7F0Ch-1E7F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX5
Address:	1F3F0Ch-1F3F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX6
Address:	1F7F0Ch-1F7F0Fh
Name:	VDbox registers4
ShortName:	VDCGCTL3F0C_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**SPARE Clock Gating Disable12** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	30	**SPARE Clock Gating Disable11** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**SPARE Clock Gating Disable10** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**SPARE Clock Gating Disable9** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**VNCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VNCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**VMXunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

	25	**VMTSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMTSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**VMPCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**VMDunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**VMCRunit Clock Gating Disable** Default Value: 1b Access: R/W _Custom_GTIReset: BUS VMCRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	21	**VMCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

20	**VMBunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VMBunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**VLFunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VLFunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**VITunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VITunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**VISunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VISunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**VIPunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VIPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

15	**VID6 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VID6 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
14	**VID5 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VID5 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
13	**VID4 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VID4 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
12	**VID3 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VID3 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
11	**VID2 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VID2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

	10	**VID1 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VID1 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	9	**VIMEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VIMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**VHRunit's Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VHRunit's Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	7	**VHMEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VHMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**VFTunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

5	**VDXunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VDXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
4	**VDSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
3	**vdl1unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS vdl1unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
2	**Csunit's Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS Csunit's Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
1	**VCREunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VCREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F0C - Vdbox unit Level Clock Gating Control 3F0C

	0	**VCPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F04

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1C3F04h-1C3F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX0
Address:	1C7F04h-1C7F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX1
Address:	1D3F04h-1D3F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX2
Address:	1D7F04h-1D7F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX3
Address:	1E3F04h-1E3F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX4
Address:	1E7F04h-1E7F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX5
Address:	1F3F04h-1F3F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX6
Address:	1F7F04h-1F7F07h
Name:	VDbox registers2
ShortName:	VDCGCTL3F04_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**spare Clock Gating Disable4** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
30	**spare Clock Gating Disable3** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
29	**spare Clock Gating Disable2** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
28	**HVSHAREunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HVSHAREunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
27	**HFTunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HFTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
26	**HFQunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HFQunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

	25	**HCRESunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HCRESunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**HCREIunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HCREIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**HCREFunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HCREFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**MEDunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MEDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**GACXunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GACXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

20	**GACunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

GACunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**ECPunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

ECPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**BSPunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

BSPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**vmmunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

vmmunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**VHLFunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VHLFunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

15 **VDKMXunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VDKMXunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

14 **HWMunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HWMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

13 **HUCMXunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HUCMXunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12 **HUCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HUCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

11 **HSSEunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HSSEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

10	**HSFunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HSFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
9	**HPRunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HPRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
8	**HPPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HPPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
7	**HMXFunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HMXFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
6	**HMXBunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HMXBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

5	**HMCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HMCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

4	**HITunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HITunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

3	**HHLFunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HHLFunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

2	**HFCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HFCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

1	**HEDunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HEDunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F04 - Vdbox unit Level Clock Gating Control 3F04

	0	**HBEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HBEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F08

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1C3F08h-1C3F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX0
Address:	1C7F08h-1C7F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX1
Address:	1D3F08h-1D3F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX2
Address:	1D7F08h-1D7F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX3
Address:	1E3F08h-1E3F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX4
Address:	1E7F08h-1E7F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX5
Address:	1F3F08h-1F3F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX6
Address:	1F7F08h-1F7F0Bh
Name:	VDbox registers3
ShortName:	VDCGCTL3F08_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**SPARE Clock Gating Disable8** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

	30	**SPARE Clock Gating Disable7** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	29	**SPARE Clock Gating Disable6** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	28	**spare Clock Gating Disable5** Access: R/W _Custom_GTIReset: BUS SPARE Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	27	**VClunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VClunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	26	**VCDunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

	25	**vbspunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS vbspunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**VBPunits Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VBPunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	23	**VAMunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VAMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**VADuit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VADuit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**VACunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VACunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

20	**USBunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

USBunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19	**SECunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SECunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18	**RDOFunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

RDOFunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17	**RDOBunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

RDOBunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16	**QRCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

QRCunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

	15	**MEDunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MEDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	14	**MPCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	13	**MDCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS MDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	12	**jusbunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS jusbunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	11	**JPGunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS JPGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

10	**HWOPunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HWOPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

9	**HVDL1unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HVDL1unit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

8	**HVDunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HVDunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

7	**HTQunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HTQunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

6	**HSAOunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HSAOunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

	5	**HRSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HRSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**HPOunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HPOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**HMDCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HMDCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**HLEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HLEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**HLCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HLCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F08 - Vdbox unit Level Clock Gating Control 3F08

	0	**HIMEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HIMEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F10

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

Register Space:	MMIO: 0/2/0
Size (in bits):	32

Address:	1C3F10h-1C3F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX0

Address:	1C7F10h-1C7F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX1

Address:	1D3F10h-1D3F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX2

Address:	1D7F10h-1D7F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX3

Address:	1E3F10h-1E3F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX4

Address:	1E7F10h-1E7F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX5

Address:	1F3F10h-1F3F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX6

Address:	1F7F10h-1F7F13h
Name:	VDbox registers5
ShortName:	VDCGCTL3F10_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:11	**Reserved** Access: RO Format: MBZ

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

10	**hmxbrouterunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

hmxbrouterunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

9	**RAMDFTunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

RAMDFTunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

8	**VWOPunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VWOPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

7	**SWPunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SWPunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

6	**VTQunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VTQunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

	5	**VSLunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VSLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**VSECunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VSECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**VRTunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VRTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**VPRunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VPRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**VOPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VOPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F10 - Vdbox unit Level Clock Gating Control 3F10

	0	**VNEunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VNEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F14

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

Register Space:	MMIO: 0/2/0
Size (in bits):	32

Address:	1C3F14h-1C3F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX0

Address:	1C7F14h-1C7F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX1

Address:	1D3F14h-1D3F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX2

Address:	1D7F14h-1D7F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX3

Address:	1E3F14h-1E3F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX4

Address:	1E7F14h-1E7F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX5

Address:	1F3F14h-1F3F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX6

Address:	1F7F14h-1F7F17h
Name:	VDbox registers6
ShortName:	VDCGCTL3F14_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31	**VDIunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

	'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
30	**SFMunit Clock Gating Disable1** Access: R/W _Custom_GTIReset: BUS SFMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
29	**SFEunit Clock Gating Disable1** Access: R/W _Custom_GTIReset: BUS SFEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
28	**SFDunits Clock Gating Disable1** Access: R/W _Custom_GTIReset: BUS SFDunits Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
27	**SFAunit Clock Gating Disable1** Access: R/W _Custom_GTIReset: BUS SFAunit Clock Gating Disable Control:

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	26	**VEOunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VEOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	25	**VNCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VNCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	24	**VMXunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMXunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

	23	**vmpcunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS vmpcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**vmmunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS vmmunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**VMCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VMCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	20	**VLFunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

	19	**VISunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VISunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	18	**vhmeunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS vhmeunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	17	**vhlfunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS vhlfunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	16	**VCWunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VCWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

15 **HWMCMD Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HWMCMD Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

14 **USBunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

USBunit Clock Gating Disable Control:

'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

13 **QRCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

QRCunit Clock Gating Disable Control:

'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

12 **MPCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

MPCunit Clock Gating Disable Control:

'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

	11	**mdcunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS mdcunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	10	**HWMunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HWMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always) **Workaround** SW is required to disable clock gating to converge timing.
	9	**IECPuit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS IECPuit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	8	**HVDunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HVDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

7	**HUCMXunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HUCMXunit Clock Gating Disable Control:

'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

6	**HUCunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HUCunit Clock Gating Disable Control:

'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

5	**HTQunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HTQunit Clock Gating Disable Control:

'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

4	**HSAOunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

HSAOunit Clock Gating Disable Control:

'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

VDCGCTL3F14 - Vdbox unit Level Clock Gating Control 3F14

	3	**HPRunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HPRunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**HPPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HPPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**HHLFunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HHLFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**HFCunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS HFCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating Control 3F18

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1C3F18h-1C3F1Bh
Name:	VDbox registers7
ShortName:	VDCGCTL3F18_VDBOX0
Address:	1C7F18h-1C7F1Bh
Name:	VDbox registers7
ShortName:	VDCGCTL3F18_VDBOX1
Address:	1D3F18h-1D3F1Bh
Name:	VDbox registers7
ShortName:	VDCGCTL3F18_VDBOX2
Address:	1D7F18h-1D7F1Bh
Name:	VDbox registers7
ShortName:	VDCGCTL3F18_VDBOX3
Address:	1E3F18h-1E3F1Bh
Name:	VDbox registers7
ShortName:	VDCGCTL3F18_VDBOX4
Address:	1E7F18h-1E7F1Bh
Name:	VDbox registers7
ShortName:	VDCGCTL3F18_VDBOX5
Address:	1F3F18h-1F3F1Bh
Name:	VDbox registers7
ShortName:	VDCGCTL3F18_VDBOX6
Address:	1F7F18h-1F7F1Bh
Name:	VDbox registers7
ShortName:	VDCGCTL3F18_VDBOX7

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

26	**VECS BE unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VECS BE unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
25	**VECS FE unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VECS FE unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
24	**VCS BE unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VCS BE unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
23	**VCS FE unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VCS FE unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

22	**amx router unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS amxb router unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
21	**amx unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS amx unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
20	**splt unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS splt unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
19	**tbc unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS tbc unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

18	**vdl1is unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

vdl1is unit Clock Gating Disable Control:

'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

17	**lbc unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

lbc unit Clock Gating Disable Control:

'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

16	**amxb unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

amxb unit Clock Gating Disable Control:

'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

15	**Reserved**

Access:	RO
Format:	MBZ

14	**awm unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

awm unit Clock Gating Disable Control:

'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

13	**aln unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

aln unit Clock Gating Disable Control:

'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

Workaround
SW is required to disable clock gating to converge timing.

12	**alf unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

alf unit Clock Gating Disable Control:

'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

11	**apr unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

apr unit Clock Gating Disable Control:

'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

10	**amc unit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

amc unit Clock Gating Disable Control:

'0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality)

'1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

9	**ait unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ait unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
8	**app unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS app unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
7	**aed unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS aed unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
6	**hfe unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS hfe unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

	5	**scr unit Clock Gating Disable 2** Access: R/W _Custom_GTIReset: BUS scr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	4	**scr unit Clock Gating Disable 1** Access: R/W _Custom_GTIReset: BUS scr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	3	**scr unit Clock Gating Disable 0** Access: R/W _Custom_GTIReset: BUS scr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)
	2	**scr unit Clock Gating Disable 3** Access: R/W _Custom_GTIReset: BUS scr unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

VDCGCTL3F18 - Vdbox unit Level Clock Gating Control 3F18

	1	**Reserved** Access: RO Format: MBZ
	0	**kin unit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS kin unit Clock Gating Disable Control: '0' : Clock Gating Enabled.; (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled.; (i.e., clocks are toggling, always)

Vdbox unit Level Clock Gating override during rstflow

VDMISCCP3F20 - Vdbox unit Level Clock Gating override during rstflow

Register Space: MMIO: 0/2/0
Size (in bits): 32

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:0	**ECO Spare Bits** Access: R/W _Custom_GTIReset: BUS Reserved

vdcp Vdbox unit Level Clock Gating override during rstflow

VDMISCCP3F20 - vdcp Vdbox unit Level Clock Gating override during rstflow

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	03F20h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**misccp Clock Gating Disable during rstflow** Default Value: 1b Access: R/W _Custom_GTIReset: BUS misccp Clock Gating Disable Control: '0' : Clock Gating Enabled during reset flows (i.e., clocks can be gated when they are not required to toggle for functionality, NOT Recommended) '1' : Clock Gating Disabled during reset flows. (i.e., clocks are toggling, always) Register bit defaults to value 1'b1, which is a requirement due to Synchronous reset flops Randomizing this bit will result in X flush not completing during the simulation

VDMBDFBARKVM

VDMBDFBARKVM - VDMBDFBARKVM

Register Space:	MMIO: 0/2/0
Size (in bits):	32
SOC_Consumer:	BIOS
Address:	134140h

Allows indirection of KVM traffic for manageability.

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18:16	**BARNUM** Default Value: 111b Access: R/W _Custom_GTIReset: BUS Indicates to which base address register VDM packets should be addressed.
	15:8	**BUSNUM** Default Value: 00000000b Access: R/W _Custom_GTIReset: BUS Indicates to which bus number VDM packets should be addressed.
	7:3	**DEVNUM** Default Value: 10110b Access: R/W _Custom_GTIReset: BUS Indicates to which Device number VDM packets should be addressed.
	2:0	**FUNNUM** Default Value: 000b Access: R/W _Custom_GTIReset: BUS Indicates to which Function number VDM packets should be addressed.

VEBOX TLB Invalidation Register

VE_TLB_INV_CR - VEBOX TLB Invalidation Register

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0CEE0h

DWord	Bit	Description
0	31:16	**Mask Bits** Default Value: 0000000000000000b Access: R/W _Custom_GTIReset: DEV
	15:4	**Reserved** Access: RO Format: MBZ
	3	**Invalidate VEBox TLBs bit3** Default Value: 0b Access: R/W _Custom_GTIReset: DEV SW writes 1 to invalidate the TLBs for the associated VEBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[3:0] invalidates VEBox[3:0] TLBs. No Effect on non-existent VEBoxs. These bits self clear.
	2	**Invalidate VEBox TLBs bit2** Default Value: 0b Access: R/W _Custom_GTIReset: DEV SW writes 1 to invalidate the TLBs for the associated VEBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[3:0] invalidates VEBox[3:0] TLBs. No Effect on non-existent VEBoxs. These bits self clear.
	1	**Invalidate VEBox TLBs bit1** Default Value: 0b Access: R/W _Custom_GTIReset: DEV

VE_TLB_INV_CR - VEBOX TLB Invalidation Register

		SW writes 1 to invalidate the TLBs for the associated VEBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[3:0] invalidates VEBox[3:0] TLBs. No Effect on non-existent VEBoxs. These bits self clear.
	0	**Invalidate VEBox TLBs bit0** Default Value: 0b Access: R/W _Custom_GTIReset: DEV SW writes 1 to invalidate the TLBs for the associated VEBox and HW clears the bit when invalidation is complete. To ensure proper invalidation of the TLBs, SW has to ensure the corresponding engine's HW pipeline is flushed and cleared from all its memory accesses. Otherwise HW cannot guarantee the proper invalidation for TLBs.Bit[3:0] invalidates VEBox[3:0] TLBs. No Effect on non-existent VEBoxs. These bits self clear.

Vebox unit Level Clock Gating Control 3F04

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1CBF04h-1CBF07h
Name:	VEbox registers
ShortName:	VECGCTL3F04_VEBOX0
Address:	1DBF04h-1DBF07h
Name:	VEbox registers
ShortName:	VECGCTL3F04_VEBOX1
Address:	1EBF04h-1EBF07h
Name:	VEbox registers
ShortName:	VECGCTL3F04_VEBOX2
Address:	1FBF04h-1FBF07h
Name:	VEbox registers
ShortName:	VECGCTL3F04_VEBOX3

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23	**ramdftunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS ramdftunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	22	**cg3ddis_spare2 Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS cg3ddis_spare2 Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	21	**cg3ddis_spare1 Clock Gating Disable**

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

	Access:	R/W
	_Custom_GTIReset:	BUS

cg3ddis_spare1 Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

20 **MCRunit Clock Gating Disable**

Default Value:	1b
Access:	R/W
_Custom_GTIReset:	BUS

MCRunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

19 **VFWunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VFWunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

18 **VEOunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

VEOunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

17 **ECSunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

ECSunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

16 **VDNunit Clock Gating Disable**

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

	Access: R/W _Custom_GTIReset: BUS VDNunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
15	**VDMunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VDMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
14	**VDIunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
13	**VCWunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VCWunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
12	**VCUSunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VCUSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
11	**SFXunit Clock Gating Disable** Access: R/W

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

	_Custom_GTIReset:	BUS

SFXunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

10 **SFOunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFOunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

9 **SFMunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

8 **SFIunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFIunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

7 **SFEunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

6 **SFDunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFDunit Clock Gating Disable Control:

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

		'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**SFAunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS SFAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	4	**NOAunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS NOAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	3	**IECPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS IECPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	2	**GCPunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	1	**GAVARBunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GAVARBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)

VECGCTL3F04 - Vebox unit Level Clock Gating Control 3F04

		'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	0	**GAVunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS GAVunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

Vebox unit Level Clock Gating Control 3F08

VECGCTL3F08 - Vebox unit Level Clock Gating Control 3F08

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1CBF08h-1CBF0Bh
Name:	VEbox registers
ShortName:	VECGCTL3F08_VEBOX0
Address:	1DBF08h-1DBF0Bh
Name:	VEbox registers
ShortName:	VECGCTL3F08_VEBOX1
Address:	1EBF08h-1EBF0Bh
Name:	VEbox registers
ShortName:	VECGCTL3F08_VEBOX2
Address:	1FBF08h-1FBF0Bh
Name:	VEbox registers
ShortName:	VECGCTL3F08_VEBOX3

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7	**VEOunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VEOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	6	**VDIunit Clock Gating Disable** Access: R/W _Custom_GTIReset: BUS VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)
	5	**VCWunit Clock Gating Disable**

VECGCTL3F08 - Vebox unit Level Clock Gating Control 3F08

	Access:	R/W
	_Custom_GTIReset:	BUS

VCWunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

4 **SFMunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFMunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

3 **SFEunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFEunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

2 **SFDunits Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFDunits Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

1 **SFAunit Clock Gating Disable**

Access:	R/W
_Custom_GTIReset:	BUS

SFAunit Clock Gating Disable Control:
'0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality)
'1' : Clock Gating Disabled. (i.e., clocks are toggling, always)

0 **IECPuit Clock Gating Disable**

Access:	R/W

VECGCTL3F08 - Vebox unit Level Clock Gating Control 3F08

		_Custom_GTIReset:	BUS
		IECPuit Clock Gating Disable Control: '0' : Clock Gating Enabled. (i.e., clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (i.e., clocks are toggling, always)	

Vebox unit Level Clock Gating override during rstflow

VEMISCCP3F10 - Vebox unit Level Clock Gating override during rstflow

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	03F10h

Unit Level Clock Gating Disable bits

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**misccp Clock Gating Disable during rstflow** Default Value: 1b Access: R/W _Custom_GTIReset: BUS misccp Clock Gating Disable Control: '0' : Clock Gating Enabled during reset flows (i.e., clocks can be gated when they are not required to toggle for functionality, NOT Recommended) '1' : Clock Gating Disabled during reset flows. (i.e., clocks are toggling, always) Randomizing this bit will result in X flush not completing during the simulation

VECS CSB

VECS_CSB - VECS CSB		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
SW reads this offset to read the CSB entry at the top of the CSB fifo. Reads must occur in pairs to obtain a single 64 bit entry. The second read pops the entry off the CSB fifo.		
DWord	**Bit**	**Description**
0	31:0	**Context Status Buffer DW** Access: RO This DW holds CSB bits[31:0] for the first read and CSB bits[63:32] for the second read.

VECS CSB Fifo Status Register

VECS_CSB_FSR - VECS CSB Fifo Status Register		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
This RO register holds status of the CSB fifo		
DWord	**Bit**	**Description**
0	31	**Not Empty** Access: RO
	30:16	**Reserved** Access: RO Format: MBZ
	15:8	**Fifo Maximum Occupancy Count** This field is a read-only field. It reflects the depth of the FIFO, which is a static value for each product.
	7:0	**FIFO Occupancy Count** Access: RO

Vendor Identification

VID2_0_2_0_PCI - Vendor Identification		
Register Space: PCI: 0/2/0 Size (in bits): 16		
Address: 00000h		
This register combined with the Device Identification register uniquely identifies any PCI device.		
DWord	**Bit**	**Description**
0	15:0	**Vendor Identification Number** Default Value: 1000000010000110b Access: RO _Custom_GTIReset: BUS PCI standard identification for Intel.

VEO Current Pipe 0 XY Register

VEO_CURRENT0_XY - VEO Current Pipe 0 XY Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1CA054h
ShortName:	VEO_CURRENT0_XY_01
Address:	1DA054h
ShortName:	VEO_CURRENT0_XY_02
Address:	1EA054h
ShortName:	VEO_CURRENT0_XY_03
Address:	1FA054h
ShortName:	VEO_CURRENT0_XY_04

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**Current Input Pipe 0 X** Default Value: 0h Access: RO
	15	**Reserved** Access: RO Format: MBZ
	14:0	**Current Input Pipe 0 Y** Default Value: 0h Access: RO

VEO DN Pipe 0 XY Register

VEO_DN0_XY - VEO DN Pipe 0 XY Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1CA04Ch
ShortName:	VEO_DN0_XY_01
Address:	1DA04Ch
ShortName:	VEO_DN0_XY_02
Address:	1EA04Ch
ShortName:	VEO_DN0_XY_03
Address:	1FA04Ch
ShortName:	VEO_DN0_XY_04

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**DN Pipe 0 X** Default Value: 0h Access: RO dn_input_x[13:0]
	15	**Reserved** Access: RO Format: MBZ
	14:0	**DN Pipe 0 Y** Default Value: 0h Access: RO dn_input_y[14:0]

VEO DN Pipe 1 XY Register

VEO_DN1_XY - VEO DN Pipe 1 XY Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1CA050h
ShortName:	VEO_DN1_XY_01
Address:	1DA050h
ShortName:	VEO_DN1_XY_02
Address:	1EA050h
ShortName:	VEO_DN1_XY_03
Address:	1FA050h
ShortName:	VEO_DN1_XY_04

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**DN Pipe 1 X** Default Value: 0h Access: RO
	15	**Reserved** Access: RO Format: MBZ
	14:0	**DN Pipe 1 Y** Default Value: 0h Access: RO

VEO DV Count Register

VEO_DV_COUNT - VEO DV Count Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1CA044h
ShortName:	VEO_DV_COUNT_01
Address:	1DA044h
ShortName:	VEO_DV_COUNT_02
Address:	1EA044h
ShortName:	VEO_DV_COUNT_03
Address:	1FA044h
ShortName:	VEO_DV_COUNT_04

DWord	Bit	Description
0	31:24	**Pipe1 Motion History DV/Hold Maxcount** Default Value: 0h Access: RO
	23:16	**Pipe1 Pixel History DV/Hold Maxcount** Default Value: 0h Access: RO
	15:8	**Pipe0 Motion History DV/Hold Maxcount** Default Value: 0h Access: RO
	7:0	**Pipe0 Pixel History DV/Hold Maxcount** Default Value: 0h Access: RO

VEO DV Hold Register

VEO_DVHOLD - VEO DV Hold Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1CA05Ch
ShortName:	VEO_DVHOLD_01
Address:	1DA05Ch
ShortName:	VEO_DVHOLD_02
Address:	1EA05Ch
ShortName:	VEO_DVHOLD_03
Address:	1FA05Ch
ShortName:	VEO_DVHOLD_04

Datavalid/Hold signals for VEO interface

DWord	Bit	Description	
0	31	**vdn_p0_veo_pixel_dv**	
		Default Value:	0h
		Access:	RO
	30	**veo_vdn_p0_pixel_hold**	
		Default Value:	0h
		Access:	RO
	29	**vdn_p0_veo_mh_dv**	
		Default Value:	0h
		Access:	RO
	28	**veo_vdn_p0_mh_hold**	
		Default Value:	0h
		Access:	RO
	27	**vdn_p0_veo_bne_luma_dv**	
		Default Value:	0h
		Access:	RO
	26	**veo_vdn_p0_bne_luma_hold**	
		Default Value:	0h
		Access:	RO
	25	**vdn_p0_veo_bne_chroma_dv**	
		Default Value:	0h

VEO_DVHOLD - VEO DV Hold Register

	Access:	RO
24	**veo_vdn_p0_bne_chroma_hold**	
	Default Value:	0h
	Access:	RO
23	**vdi_p0_veo_pixel_dv**	
	Default Value:	0h
	Access:	RO
22	**veo_vdi_p0_pixel_hold**	
	Default Value:	0h
	Access:	RO
21	**vdi_p0_veo_stmm_dv**	
	Default Value:	0h
	Access:	RO
20	**veo_vdi_p0_stmm_hold**	
	Default Value:	0h
	Access:	RO
19	**vdi_p0_veo_fmd_dv**	
	Default Value:	0h
	Access:	RO
18	**veo_vdi_p0_fmd_hold**	
	Default Value:	0h
	Access:	RO
17	**iecp_p0_veo_dv**	
	Default Value:	0h
	Access:	RO
16	**veo_iecp_p0_hold**	
	Default Value:	0h
	Access:	RO
15	**vdn_p1_veo_pixel_dv**	
	Default Value:	0h
	Access:	RO
14	**veo_vdn_p1_pixel_hold**	
	Default Value:	0h
	Access:	RO
13	**vdn_p1_veo_mh_dv**	
	Default Value:	0h

VEO_DVHOLD - VEO DV Hold Register

	Access:	RO
12	**veo_vdn_p1_mh_hold**	
	Default Value:	0h
	Access:	RO
11	**vdn_p1_veo_bne_luma_dv**	
	Default Value:	0h
	Access:	RO
10	**veo_vdn_p1_bne_luma_hold**	
	Default Value:	0h
	Access:	RO
9	**vdn_p1_veo_bne_chroma_dv**	
	Default Value:	0h
	Access:	RO
8	**veo_vdn_p1_bne_chroma_hold**	
	Default Value:	0h
	Access:	RO
7	**vdi_p1_veo_pixel_dv**	
	Default Value:	0h
	Access:	RO
6	**veo_vdi_p1_pixel_hold**	
	Default Value:	0h
	Access:	RO
5	**vdi_p1_veo_stmm_dv**	
	Default Value:	0h
	Access:	RO
4	**veo_vdi_p1_stmm_hold**	
	Default Value:	0h
	Access:	RO
3	**vdi_p1_veo_fmd_dv**	
	Default Value:	0h
	Access:	RO
2	**veo_vdi_p1_fmd_hold**	
	Default Value:	0h
	Access:	RO
1	**iecp_p1_veo_dv**	
	Default Value:	0h

VEO_DVHOLD - VEO DV Hold Register			
		Access:	RO
	0	**veo_iecp_p1_hold**	
		Default Value:	0h
		Access:	RO

VEO Previous Pipe 0 XY Register

VEO_PREVIOUS0_XY - VEO Previous Pipe 0 XY Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1CA058h
ShortName:	VEO_PREVIOUS0_XY_01
Address:	1DA058h
ShortName:	VEO_PREVIOUS0_XY_02
Address:	1EA058h
ShortName:	VEO_PREVIOUS0_XY_03
Address:	1FA058h
ShortName:	VEO_PREVIOUS0_XY_04

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29:16	**Previous Input Pipe 0 X** Default Value: 0h Access: RO
	15	**Reserved** Access: RO Format: MBZ
	14:0	**Previous Input Pipe 0 Y** Default Value: 0h Access: RO

VEO State Register

VEO_STATE - VEO State Register			
Register Space:	MMIO: 0/2/0		
Access:	RO		
Size (in bits):	32		
Address:	1CA040h		
ShortName:	VEO_STATE_01		
Address:	1DA040h		
ShortName:	VEO_STATE_02		
Address:	1EA040h		
ShortName:	VEO_STATE_03		
Address:	1FA040h		
ShortName:	VEO_STATE_04		
Data valids and holds for the statistics interface			
DWord	**Bit**	**Description**	
0	31	**iecp_p0_veo_his_dv**	
		Default Value:	0h
		Access:	RO
	30	**iecp_p0_veo_skin_dv**	
		Default Value:	0h
		Access:	RO
	29	**iecp_p0_veo_rgb_his_dv**	
		Default Value:	0h
		Access:	RO
	28	**iecp_p0_veo_out_dist_dv**	
		Default Value:	0h
		Access:	RO
	27	**iecp_p1_veo_his_dv**	
		Default Value:	0h
		Access:	RO
	26	**iecp_p1_veo_skin_dv**	
		Default Value:	0h
		Access:	RO
	25	**iecp_p1_veo_out_dist_dv**	
		Default Value:	0h

VEO_STATE - VEO State Register

	Access:	RO
24	**veo_iecp_p0_rgb_his_hold**	
	Default Value:	0h
	Access:	RO
23	**Reserved**	
	Access:	RO
	Format:	MBZ
22:19	**VSC_FSM_State**	
	Default Value:	0h
	Access:	RO
	State of the VEO_VSC_CNTRL state machine	
18:16	**GAV Command Credit Count**	
	Default Value:	4h
	Access:	RO
15:12	**GAV Data Credit Count**	
	Default Value:	8h
	Access:	RO
11:8	**Reserved**	
	Access:	RO
	Format:	MBZ
7:0	**GAV Stall Clk Cnt Max**	
	Default Value:	0h
	Access:	RO
	The longest stall from GAV since the beginning of the frame.	

VE SFC Forced Lock Acknowledgement Register

VE_SFC_FORCED_LOCK_ACK - VE SFC Forced Lock Acknowledgement Register

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1CA018h
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS0
Address:	1DA018h
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS1
Address:	1EA018h
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS2
Address:	1FA018h
ShortName:	VE_SFC_FORCED_LOCK_ACK_VECS3

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**VE_SFC_FORCED_LOCK_ACK** Access: RO Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit is going to be polled by driver. This bit indicates that VE has received MFX_SFC_Forced_Lock from driver and it has sent that signal to SFC. Once this bit is set, it indicates SFC status (lock or unlock) will not be changed anymore. Driver will be safe to start the reset process after this bit is set. Hardware has to de-assert this bit after driver de-assert VE_SFC_Forced_Lock as well.

VE SFC Forced Lock Register

VE_SFC_FORCED_LOCK - VE SFC Forced Lock Register

Register Space:	MMIO: 0/2/0
Access:	WO
Size (in bits):	32
Address:	1CA01Ch
ShortName:	VE_SFC_FORCED_LOCK_01
Address:	1DA01Ch
ShortName:	VE_SFC_FORCED_LOCK_02
Address:	1EA01Ch
ShortName:	VE_SFC_FORCED_LOCK_03
Address:	1FA01Ch
ShortName:	VE_SFC_FORCED_LOCK_04

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**VE_SFC_FORCED_LOCK** Access: WO Format: U1 This bit can only be set by driver and it has to be clear by driver as well. Driver should set this bit before issuing the software (watchdog timer) reset. It tells VEBox that a software reset is going to happen. VE then issues a forced lock to SFC. If SFC is currently locked to VE, SFC should not unlock itself from VE. If SFC is NOT currently locked to VE, SFC should not accept the lock request from VE. Driver needs to clear this bit after the software reset sequence is complete.

VE VFW SFC Usage Register

VE_SFC_USAGE - VE VFW SFC Usage Register	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	1CA014h
ShortName:	VE_SFC_USAGE_VECS0
Address:	1DA014h
ShortName:	VE_SFC_USAGE_VECS1
Address:	1EA014h
ShortName:	VE_SFC_USAGE_VECS2
Address:	1FA014h
ShortName:	VE_SFC_USAGE_VECS3

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**VE_SFC_USAGE** Access: RO Format: U1 This bit can only be set by hardware and it has to be clear by hardware as well. This bit indicates SFC is currently locked to VE. This bit should be set after SFC accepts the lock request from VE. This bit should be clear once SFC finishes the workload and unlocked from VEBox. In case a reset happens on MFX, this bit must be reset once a new workload is received

VF_CAPABILITY_REGISTER

VF_CAP_REG - VF_CAPABILITY_REGISTER

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	1901F8h

This register is used to communicate information about the VF to the VM Drivers. The same offset (0x1901F8) is used for all VF and the PF.

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Virtual Function** Access: RO _Custom_GTIReset: BUS Value / Name: 0b – Physical Function **[Default]** 1b – Virtual Function

VF_SW_FLAG

VF_SW_FLAG	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	190240h
Name:	VF_SW_FLAG_0
ShortName:	VF_SW_FLAG_0
Address:	190244h
Name:	VF_SW_FLAG_1
ShortName:	VF_SW_FLAG_1
Address:	190248h
Name:	VF_SW_FLAG_2
ShortName:	VF_SW_FLAG_2
Address:	19024Ch
Name:	VF_SW_FLAG_3
ShortName:	VF_SW_FLAG_3

Each Virtual Function has 4x32bit Software Flag registers, which can be used as scratch registers.

DWord	Bit	Description
0	31:0	**Data** Default Value: 00000000h Access: R/W _Custom_GTIReset: BUS The format of this register is defined by Software.

VF ARI Capability

VF_ARI_CAP_0_2_0_PCI - VF ARI Capability		
Register Space:	PCI: 0/2/1	
Size (in bits):	16	
Address:	00104h	
VF ARI capability reports support for Alternative Routing ID (ARI) on Gfx device, compliant to PCI-Express ARI ECN.		

DWord	Bit	Description
0	15:8	**Next Function Number** Default Value: 02h Access: RO Variant _Custom_GTIReset: BUS Hardwired to 2. This field indicates the Function Number of the next higher number function in the device, or 00h if there are no higher number functions. Function 0 starts this linked list of functions.
	7:2	**Reserved** Access: RO Format: MBZ
	1	**ACS Function Groups Capability (A)** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0. Applicable only for Function 0; must be 0b for all other functions. If 1b, indicates that the ARI device supports Function Group level granularity for ACS P2P Egress Control via its ACS Capability Structures.
	0	**MFVC Function Groups Capability (M)** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0. Applicable only for Function 0; must be 0b for all other functions. If 1b, indicates that the ARI Device supports Function Group level arbitration via its Multi-function Virtual Channel (MFVC) Capability structure.

VF ARI Control

VF_ARI_CTRL_0_2_0_PCI - VF ARI Control

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	00106h

VF Alternative Routing ID (ARI) control for Gfx device.

DWord	Bit	Description
0	15:7	**Reserved** Access: RO Format: MBZ
	6:4	**Function Group** Default Value: 000b Access: RO _Custom_GTIReset: BUS Hardwired to 000b. Must be hardwired to 000b if in function 0, the MFVC Function Capability bit and ACS Function Groups Capability bit are both 0b.
	3:2	**Reserved** Access: RO Format: MBZ
	1	**ACS Function Groups Enable (A)** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0. Gfx does not support ACS Function Groups capability.
	0	**MFVC Function Groups Enable (M)** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0. Gfx does not support MFVC Function Group.

VF ARI Extended Capability Header

VF_ARI_CAPHDR_0_2_0_PCI - VF ARI Extended Capability Header

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	00100h

VF Alternative Routing Identification (ARI) capability reports support for more than 8 functions.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Access: RO _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list (0x000 - END) Value: 000000000000b — Name: EOL **[Default]**
	19:16	**Version** Default Value: 0001b Access: RO _Custom_GTIReset: BUS Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000001110b Access: RO _Custom_GTIReset: BUS Hardwired to 000Eh which is the PCI Express Extended Cap ID for the ARI capability.

VF BAR0 LDW

VF_BAR0_LDW_0_2_0_PCI - VF BAR0 LDW

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00344h

Lower DW of the BAR that defines the base address of GTTMMADR for all VFs.

DWord	Bit	Description
0	31:26	**VF GTTMMADDR Lower DW** Default Value: 0000000000h Access: R/W _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [31:26].
	25	**VF GTTMMADDR Lower DW Tile 1** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [25:24]. The accessibility of these registers is governed by the tile count. If 1 tile, then these are R/W.
	24	**VF GTTMMADDR Lower DW Tile 0** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Set by the OS, these bits correspond to address signals [25:24]. The accessibility of these registers is governed by the tile count. If 1 tile, then these are R/W.
	23:4	**VF GTTMMADDR Lower DW Mask** Default Value: 00000000000000000000000000b Access: RO _Custom_GTIReset: BUS VF GTTMMADDR Lower DW Mask
	3	**PREFETCHABLE** Access: RO Variant _Custom_GTIReset: BUS Indicates if a BAR is Prefetchable or Non-prefetchable

VF_BAR0_LDW_0_2_0_PCI - VF BAR0 LDW

		Value / **Name** 1b — PREFETCHABLE BAR **[Default]** 0b — NONPREFETCHABLE BAR
	2:1	**Type** Default Value: 10b Access: RO _Custom_GTIReset: BUS Type. Value 10 indicates 64 bit BAR
	0	**Memory Space Indicator** Default Value: 0b Access: RO _Custom_GTIReset: BUS Memory space Indicator. Value 0 indicates memory space.

VF BAR0 UDW

VF_BAR0_UDW_0_2_0_PCI - VF BAR0 UDW		
Register Space: PCI: 0/2/0 Size (in bits): 32		
Address: 00348h		
Upper DW of the BAR that defines the base address of GTTMMADR for all VFs		
DWord	**Bit**	**Description**
0	31:0	**VF GTTMMMADDR Upper DW** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS VF GTTMMADDR Upper DW

VF BAR1 LDW

VF_BAR1_LDW_0_2_0_PCI - VF BAR1 LDW

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	0034Ch

Description

Lower DW of the BAR that defines the base address of LMEMBAR for all VFs.

DWord	Bit	Description
0	31	**4GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 4GB
	30	**2GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 2GB
	29	**1GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 1GB
	28	**512MB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 512MB

VF_BAR1_LDW_0_2_0_PCI - VF BAR1 LDW

	27	**256MB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 256MB
	26:4	**VF LMEMBAR Lower DW Mask** Default Value: 00000000000000000000b Access: RO _Custom_GTIReset: BUS VF LMEMBAR Lower DW Mask
	3	**Prefetchable** Default Value: 1b Access: RO _Custom_GTIReset: BUS Indicates if a BAR is Prefetchable or Non-Prefetchable
	2:1	**Type** Default Value: 10b Access: RO _Custom_GTIReset: BUS Type. Value 10 indicates 64 bit BAR
	0	**Memory Space Indicator** Default Value: 0b Access: RO _Custom_GTIReset: BUS Memory space Indicator. Value 0 indicates memory space.

VF BAR1 UDW

VF_BAR1_UDW_0_2_0_PCI - VF BAR1 UDW

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00350h

Upper DW of the BAR that defines the base address of GMADR for all VFs

DWord	Bit	Description
0	31:7	**VF LMEMBAR Base Address** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS VF LMEMBAR Upper DW The VF resizable capability structure setting will affect the access attributes of this register. Bit 27 : 256MB Mask Bit 28 : 512MB Mask Bit 29 : 1GB Mask Bit 30 : 2GB Mask Bit 31 : 4GB Mask Bit 32 : 8GB Mask Bit 33 : 16GB Mask Bit 34 : 32GB Mask Bit 35 : 64GB Mask Bit 36 : 128GB Mask Bit 37 : 256GB Mask Bit 38 : 512GB Mask
	6	**512GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 512GB
	5	**256GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 256GB

VF_BAR1_UDW_0_2_0_PCI - VF BAR1 UDW

	4	**128GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 128GB
	3	**64GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 64GB
	2	**32GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 32GB
	1	**16GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 16GB
	0	**8GB Address Mask** Default Value: 0b Access: R/W _Custom_GTIReset: BUS This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of VFBAR1 Size. RO and forced to 0 when VFBAR1 Size >= 8GB

VF BAR2 LDW

VF_BAR2_LDW_0_2_0_PCI - VF BAR2 LDW		
Register Space:	PCI: 0/2/0	
Size (in bits):	32	
Address:	00354h	
Lower DW of Unused BAR		
DWord	**Bit**	**Description**
0	31:0	**Reserved Bar** Default Value: 00000000000000000000000000000000b Access: RO _Custom_GTIReset: BUS Reserved

VF BAR2 UDW

VF_BAR2_UDW_0_2_0_PCI - VF BAR2 UDW		
Register Space: PCI: 0/2/0 Size (in bits): 32		
Address: 00358h		
Upper DW of Unused BAR		
DWord	**Bit**	**Description**
0	31:0	**Reserved Bar** Default Value: 00000000000000000000000000000000b Access: RO _Custom_GTIReset: BUS Reserved

VF Built In Self Test

BIST_0_2_1_PCI - VF Built In Self Test

Register Space:	PCI: 0/2/1
Size (in bits):	8
Address:	0000Fh

This register is used for control and status of Built In Self Test (BIST).

DWord	Bit	Description
0	7	**BIST Supported** Default Value: 0b Access: RO _Custom_GTIReset: BUS BIST is not supported. This bit is hardwired to 0.
	6:0	**Reserved** Access: RO Format: MBZ

VF Cache Line Size

CLS_0_2_1_PCI - VF Cache Line Size		
Register Space:	PCI: 0/2/1	
Size (in bits):	8	
Address:	0000Ch	
DWord	**Bit**	**Description**
0	7:0	**Cache Line Size Value** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

VF Capabilities Pointer

CAPPOINT_0_2_1_PCI - VF Capabilities Pointer

Register Space:	PCI: 0/2/1
Size (in bits):	8
Address:	00034h

This register points to a linked list of capabilities implemented by this device.

DWord	Bit	Description
0	7:0	**Capabilities Pointer Value** Default Value: 01110000b Access: RO _Custom_GTIReset: BUS This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 70h.

VF Device Capabilities

DEVICECAP_0_2_1_PCI - VF Device Capabilities

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	00074h

PCI Express Device Capabilities

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28	**Functional Level Reset Capability** Default Value: 1b Access: RO _Custom_GTIReset: BUS Hardwired to 1b to indicate the Function supports the optional Function Level Reset mechanism.
	27:26	**Captured Slot Power Limit Scale** Default Value: 00b Access: RO _Custom_GTIReset: BUS Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00b
	25:18	**Captured Slot Power Limit Value** Default Value: 00000000h Access: RO _Custom_GTIReset: BUS Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00h
	17:16	**Reserved** Access: RO Format: MBZ
	15	**Role-Based Error Reporting** Default Value: 1b Access: RO _Custom_GTIReset: BUS When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated

DEVICECAP_0_2_1_PCI - VF Device Capabilities

		into PCI Express Base Specification, Revision 1.1.Hardwired to 1b as this bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
	14:12	**Reserved** Access: RO Format: MBZ
	11:9	**Endpoint L1 Acceptable Latency** Default Value: 111b Access: RO Variant _Custom_GTIReset: BUS This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state.
	8:6	**Endpoint L0s Acceptable Latency** Default Value: 111b Access: RO Variant _Custom_GTIReset: BUS This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state.
	5	**Extended Tag Field Supported** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit indicates the maximum supported size of the Tag field as a Requester. This does not apply to the integrated graphics device, so it is hardwired to 0b (5-bit Tag field supported).
	4:3	**Phantom Functions Supported** Default Value: 00b Access: RO _Custom_GTIReset: BUS This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices. This does not apply to the integrated graphics device, so it is hardwired to 00b to indicate no Function Number bits are used for Phantom Functions.
	2:0	**Max Payload Size Supported** Default Value: 000b Access: RO _Custom_GTIReset: BUS

DEVICECAP_0_2_1_PCI - VF Device Capabilities		
		This field indicates the maximum payload size that the Function can support for TLPs.Hardwired to 000b to represents 128 bytes, the minimum allowed value.

VF Device Capabilities 2

DEVCAP2_0_2_1_PCI - VF Device Capabilities 2

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	00094h

This register provides information on the PCIe Device capabilities.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30:28	**Reserved** Access: RO Format: MBZ
	27:21	**Reserved** Access: RO Format: MBZ
	20	**Extended Format Field** Default Value: 1b Access: RO _Custom_GTIReset: BUS If set, function supports 3 bit definition of FMT field. Functions are strongly recommended to supported 3-bit definition of FMT field.
	19:18	**OBFF Supported** Default Value: 00b Access: RO _Custom_GTIReset: BUS 00b OBFF not supported; 01b OBFF supported using message; 10b OBFF supported using WAKE# signaling; 11b OBFF supported using WAKE# and message signaling.
	17	**10-Bit Tag Requester Supported** Default Value: 1b Access: RO _Custom_GTIReset: BUS 10-Bit Tag Requester Supported
	16	**10-bit Tag Completer supported**

DEVCAP2_0_2_1_PCI - VF Device Capabilities 2

	Default Value:	1b
	Access:	RO
	_Custom_GTIReset:	BUS

10-bit Tag Completer Supported

15:14 **LN System CLS**

Default Value:	00b
Access:	RO
_Custom_GTIReset:	BUS

00b LN Completer not supported and not in effect

13:12 **TPH Completer Supported**

Default Value:	00b
Access:	RO
_Custom_GTIReset:	BUS

00b TPH and Extended TPH completer not supported.

11 **LTR Mechanism Supported**

Default Value:	1b
Access:	RO
_Custom_GTIReset:	BUS

1b indicates support for the options Latency Tolerance Reporting (LTR) mechanism.

10 **Reserved**

Access:	RO
Format:	MBZ

9:7 **AtomicOp Completer**

Default Value:	000b
Access:	RO
_Custom_GTIReset:	BUS

These bits apply if FetchAdd, Swap, and CAS AtomicOps are supported.

6:5 **Reserved**

Access:	RO
Format:	MBZ

4 **Completion Timeout Disable**

Default Value:	1b
Access:	RO

DEVCAP2_0_2_1_PCI - VF Device Capabilities 2

		_Custom_GTIReset: BUS Completion Timeout Disable supported. 1b indicates support for the completion timeout disable mechanism. Completion timeout disable is required for endpoints that issue requests on their own behalf.
	3:0	**Completion Timeout Range** Default Value: 0010b Access: RO _Custom_GTIReset: BUS Completion Timeout ranges supported. Range B : 10ms to 250ms (0010b)

VF Device ID

VF_DEVICEID_0_2_0_PCI - VF Device ID

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00338h

Defines the Device ID to be used by all Virtual Functions

DWord	Bit	Description
0	31:16	**VF DEVICE ID VALUE** Access: RO Variant _Custom_GTIReset: BUS Mirror the same device ID as the PF Value: 0000001000000001b — Name: **[Default]**
	15:0	**Reserved** Access: RO Format: MBZ

VF Device Identification

DID2_0_2_1_PCI - VF Device Identification		
Register Space:	PCI: 0/2/1	
Size (in bits):	16	
Address:	00002h	
This register combined with the Vendor Identification register uniquely identifies any PCI device.		
DWord	**Bit**	**Description**
0	15:0	**Device Identification Number** Default Value: 1111111111111111b Access: RO _Custom_GTIReset: BUS This is the upper part of a 16 bit value assigned to the device.

VF Header Type

HDR2_0_2_1_PCI - VF Header Type

Register Space:	PCI: 0/2/1
Size (in bits):	8
Address:	0000Eh

This register contains the Header Type of the IGD.

DWord	Bit	Description
0	7	**Multi Function Status** Default Value: 0b Access: RO _Custom_GTIReset: BUS Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.
	6:0	**Header Code** Default Value: 0000000b Access: RO _Custom_GTIReset: BUS This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.

VF Interrupt Line

INTRLINE_0_2_1_PCI - VF Interrupt Line		
Register Space:	PCI: 0/2/1	
Size (in bits):	8	
Address:	0003Ch	
This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.		
DWord	**Bit**	**Description**
0	7:0	**Interrupt Connection** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

VF Interrupt Pin

INTRPIN_0_2_1_PCI - VF Interrupt Pin		
Register Space:	PCI: 0/2/1	
Size (in bits):	8	
Address:	0003Dh	
This register tells which interrupt pin the device uses.		
DWord	**Bit**	**Description**
0	7:0	**Interrupt Pin Value** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.

VF Interrupt Trigger Register

VF_INT_TRIGGER - VF Interrupt Trigger Register

Register Space:	MMIO: 0/2/0
Size (in bits):	64
Address:	102030h

SRIOV64: VF Interrupt trigger register to log interrupts of each function from GT
GT writes to offset: 102030 with function# encoded in wr_data[5:0]
SGunit decodes the data and sets the respective bit in this register

DWord	Bit	Description	
0..1	63	**Interrupt function number 63**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	62	**Interrupt function number 62**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	61	**Interrupt function number 61**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	60	**Interrupt function number 60**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	59	**Interrupt function number 59**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	58	**Interrupt function number 58**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	57	**Interrupt function number 57**	
		Default Value:	0h
		Access:	R/W

VF_INT_TRIGGER - VF Interrupt Trigger Register

		_Custom_GTIReset:	BUS
	56	**Interrupt function number 56**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	55	**Interrupt function number 55**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	54	**Interrupt function number 54**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	53	**Interrupt function number 53**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	52	**Interrupt function number 52**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	51	**Interrupt function number 51**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	50	**Interrupt function number 50**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	49	**Interrupt function number 49**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	48	**Interrupt function number 48**	
		Default Value:	0h
		Access:	R/W

VF_INT_TRIGGER - VF Interrupt Trigger Register

		_Custom_GTIReset:	BUS
	47	**Interrupt function number 47**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	46	**Interrupt function number 46**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	45	**Interrupt function number 45**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	44	**Interrupt function number 44**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	43	**Interrupt function number 43**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	42	**Interrupt function number 42**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	41	**Interrupt function number 41**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	40	**Interrupt function number 40**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	39	**Interrupt function number 39**	
		Default Value:	0h
		Access:	R/W

VF_INT_TRIGGER - VF Interrupt Trigger Register

		_Custom_GTIReset:	BUS
	38	**Interrupt function number 38**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	37	**Interrupt function number 37**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	36	**Interrupt function number 36**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	35	**Interrupt function number 35**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	34	**Interrupt function number 34**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	33	**Interrupt function number 33**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	32	**Interrupt function number 32**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	31	**Interrupt function number 31**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	30	**Interrupt function number 30**	
		Default Value:	0h
		Access:	R/W

VF_INT_TRIGGER - VF Interrupt Trigger Register

		_Custom_GTIReset:	BUS
	29	**Interrupt function number 29**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	28	**Interrupt function number 28**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	27	**Interrupt function number 27**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	26	**Interrupt function number 26**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	25	**Interrupt function number 25**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	24	**Interrupt function number 24**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	23	**Interrupt function number 23**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	22	**Interrupt function number 22**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	21	**Interrupt function number 21**	
		Default Value:	0h
		Access:	R/W

VF_INT_TRIGGER - VF Interrupt Trigger Register

		_Custom_GTIReset:	BUS
	20	**Interrupt function number 20**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	19	**Interrupt function number 19**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	18	**Interrupt function number 18**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	17	**Interrupt function number 17**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	16	**Interrupt function number 16**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	15	**Interrupt function number 15**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	14	**Interrupt function number 14**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	13	**Interrupt function number 13**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	12	**Interrupt function number 12**	
		Default Value:	0h
		Access:	R/W

VF_INT_TRIGGER - VF Interrupt Trigger Register

		_Custom_GTIReset:	BUS
	11	**Interrupt function number 11**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	10	**Interrupt function number 10**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	9	**Interrupt function number 9**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	8	**Interrupt function number 8**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	7	**Interrupt function number 7**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	6	**Interrupt function number 6**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	5	**Interrupt function number 5**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	4	**Interrupt function number 4**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	3	**Interrupt function number 3**	
		Default Value:	0h
		Access:	R/W

VF_INT_TRIGGER - VF Interrupt Trigger Register

		_Custom_GTIReset:	BUS
	2	**Interrupt function number 2**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	1	**Interrupt function number 1**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS
	0	**Interrupt function number 0**	
		Default Value:	0h
		Access:	R/W
		_Custom_GTIReset:	BUS

VF Link Capabilities

LINKCAP_0_2_1_PCI - VF Link Capabilities

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	0007Ch

This register provides information on the PCIe link capabilities.

DWord	Bit	Description
0	31:24	**Port Number** Default Value: 00h Access: RO _Custom_GTIReset: BUS PCIe port number for the given PCIe link.
	23	**Reserved** Access: RO Format: MBZ
	22	**ASPM Optionality Compliance** Default Value: 1b Access: RO _Custom_GTIReset: BUS This bit must be set to 1b in all Functions. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests
	21	**Link Bandwidth Notification Cap** Default Value: 0b Access: RO _Custom_GTIReset: BUS This field is reserved for PCIe endpoints.
	20	**Link Active Report Cap** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit must be 1b if component supports optional cap of reported DL_Active state.
	19	**Surprise Down Report Cap** Default Value: 0b

LINKCAP_0_2_1_PCI - VF Link Capabilities

	Access:	RO
	_Custom_GTIReset:	BUS
	Set if optional capability of detecting and reporting a surprise down error condition.	
18	**Clock PM**	
	Default Value:	0b
	Access:	RO
	_Custom_GTIReset:	BUS
	For downstream ports, this bit must be hardwired to 0b.	
17:15	**L1 Exit Latency**	
	Default Value:	000b
	Access:	RO
	_Custom_GTIReset:	BUS
	This field indicates the L1 exit latency of the given PCIe link. The value reported indicates the length of time this port required to complete transtion from ASPM L1 to L0. 000b=less than 1us.	
14:12	**L0s Exit Latency**	
	Default Value:	000b
	Access:	RO
	_Custom_GTIReset:	BUS
	This field indicates the L0s exit latency fo the given PCIe link. The value reported indicates the length of time this port requires to complete transition from L0s to L0. 000b=less than 64ns.	
11:10	**Active State PM**	
	Default Value:	11b
	Access:	RO
	_Custom_GTIReset:	BUS
	This field indicates the level of ASPM supported on the given PCIe Link. Hardwired to 11 to indicate L0s and L1 supported.	
9:4	**Max Link Width**	
	Default Value:	000001b
	Access:	RO
	_Custom_GTIReset:	BUS
	Maximum Link Width Per IOSF spec recommendation, report x1. Encoding is 00 0001b (x1 width).	
3:0	**Max LInk Speed**	

LINKCAP_0_2_1_PCI - VF Link Capabilities

Default Value:	0001b
Access:	RO
_Custom_GTIReset:	BUS

Max Link Speed Per IOSF Spec, report Gen1. This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. The encoding is 0001b.

VF Link Capabilities 2

LINKCAP2_0_2_1_PCI - VF Link Capabilities 2

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	0009Ch

This register provides information on the link capabilities 2 register

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:1	**Supported Link Speed Vector** Default Value: 000001b 2_5GTs Access: RO _Custom_GTIReset: BUS This field indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. See Section 8.2.1 for further requirements. Bit definitions within this field are: Bit 0: 2.5 GT/s Bit 1: 5.0 GT/s Bit 2: 8.0 GT/s Bit 3: 16.0 GT/s Bits 6:4: RsvdP Multi-Function Devices associated with an Upstream Port must report the same value in this field for all Functions
	0	**Reserved** Access: RO Format: MBZ

VFL Scratch Pad

VFLSKPD - VFL Scratch Pad

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	062A8h-062ABh
Name:	VFL Scratch Pad Registers
ShortName:	VFLSKPD_SVGUNIT
Address:	172A8h-172ABh
Name:	VFL Scratch Pad Registers
ShortName:	VFLSKPD_SVGRUNIT

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask[15:0] _Custom_GTIReset: DEV Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)
	15	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	14:13	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	12	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	11	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV

VFLSKPD - VFL Scratch Pad

10 **Reserved**

Access:	RO
Format:	MBZ

9 **Partial Autostrip Disable**

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Enable_9 **[Default]**	The VF can generate "partial autostrip" primitives from TRILIST inputs (if/when possible).
1h	Disable_9	VF will not generate "partial autostrip" primitives

8 **Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

7 **Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

6 **Autostrip Disable**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Enable_6 **[Default]**	The VF can generate "autostrip" primitives from TRILIST inputs (if/when possible).
1h	Disable_6	VF will not generate "autostrip" primitives.

5 **TLB Prefectch Enable**

Access:	R/W
Format:	U1
_Custom_GTIReset:	DEV

Value	Name	Description
0h	Disable_5 **[Default]**	The VF will generate prefetch of TLB when it is fetching sequential vertex data and four or fewer vertex buffers are valid.
1h	Enable_5	VF will disable prefetch of TLB entries.

VFLSKPD - VFL Scratch Pad

4	**Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

3	**Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

2	**Reserved**

Access:	R/W
Format:	PBC
_Custom_GTIReset:	DEV

1	**Disable Over Fetch Cache**

Access:	R/W
_Custom_GTIReset:	DEV

Value	Name	Description
0h	**[Default]**	Cache will check for data in cache before making a request to memory
1h		Always re-fetch new data from memory.

Programming Notes
Note that the Disable Multiple Miss Read squash bit must be cleared for Disable Over Fetch Cache to be set.

0	**Disable Multiple Miss Read squash**

Access:	R/W
Format:	Disable
_Custom_GTIReset:	DEV

Value	Name	Description
0h	**[Default]**	Allow VF to squash reads that are to the same cacheline for vertex buffer requests.
1h		Disallow VF from squashing reads that are to the same cacheline for vertex buffer requests.

VF Primary Latency Timer

MLT2_0_2_1_PCI - VF Primary Latency Timer		
Register Space:	PCI: 0/2/1	
Size (in bits):	8	
Address:	0000Dh	
The IGD does not support the programmability of the primary latency timer because it does not perform bursts.		
DWord	**Bit**	**Description**
0	7:0	**Primary Latency Timer Count Value** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s.

VF Maximum Latency

MAXLAT_0_2_1_PCI - VF Maximum Latency		
Register Space:	PCI: 0/2/1	
Size (in bits):	8	
Address:	0003Fh	
The Integrated Graphics Device has no requirement for the settings of Latency Timers.		
DWord	**Bit**	**Description**
0	7:0	**Maximum Latency Value** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.

VF Message Address

MA_0_2_1_PCI - VF Message Address

Register Space:	PCI: 0/2/1
Size (in bits):	64
Address:	000B0h

This register contains the Message Address for MSIs sent by the device.

DWord	Bit	Description
0	63:32	**Message Address MSB** Default Value: 0x00000000 Access: R/W _Custom_GTIReset: BUS Used by system software to assign the upper DWORD of MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
	31:2	**Message Address LSB** Default Value: 00000000000000000000000000000000b Access: R/W _Custom_GTIReset: BUS Used by system software to assign an MSI address to the device.The device handles an MSI by writing the padded contents of the MD register to this address.
	1:0	**Reserved** Access: RO Format: MBZ

VF Message Control

MC_0_2_1_PCI - VF Message Control

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	000AEh

Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

DWord	Bit	Description
0	15:9	**Reserved** Access: RO Format: MBZ
	8	**Per Vector Mask Capable** Default Value: 1b Access: RO _Custom_GTIReset: BUS SR-IOV requires this capability.
	7	**64 Bit Capable** Access: RO _Custom_GTIReset: BUS Description: Hardwired to 1 to indicate that the function is capable of generating a 64-bit memory address. Value: 1b — Name: **[Default]**
	6:4	**Multiple Message Enable** Default Value: 000b Access: R/W _Custom_GTIReset: BUS System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. Value: Number of requests000: 1001: 2010: 4011: 8100: 16101: 32110: Reserved111: Reserved

MC_0_2_1_PCI - VF Message Control

	3:1	**Multiple Message Capable** Default Value: 000b Access: RO _Custom_GTIReset: BUS System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.
	0	**MSI Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Controls the ability of this device to generate MSIs.

VF Message Data

MD_0_2_1_PCI - VF Message Data

Register Space: PCI: 0/2/1
Size (in bits): 16

Address: 000B8h

This register contains the Message Data for MSIs sent by the device.

DWord	Bit	Description
0	15:0	**Message Data** Default Value: 0000000000000000b Access: R/W _Custom_GTIReset: BUS Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

VF Message Signaled Interrupts Capability ID

MSI_CAPID_0_2_1_PCI - VF Message Signaled Interrupts Capability ID

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	000ACh

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

DWord	Bit	Description
0	15:8	**Pointer to Next Capability** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list.
	7:0	**Capability ID** Default Value: 00000101b Access: RO _Custom_GTIReset: BUS This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.

VF Migration State Array Offset

VF_MIGST_OFFSET_0_2_0_PCI - VF Migration State Array Offset

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	0035Ch

Defines offset from a PF BAR to the VF Migration State Array. VF Migration not supported in this implementation

DWord	Bit	Description
0	31:0	**Reserved bits** Default Value: 00000000000000000000000000000000b Access: RO _Custom_GTIReset: BUS Reserved

VF Minimum Grant

MINGNT_0_2_1_PCI - VF Minimum Grant		
Register Space:	PCI: 0/2/1	
Size (in bits):	8	
Address:	0003Eh	
The Integrated Graphics Device has no requirement for the settings of Latency Timers.		
DWord	**Bit**	**Description**
0	7:0	**Minimum Grant Value** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s because the IGD does not burst as a PCI compliant primary.

VF MSI Mask Bits

MSI_MASK_0_2_1_PCI - VF MSI Mask Bits

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	000BCh

This register contains the MSI Mask Bits

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Mask Bit for Vector 0** Default Value: 0b Access: R/W _Custom_GTIReset: BUS For each Mask bit that is set, the function is prohibited from sending the associated message.

VF MSI Pending Bits

MSI_PEND_0_2_1_PCI - VF MSI Pending Bits

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	000C0h

This register contains the MSI Pending Bits

DWord	Bit	Description
0	31:1	**Reserved** Access: RO Format: MBZ
	0	**Pending Bit for Vector 0** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS For each Pending bit that is set, the function has a pending associated message. If this bit is set when the corresponding vector's Mask bit is cleared, the function will send an MSI and then clear the Pending bit.

VF PCI Command

PCICMD_0_2_1_PCI - VF PCI Command

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	00004h

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant primary accesses to main memory.

DWord	Bit	Description
0	15:11	**Reserved** Access: RO Format: MBZ
	10	**Interrupt Disable** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit disables the device from asserting INT interrupts. Hardwired to 0.
	9	**Fast Back-to-Back** Default Value: 0b Access: RO _Custom_GTIReset: BUS Not Implemented. Hardwired to 0.
	8	**SERR Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Not Implemented. Hardwired to 0.
	7	**Wait Cycle Control** Default Value: 0b Access: RO _Custom_GTIReset: BUS Not Implemented. Hardwired to 0.

PCICMD_0_2_1_PCI - VF PCI Command

6	**Parity Error Enable**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.

5	**Video Palette Snooping**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

This bit is hardwired to 0 to disable snooping.

4	**Memory Write and Invalidate Enable**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 0. The IGD does not support memory write and invalidate commands.

3	**Special Cycle Enable**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

This bit is hardwired to 0. The IGD ignores Special cycles.

2	**Bus Primary Enable**

Default Value:	0b
Access:	R/W
_Custom_GTIReset:	BUS

0: Disable IGD bus primary. 1: Enable the IGD to function as a PCI compliant primary.

1	**Memory Access Enable**

Default Value:	0b
Access:	RO
_Custom_GTIReset:	BUS

Hardwired to 0 (does not apply to VFs). VF memory space is controlled by VF MSE bit in VF control register.

PCICMD_0_2_1_PCI - VF PCI Command

	0	**I/O Access Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 (does not apply to VFs)

VF PCI Express Capability

PCIECAP_0_2_1_PCI - VF PCI Express Capability

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	00072h

PCI Express Capability

DWord	Bit	Description
0	15:14	**Reserved** Access: RO Format: MBZ
	13:9	**Interrupt Message Number** Default Value: 00000b Access: RO _Custom_GTIReset: BUS This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Since this device only supports one MSI vector, this field is hardwired to 0.
	8	**Slot Implemented** Default Value: 0b Access: RO _Custom_GTIReset: BUS This field is hardwired to 0 for an endpoint device.
	7:4	**Device Type** Access: RO _Custom_GTIReset: BUS This field is hardwired to 0h to indicate a PCIe Endpoint 9h to indicate a Root complex integrated end point Value: 0000b — Name: **[Default]**
	3:0	**Capability Version** Default Value: 0010b Access: RO _Custom_GTIReset: BUS This field is hardwired to 2h to indicate Functions compliant to PCI Express 3.0 Base Specification.

VF PCI Express Capability Header

PCIECAPHDR_0_2_1_PCI - VF PCI Express Capability Header

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	00070h

PCI Express Capability Header

DWord	Bit	Description
0	15:8	**Next Capability Pointer** Default Value: 10101100b Access: RO _Custom_GTIReset: BUS This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.
	7:0	**Capability Identifier** Default Value: 00010000b Access: RO _Custom_GTIReset: BUS This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.

VF PCI Express Capability Structure

DEVICESTS_0_2_1_PCI - VF PCI Express Capability Structure

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	0007Ah

PCI Express Capability Structure

DWord	Bit	Description
0	15:6	**Reserved** Access: RO Format: MBZ
	5	**Transactions Pending** Default Value: 0b Access: RO Variant _Custom_GTIReset: BUS When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed. A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
	4	**Aux Power Detected** Default Value: 0b Access: RO _Custom_GTIReset: BUS Functions that require Aux power report this bit as Set if Aux power is detected by the Function. Hardwired to 0b, the integrated graphics device does not require Aux power.
	3	**Unsupported Request Detected** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit indicates the Function received an Unsupported Request. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
	2	**Fatal Error Detected** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit indicates the status of Fatal errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.

DEVICESTS_0_2_1_PCI - VF PCI Express Capability Structure

	1	**Non-Fatal Error Detected** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit indicates the status of Non-Fatal errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
	0	**Correctable Error Detected** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit indicates the status of Correctable errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.

VF PCI Express Device Control

DEVICECTL_0_2_1_PCI - VF PCI Express Device Control

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	00078h

PCI Express Device Control

DWord	Bit	Description
0	15	**Initiate Function Level Reset** Default Value: 0b Access: R/W _Custom_GTIReset: BUS A write of 1b initiates Function Level Reset to the Function. During FLR, a read will return 1b since device 2 reads abort. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.
	14:12	**Max Read Request Size** Default Value: 000b Access: RO _Custom_GTIReset: BUS Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.
	11	**Enable No Snoop** Default Value: 0b Access: RO _Custom_GTIReset: BUS This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates. The graphics device never generates a PCI Express TLP.
	10	**Aux Power PM Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Functions that do not implement this capability hardwire this bit to 0b.

DEVICECTL_0_2_1_PCI - VF PCI Express Device Control

9	**Phantom Functions Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Functions that do not implement this capability hardwire this bit to 0b.
8	**Extended Tag field Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Functions that do not implement this capability hardwire this bit to 0b.
7:5	**Max Payload Size** Default Value: 000b Access: RO _Custom_GTIReset: BUS Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.
4	**Enable Relaxed Ordering** Default Value: 0b Access: RO _Custom_GTIReset: BUS A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. The graphics device never generates a PCI Express TLP.
3	**Unsupported Request Response Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
2	**Fatal Error Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.

DEVICECTL_0_2_1_PCI - VF PCI Express Device Control

	1	**Non-Fatal Error Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
	0	**Correctable Error Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.

VF PCI Status

PCISTS2_0_2_1_PCI - VF PCI Status

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	00006h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant primary abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

DWord	Bit	Description
0	15	**Detected Parity Error** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: BUS Since the IGD does not detect parity, this bit is always hardwired to 0.
	14	**Signaled System Error** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: BUS The IGD never asserts SERR#, therefore this bit is hardwired to 0.
	13	**Received Primary Abort Status** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: BUS The IGD never gets a Primary Abort, therefore this bit is hardwired to 0.
	12	**Received Target Abort Status** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: BUS The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
	11	**Signaled Target Abort Status** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: BUS Hardwired to 0. The IGD does not use target abort semantics.

PCISTS2_0_2_1_PCI - VF PCI Status

	10:9	**DEVSEL Timing** Default Value: 00b Access: R/W One Clear _Custom_GTIReset: BUS Hardwired to 00.
	8	**Primary Data Parity Error Detected** Default Value: 0b Access: R/W One Clear _Custom_GTIReset: BUS Hardwired to 0. Not required for VF.
	7	**Fast Back-to-Back** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 to be compliant to PCI Express Base Spec (rev 3.0).
	6	**User Defined Format** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0.
	5	**66 MHz PCI Capable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0.
	4	**Capability List** Default Value: 1b Access: RO _Custom_GTIReset: BUS Indicates presence of Extended capabilities. All PCIe functions must support this. Hardwired to 1.

PCISTS2_0_2_1_PCI - VF PCI Status

	3	**Interrupt Status** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0. Does not apply for VFs.
	2:0	**Reserved** Access: RO Format: MBZ

VF Resizable Capability

VF_RESIZE_CAP_0_2_0_PCI - VF Resizable Capability

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00224h

VF Resizable capability reports support for VF Resizing of Gfx device VF LMEMBAR sizes.

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:12	**VFSUPSIZES** Default Value: 111111111111b Access: RO Variant _Custom_GTIReset: BUS Hardwired to 1s. Bit 12=Function will operate with BAR sized to 256MB. Bit 13=Function will operate with BAR sized to 512MB. Bit 14=Function will operate with BAR sized to 1GB. Bit 15=Function will operate with BAR sized to 2GB. Bit 16=Function will operate with BAR sized to 4GB. Bit 17=Function will operate with BAR sized to 8GB. Bit 18=Function will operate with BAR sized to 16GB. Bit 19=Function will operate with BAR sized to 32GB. Bit 20=Function will operate with BAR sized to 64GB. Bit 21=Function will operate with BAR sized to 128GB. Bit 22=Function will operate with BAR sized to 256GB. Bit 23=Function will operate with BAR sized to 512GB.
	11:4	**VFUNSUPSIZES** Default Value: 00000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s. Bit 4=Function will operate with BAR sized to 1MB. Bit 5=Function will operate with BAR sized to 2MB. Bit 6=Function will operate with BAR sized to 4MB. Bit 7=Function will operate with BAR sized to 8MB. Bit 8=Function will operate with BAR sized to 16MB. Bit 9=Function will operate with BAR sized to 32MB. Bit 10=Function will operate with BAR sized to 64MB. Bit 11=Function will operate with BAR sized to 128MB.

VF_RESIZE_CAP_0_2_0_PCI - VF Resizable Capability			
	3:0	**Reserved**	
		Access:	RO
		Format:	MBZ

VF Resizable Capability Header

VF_RESIZE_CAPHDR_0_2_0_PCI - VF Resizable Capability Header

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00220h

VF Resizablecapabilityallows the VF LMEMBAR value to be resized for each VF.

DWord	Bit	Description
0	31:20	**Next Capability Offset** Access: RO _Custom_GTIReset: BUS This is a hardwired pointer to the next item in the capabilities list (0x320 SRIOV Extended Capability Header). Value: 001100100000b — Name: 0x320 - SRIOV Extended Capability **[Default]**
	19:16	**Version** Default Value: 0001b Access: RO _Custom_GTIReset: BUS Hardwired to capability version 1.
	15:0	**Capability ID** Default Value: 0000000000100100b Access: RO _Custom_GTIReset: BUS Hardwired to 0024h which is the PCI Express Extended Cap ID for the VF Resizable BAR capability.

VF Resizable Control

VF_RESIZABLE_CTRL_0_2_0_PCI - VF Resizable Control

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00228h

VF Resizable BAR control for Gfx device.

DWord	Bit	Description
0	31:14	**Reserved** Access: RO Format: MBZ
	13:8	**VF BAR Size** Access: R/W _Custom_GTIReset: BUS VF Bar Size - This is an encode value. 0=1MB (2^20) 1=2MB (2^21) 2=4MB (2^22) 3=8MB (2^23) ... 8=256MB ... 13=8GB 14=16GB 15=32GB 16=64GB ... 43=8EB (2^63) The default value of this field is equal to the default size of the address space that the VFBAR resource is requesting via the VFBAR's Read-only bits. Behavior is undefined if a value is written in the field and the corresponding supported size bit is not Set in the VF Resizable BAR Capability or VF Resizable BAR control registers. When this register field is programmed, the value is immediately reflected in the size of the resource, as encoded in the number of read-only bits in the VF BAR. Note that this value represents the size of a BAR for a single VF. The total space required for all enabled VFs depends on the Num VF value in the SRIOV Extended Capability Structure. Value: 001000b — Name: **[Default]**

VF_RESIZABLE_CTRL_0_2_0_PCI - VF Resizable Control

	7:5	**Num VF Resizable BARs** Default Value: 1b Access: RO _Custom_GTIReset: BUS Hardwired to 1, only VF LMEMBAR is resizable. Indicates the total number of resizable VB BARs in the capability structure for the function. The value of this field must be in the range of 1h to 6h. The field is valid in VB Resizable BAR control register (0).
	4:0	**VF Bar Index** Default Value: 02h Access: RO _Custom_GTIReset: BUS ATS value = 02h which indicates VF BAR1 Lower DW (64b BAR) 0=VF BAR at offset 24h 1=VF BAR at offset 28h 2=VF BAR at offset 2Ch 3=VF BAR at offset 30h 4=VF BAR at offset 34h 5=VF BAR at offset 38h For a 64-bit Base address register, the VF BAR index indicates the lower Dword. This value indicates which VF BAR supports a negotiable size.

VF Revision Identification and Class Code

RID2_CC_0_2_1_PCI - VF Revision Identification and Class Code

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	00008h

This register contains the revision number for Device #2 Function 1. This register also contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code. Mirrored from PF RID and Class code register.

DWord	Bit	Description
0	31:24	**Base Class Code** Default Value: 00000011b Access: RO Variant _Custom_GTIReset: BUS This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 04h, indicating a Multimedia Device.
	23:16	**Sub-Class Code** Default Value: 00000000b Access: RO Variant _Custom_GTIReset: BUS When MGGC0[VAMEN] is 0 this value will be determined based on Device 0 GGC register, GMS and IVD fields.00h: VGA compatible80h: Non VGA (GMS = "00h" or IVD = "1b")When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device.
	15:8	**Programming Interface** Default Value: 00000000b Access: RO Variant _Custom_GTIReset: BUS When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.
	7:4	**Revision Identification Number MSB** Default Value: 0000b Access: RO Variant _Custom_GTIReset: BUS Four MSB of RID

RID2_CC_0_2_1_PCI - VF Revision Identification and Class Code

	3:0	**Revision Identification Number** Default Value: 0000b Access: RO Variant _Custom_GTIReset: BUS Four LSB of RID

VF Scratch Pad

VFSKPD - VF Scratch Pad

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	083A8h-083ABh
Name:	VF Scratch Pad
ShortName:	VFSKPD_VFUNIT
Address:	16EA8h-16EABh
Name:	VF Scratch Pad
ShortName:	VFSKPD_VFRUNIT

DWord	Bit	Description
0	31:16	**Mask** Access: WO Format: Mask _Custom_GTIReset: DEV Must be set to modify corresponding bit in Bits 15:0. (All bits implemented)
	15	**Reserved** Access: RO Format: MBZ
	14	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	13	**Mid Object Preemption Topology Fix Disable** Access: R/W Format: Disable _Custom_GTIReset: DEV Value / Name / Description 0h / Enable **[Default]** / VF replay topology fix is enabled - VF will output correct topology after Object Level Pre-emption. 1h / / VF replay topology fix is disabled

VFSKPD - VF Scratch Pad

	12	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
	11	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
	10	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
	9	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
	8	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
	7	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
	6	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
	5	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV
	4	**Reserved**
		Access: R/W
		Format: PBC
		_Custom_GTIReset: DEV

VFSKPD - VF Scratch Pad

	3	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	2	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	1	**Reserved** Access: R/W Format: PBC _Custom_GTIReset: DEV
	0	**VFG OA Cull enable** Access: R/W Format: PBC _Custom_GTIReset: DEV

Value	Name	Description
0h	**[Default]**	VFG will accept all draws. [] When Mesh Shading is Enabled, VFG will accept all 3DMESH commands.
1h		VFG will cull all draws [] When Mesh Shading is Enabled, VFG will cull all 3DMESH commands.

VF Stride

VF_STRIDE_0_2_0_PCI - VF Stride		
Register Space:	PCI: 0/2/0	
Size (in bits):	16	
Address:	00336h	
Defines the stride of the function number from one VF to the next.		
DWord	**Bit**	**Description**
0	15:0	**VF STRIDE VALUE** Default Value: 0000000000000001b Access: RO _Custom_GTIReset: BUS Defines the Routing ID offset from one VF to the next one for all VFs associated with the PF that contains this Capability structure. The next VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the current VF, ignoring any carry, using unsigned 16-bit arithmetic. The value of this field is hardwired to 0001h.

VF Subsystem Identification

SID2_0_2_1_PCI - VF Subsystem Identification		
Register Space:	PCI: 0/2/1	
Size (in bits):	16	
Address:	0002Eh	
This register is used to uniquely identify the subsystem where the PCI device resides.		
DWord	**Bit**	**Description**
0	15:0	**Subsystem Identification** Default Value: 0000000000000000b Access: RO Variant _Custom_GTIReset: BUS This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

VF Subsystem Vendor Identification

SVID2_0_2_1_PCI - VF Subsystem Vendor Identification

Register Space:	PCI: 0/2/1
Size (in bits):	16
Address:	0002Ch

This register is used to uniquely identify the subsystem where the PCI device resides. Mirrored from PF register.

DWord	Bit	Description
0	15:0	**Subsystem Vendor ID** Default Value: 0000000000000000b Access: RO Variant _Custom_GTIReset: BUS This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

VF Vendor Identification

VID2_0_2_1_PCI - VF Vendor Identification		
Register Space: PCI: 0/2/1 Size (in bits): 16		
Address: 00000h		
This register combined with the Device Identification register uniquely identifies any PCI device.		
DWord	**Bit**	**Description**
0	15:0	**Vendor Identification Number** Default Value: 1111111111111111b Access: RO _Custom_GTIReset: BUS PCI standard identification for Intel.

VF Video BIOS ROM Base Address

ROMADR_0_2_1_PCI - VF Video BIOS ROM Base Address

Register Space:	PCI: 0/2/1
Size (in bits):	32
Address:	00030h

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

DWord	Bit	Description
0	31:18	**ROM Base Address** Default Value: 00000000000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0's.
	17:11	**Address Mask** Default Value: 0000000b Access: RO _Custom_GTIReset: BUS Hardwired to 0s to indicate 256 KB address range.
	10:1	**Reserved** Access: RO Format: MBZ
	0	**ROM BIOS Enable** Default Value: 0b Access: RO _Custom_GTIReset: BUS Hardwired to 0 to indicate ROM not accessible.

VFW Credit Count Register

VFW_CREDIT_CNT - VFW Credit Count Register		
Register Space:	MMIO: 0/2/0	
Access:	RO	
Size (in bits):	32	
Address:	1CA010h	
ShortName:	VFW_CREDIT_CNT_01	
Address:	1DA010h	
ShortName:	VFW_CREDIT_CNT_02	
Address:	1EA010h	
ShortName:	VFW_CREDIT_CNT_03	
Address:	1FA010h	
ShortName:	VFW_CREDIT_CNT_04	

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:0	**Credit Count** Default Value: 4h Access: RO The number of outstanding credits between VFW and GAV. If zero VEBOX cannot proceed due to GAV not releasing credits.

VGA_CONTROL

VGA_CONTROL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	41000h-41003h
Name:	VGA Control
ShortName:	VGA_CONTROL
Reset:	global

Restriction

VGA requires panel fitting to be enabled.VGA is always connected to pipe A.VGA can not be enabled while the display power well is powered down.VGA display should only be enabled if all display planes other than VGA are disabled.

DWord	Bit	Description
0	31	**VGA Display Disable** Access: R/W This bit will disable the VGA compatible display mode.It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA I/O register settings. Value: 0b — Name: Enable Value: 1b — Name: Disable **[Default]** **Restriction** The VGA SR01 screen off bit must be programmed when enabling and disabling VGA. See the VGA Registers document.
	30:27	**Reserved** Access: RO Format: MBZ
	26	**VGA Border Enable** Access: R/W This bit determines if the VGA border areas are included in the active display area.The border will be scaled along with the pixel data. Value: 0b — Name: Disable Value: 1b — Name: Enable
	25	**DBuf Clock Gate**

	Access:	R/W

The bit controls the Display buffer clocking when VGA is used.
Software must set this bit to 0b before enabling VGA and set it to 1b after VGA gets disabled.

24 Pipe CSC Enable

Access:	R/W

This bit enables pipe color space conversion and the pipe pre-CSC gammafor the VGA pixel data.

Value	Name
0b	Disable
1b	Enable

23:21 Reserved

Access:	RO
Format:	MBZ

20 Legacy 8Bit Palette En

Access:	R/W

This bit affects reads and writes to the palette through VGA I/O addresses.In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read.This provides backward compatibility for original VGA programs as well as VESA VBE support for 8-bit palette.It does not affect palette accesses through the palette register MMIO path.

Value	Name
0b	6 bit DAC
1b	8 bit DAC

19 Reserved

Access:	R/W

18 Reserved

Access:	R/W

17:16 Reserved

Access:	RO
Format:	MBZ

15:12 Reserved

Access:	R/W

11:8 Reserved

Access:	R/W

7:6 Blink Duty Cycle

Access:	R/W

Controls the VGA text mode blink duty cycle relative to the VGA cursor blink duty cycle.

VGA_CONTROL

Value	Name	Description
00b	100%	100% Duty Cycle, Full Cursor Rate
01b	25%	25% Duty Cycle, 1/2 Cursor Rate
10b	50%	50% Duty Cycle, 1/2 Cursor Rate
11b	75%	75% Duty Cycle, 1/2 Cursor Rate

5:0 **VSYNC Blink Rate**

Access:	R/W

Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle.

Programming Notes
Program with (VSYNCs/cycle)/2-1

VIDEO_DIP_CTL

VIDEO_DIP_CTL

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	60200h-60203h
Name:	Transcoder Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_A
Reset:	soft

Address:	61200h-61203h
Name:	Transcoder Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_B
Reset:	soft

Address:	62200h-62203h
Name:	Transcoder Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_C
Reset:	soft

Address:	63200h-63203h
Name:	Transcoder Video Data Island Packet Control
ShortName:	VIDEO_DIP_CTL_D
Reset:	soft

Each type of Video DIP will be sent once each frame while it is enabled.

DWord	Bit	Description
0	31	**Disable SDP CRC** Access: R/W This bit is to enable or disable CRC on all SDPs universally. Note that CRC is calculated only on the SDP payload. HW is not tracking that its new vs replay of metadata. **Value** / **Name**: 0b – Do not disable SDP CRC **[Default]** 1b – Disable SDP CRC **Restriction**: SDP CRC can only be enabled for DP2.0. HW will automatically disable SDP CRC for DP1.x.

VIDEO_DIP_CTL

30 Allow DB Stall

Access:	R/W

This field controls whether double buffer updates are allowed to be stalled for this register.

Value	Name
0b	Not Allowed **[Default]**
1b	Allowed

29 Reserved

Access:	R/W

28 DRM DIP enable

Access:	Double Buffered

This bit enables the output of the DRM DIP.

Value	Name
1b	DRM DIP enable
0b	DRM DIP disable

Programming Notes
This needs to be enabled with HDMI only.

27 PSR PSR2 VSC bit 7

Access:	R/W

This bit manually sets PSR VSC bit for future specification changes.

Value	Name
0b	Do not set
1b	Set

26:25 VSC select

Access:	R/W

Select between hardware and software control of the VSC DIP data and header. When hardware controls it will send PSR1 header and data values when PSR1 is enabled, and PSR2 + Y-coordinate header and data values when PSR2 is enabled.
If PSR2/SU SDP without Y-coordinate is enabled SW must set the header bits of the VSC packet to the PSR2 without Y-coordinate value from the eDP standard.

Value	Name	Description
00b	Header and Data	Hardware controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+. Recommended for use when PSR is enabled and software is not using VSC for other types of data.
10b	Data Only	Software controls all headers bytes. Hardware controls data bytes 0-13. Software controls data bytes 14+.

VIDEO_DIP_CTL

		Recommended for use when software is sending data with VSC. If PSR is enabled, software must configure the header to include the PSR revision and byte count.
11b	None	Software controls all headers bytes. Software controls all data bytes. Not recommended for use.

24 VDIP Enable PPS

Access:	Double Buffered

Description
This field controls enable/disable of PPS DIP. It should be enabled prior to enabling VDSC. SW should enable DSC hardware feature only after programming PPS. Hardware still sends PPS once at the beginning of enable cycle in disable PPS case. PPS DIP can only be enabled with DisplayPort.
This bit should be set all the time for DP v2.0 use case. However, on the fly PPS changes are not supported.

Value	Name
0b	Disable
1b	Enable

23 Adaptive Sync SDP Enable

Access:	Double Buffered

This is adaptive sync SDP enable bit. This bit is double buffered at VRR DB update point.
TRANS_VRR_VSYNC must be configured to set the adaptive sync SDP position before enabling.

Value	Name
0b	Disable
1b	Enable

22 Reserved

Access:	R/W

21 Reserved

Access:	RO
Format:	MBZ

VIDEO_DIP_CTL

20	**VDIP Enable VSC** Access: Double Buffered This bit enables the output of the Video Stream Configuration DIP. **Value** / **Name** 0b / Disable VSC DIP 1b / Enable VSC DIP **Restriction** VSC can only be enabled with DisplayPort. VSC should be enabled prior to enabling PSR or stereo 3D if VSC will be used to transmit stereo 3D related information.
19:17	**Reserved** Access: RO Format: MBZ
16	**VDIP Enable GCP** Access: Double Buffered This bit enables the output of the General Control Packet (GCP) DIP.GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore there is a VIDEO_DIP_GCP register instead of DIP data buffers for GCP. **Value** / **Name** 0b / Disable GCP DIP 1b / Enable GCP DIP **Restriction** GCP is only supported with HDMI when the bits per color is not equal to 8. GCP must be enabled prior to enabling TRANS_DDI_FUNC_CTL for HDMI with bits per color not equal to 8 and disabled after disabling TRANS_DDI_FUNC_CTL
15:13	**Reserved** Access: RO Format: MBZ
12	**VDIP Enable AVI** Access: Double Buffered This bit enables the output of the Auxiliary Video Information DIP. **Value** / **Name** 0b / Disable AVI DIP 1b / Enable AVI DIP **Restriction** Only enable with HDMI.

VIDEO_DIP_CTL

11:9 Reserved

Access:	RO
Format:	MBZ

8 VDIP Enable VS

Access:	Double Buffered

This bit enables the output of the Vendor Specific (VS) DIP.

Value	Name
0b	Disable VS DIP
1b	Enable VS DIP

Restriction
Only enable with HDMI.

7:5 Reserved

Access:	RO
Format:	MBZ

4 VDIP Enable GMP

Access:	Double Buffered

Description
This bit enables the output of the Gamut Metadata Packet (GMP) DIP.GMP can be enabled with either DisplayPort or HDMI.
Enable GMP bit is double buffered when GMP double buffer disable (bit [29] of this register) is not set.

Value	Name
0b	Disable GMP DIP
1b	Enable GMP DIP

3:1 Reserved

Access:	RO
Format:	MBZ

0 VDIP Enable SPD

Access:	Double Buffered

This bit enables the output of the Source Product Description (SPD) DIP.

Value	Name
0b	Disable SPD DIP
1b	Enable SPD DIP

Restriction

VIDEO_DIP_CTL		
		Only enable with HDMI.

VIDEO_DIP_DATA

VIDEO_DIP_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60220h-60223h
Name:	Transcoder Video Data Island Packet AVI Data 0
ShortName:	VIDEO_DIP_AVI_DATA_0_A
Reset:	soft
Address:	60224h-60227h
Name:	Transcoder Video Data Island Packet AVI Data 1
ShortName:	VIDEO_DIP_AVI_DATA_1_A
Reset:	soft
Address:	60228h-6022Bh
Name:	Transcoder Video Data Island Packet AVI Data 2
ShortName:	VIDEO_DIP_AVI_DATA_2_A
Reset:	soft
Address:	6022Ch-6022Fh
Name:	Transcoder Video Data Island Packet AVI Data 3
ShortName:	VIDEO_DIP_AVI_DATA_3_A
Reset:	soft
Address:	60230h-60233h
Name:	Transcoder Video Data Island Packet AVI Data 4
ShortName:	VIDEO_DIP_AVI_DATA_4_A
Reset:	soft
Address:	60234h-60237h
Name:	Transcoder Video Data Island Packet AVI Data 5
ShortName:	VIDEO_DIP_AVI_DATA_5_A
Reset:	soft
Address:	60238h-6023Bh
Name:	Transcoder Video Data Island Packet AVI Data 6
ShortName:	VIDEO_DIP_AVI_DATA_6_A
Reset:	soft
Address:	6023Ch-6023Fh
Name:	Transcoder Video Data Island Packet AVI Data 7

VIDEO_DIP_DATA	
ShortName:	VIDEO_DIP_AVI_DATA_7_A
Reset:	soft
Address:	60260h-60263h
Name:	Transcoder Video Data Island Packet VS Data 0
ShortName:	VIDEO_DIP_VS_DATA_0_A
Reset:	soft
Address:	60264h-60267h
Name:	Transcoder Video Data Island Packet VS Data 1
ShortName:	VIDEO_DIP_VS_DATA_1_A
Reset:	soft
Address:	60268h-6026Bh
Name:	Transcoder Video Data Island Packet VS Data 2
ShortName:	VIDEO_DIP_VS_DATA_2_A
Reset:	soft
Address:	6026Ch-6026Fh
Name:	Transcoder Video Data Island Packet VS Data 3
ShortName:	VIDEO_DIP_VS_DATA_3_A
Reset:	soft
Address:	60270h-60273h
Name:	Transcoder Video Data Island Packet VS Data 4
ShortName:	VIDEO_DIP_VS_DATA_4_A
Reset:	soft
Address:	60274h-60277h
Name:	Transcoder Video Data Island Packet VS Data 5
ShortName:	VIDEO_DIP_VS_DATA_5_A
Reset:	soft
Address:	60278h-6027Bh
Name:	Transcoder Video Data Island Packet VS Data 6
ShortName:	VIDEO_DIP_VS_DATA_6_A
Reset:	soft
Address:	6027Ch-6027Fh
Name:	Transcoder Video Data Island Packet VS Data 7
ShortName:	VIDEO_DIP_VS_DATA_7_A
Reset:	soft
Address:	602A0h-602A3h
Name:	Transcoder Video Data Island Packet SPD Data 0

VIDEO_DIP_DATA	
ShortName:	VIDEO_DIP_SPD_DATA_0_A
Reset:	soft
Address:	602A4h-602A7h
Name:	Transcoder Video Data Island Packet SPD Data 1
ShortName:	VIDEO_DIP_SPD_DATA_1_A
Reset:	soft
Address:	602A8h-602ABh
Name:	Transcoder Video Data Island Packet SPD Data 2
ShortName:	VIDEO_DIP_SPD_DATA_2_A
Reset:	soft
Address:	602ACh-602AFh
Name:	Transcoder Video Data Island Packet SPD Data 3
ShortName:	VIDEO_DIP_SPD_DATA_3_A
Reset:	soft
Address:	602B0h-602B3h
Name:	Transcoder Video Data Island Packet SPD Data 4
ShortName:	VIDEO_DIP_SPD_DATA_4_A
Reset:	soft
Address:	602B4h-602B7h
Name:	Transcoder Video Data Island Packet SPD Data 5
ShortName:	VIDEO_DIP_SPD_DATA_5_A
Reset:	soft
Address:	602B8h-602BBh
Name:	Transcoder Video Data Island Packet SPD Data 6
ShortName:	VIDEO_DIP_SPD_DATA_6_A
Reset:	soft
Address:	602BCh-602BFh
Name:	Transcoder Video Data Island Packet SPD Data 7
ShortName:	VIDEO_DIP_SPD_DATA_7_A
Reset:	soft
Address:	602E0h-602E3h
Name:	Transcoder Video Data Island Packet GMP Data 0
ShortName:	VIDEO_DIP_GMP_DATA_0_A
Reset:	soft
Address:	602E4h-602E7h
Name:	Transcoder Video Data Island Packet GMP Data 1

VIDEO_DIP_DATA	
ShortName:	VIDEO_DIP_GMP_DATA_1_A
Reset:	soft
Address:	602E8h-602EBh
Name:	Transcoder Video Data Island Packet GMP Data 2
ShortName:	VIDEO_DIP_GMP_DATA_2_A
Reset:	soft
Address:	602ECh-602EFh
Name:	Transcoder Video Data Island Packet GMP Data 3
ShortName:	VIDEO_DIP_GMP_DATA_3_A
Reset:	soft
Address:	602F0h-602F3h
Name:	Transcoder Video Data Island Packet GMP Data 4
ShortName:	VIDEO_DIP_GMP_DATA_4_A
Reset:	soft
Address:	602F4h-602F7h
Name:	Transcoder Video Data Island Packet GMP Data 5
ShortName:	VIDEO_DIP_GMP_DATA_5_A
Reset:	soft
Address:	602F8h-602FBh
Name:	Transcoder Video Data Island Packet GMP Data 6
ShortName:	VIDEO_DIP_GMP_DATA_6_A
Reset:	soft
Address:	602FCh-602FFh
Name:	Transcoder Video Data Island Packet GMP Data 7
ShortName:	VIDEO_DIP_GMP_DATA_7_A
Reset:	soft
Address:	60300h-60303h
Name:	Transcoder Video Data Island Packet GMP Data 8
ShortName:	VIDEO_DIP_GMP_DATA_8_A
Reset:	soft
Address:	60320h-60323h
Name:	Transcoder Video Data Island Packet VSC Data 0
ShortName:	VIDEO_DIP_VSC_DATA_0_A
Reset:	soft
Address:	60324h-60327h
Name:	Transcoder Video Data Island Packet VSC Data 1

VIDEO_DIP_DATA	
ShortName:	VIDEO_DIP_VSC_DATA_1_A
Reset:	soft
Address:	60328h-6032Bh
Name:	Transcoder Video Data Island Packet VSC Data 2
ShortName:	VIDEO_DIP_VSC_DATA_2_A
Reset:	soft
Address:	6032Ch-6032Fh
Name:	Transcoder Video Data Island Packet VSC Data 3
ShortName:	VIDEO_DIP_VSC_DATA_3_A
Reset:	soft
Address:	60330h-60333h
Name:	Transcoder Video Data Island Packet VSC Data 4
ShortName:	VIDEO_DIP_VSC_DATA_4_A
Reset:	soft
Address:	60334h-60337h
Name:	Transcoder Video Data Island Packet VSC Data 5
ShortName:	VIDEO_DIP_VSC_DATA_5_A
Reset:	soft
Address:	60338h-6033Bh
Name:	Transcoder Video Data Island Packet VSC Data 6
ShortName:	VIDEO_DIP_VSC_DATA_6_A
Reset:	soft
Address:	6033Ch-6033Fh
Name:	Transcoder Video Data Island Packet VSC Data 7
ShortName:	VIDEO_DIP_VSC_DATA_7_A
Reset:	soft
Address:	60340h-60343h
Name:	Transcoder Video Data Island Packet VSC Data 8
ShortName:	VIDEO_DIP_VSC_DATA_8_A
Reset:	soft
Address:	60484h-60487h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 0
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_0_A
Reset:	soft
Address:	60488h-6048Bh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 1

VIDEO_DIP_DATA	
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_1_A
Reset:	soft
Address:	6048Ch-6048Fh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 2
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_2_A
Reset:	soft
Address:	60490h-60493h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 3
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_3_A
Reset:	soft
Address:	60494h-60497h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 4
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_4_A
Reset:	soft
Address:	60498h-6049Bh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 5
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_5_A
Reset:	soft
Address:	6049Ch-6049Fh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 6
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_6_A
Reset:	soft
Address:	604A0h-604A3h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 7
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_7_A
Reset:	soft
Address:	604A4h-604A7h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 8
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_8_A
Reset:	soft
Address:	61220h-61223h
Name:	Transcoder Video Data Island Packet AVI Data 0
ShortName:	VIDEO_DIP_AVI_DATA_0_B
Reset:	soft

Address:	61224h-61227h
Name:	Transcoder Video Data Island Packet AVI Data 1
ShortName:	VIDEO_DIP_AVI_DATA_1_B
Reset:	soft
Address:	61228h-6122Bh
Name:	Transcoder Video Data Island Packet AVI Data 2
ShortName:	VIDEO_DIP_AVI_DATA_2_B
Reset:	soft
Address:	6122Ch-6122Fh
Name:	Transcoder Video Data Island Packet AVI Data 3
ShortName:	VIDEO_DIP_AVI_DATA_3_B
Reset:	soft
Address:	61230h-61233h
Name:	Transcoder Video Data Island Packet AVI Data 4
ShortName:	VIDEO_DIP_AVI_DATA_4_B
Reset:	soft
Address:	61234h-61237h
Name:	Transcoder Video Data Island Packet AVI Data 5
ShortName:	VIDEO_DIP_AVI_DATA_5_B
Reset:	soft
Address:	61238h-6123Bh
Name:	Transcoder Video Data Island Packet AVI Data 6
ShortName:	VIDEO_DIP_AVI_DATA_6_B
Reset:	soft
Address:	6123Ch-6123Fh
Name:	Transcoder Video Data Island Packet AVI Data 7
ShortName:	VIDEO_DIP_AVI_DATA_7_B
Reset:	soft
Address:	61260h-61263h
Name:	Transcoder Video Data Island Packet VS Data 0
ShortName:	VIDEO_DIP_VS_DATA_0_B
Reset:	soft
Address:	61264h-61267h
Name:	Transcoder Video Data Island Packet VS Data 1
ShortName:	VIDEO_DIP_VS_DATA_1_B
Reset:	soft

Address:	61268h-6126Bh
Name:	Transcoder Video Data Island Packet VS Data 2
ShortName:	VIDEO_DIP_VS_DATA_2_B
Reset:	soft
Address:	6126Ch-6126Fh
Name:	Transcoder Video Data Island Packet VS Data 3
ShortName:	VIDEO_DIP_VS_DATA_3_B
Reset:	soft
Address:	61270h-61273h
Name:	Transcoder Video Data Island Packet VS Data 4
ShortName:	VIDEO_DIP_VS_DATA_4_B
Reset:	soft
Address:	61274h-61277h
Name:	Transcoder Video Data Island Packet VS Data 5
ShortName:	VIDEO_DIP_VS_DATA_5_B
Reset:	soft
Address:	61278h-6127Bh
Name:	Transcoder Video Data Island Packet VS Data 6
ShortName:	VIDEO_DIP_VS_DATA_6_B
Reset:	soft
Address:	6127Ch-6127Fh
Name:	Transcoder Video Data Island Packet VS Data 7
ShortName:	VIDEO_DIP_VS_DATA_7_B
Reset:	soft
Address:	612A0h-612A3h
Name:	Transcoder Video Data Island Packet SPD Data 0
ShortName:	VIDEO_DIP_SPD_DATA_0_B
Reset:	soft
Address:	612A4h-612A7h
Name:	Transcoder Video Data Island Packet SPD Data 1
ShortName:	VIDEO_DIP_SPD_DATA_1_B
Reset:	soft
Address:	612A8h-612ABh
Name:	Transcoder Video Data Island Packet SPD Data 2
ShortName:	VIDEO_DIP_SPD_DATA_2_B
Reset:	soft
Address:	612ACh-612AFh

Name:	Transcoder Video Data Island Packet SPD Data 3
ShortName:	VIDEO_DIP_SPD_DATA_3_B
Reset:	soft
Address:	612B0h-612B3h
Name:	Transcoder Video Data Island Packet SPD Data 4
ShortName:	VIDEO_DIP_SPD_DATA_4_B
Reset:	soft
Address:	612B4h-612B7h
Name:	Transcoder Video Data Island Packet SPD Data 5
ShortName:	VIDEO_DIP_SPD_DATA_5_B
Reset:	soft
Address:	612B8h-612BBh
Name:	Transcoder Video Data Island Packet SPD Data 6
ShortName:	VIDEO_DIP_SPD_DATA_6_B
Reset:	soft
Address:	612BCh-612BFh
Name:	Transcoder Video Data Island Packet SPD Data 7
ShortName:	VIDEO_DIP_SPD_DATA_7_B
Reset:	soft
Address:	612E0h-612E3h
Name:	Transcoder Video Data Island Packet GMP Data 0
ShortName:	VIDEO_DIP_GMP_DATA_0_B
Reset:	soft
Address:	612E4h-612E7h
Name:	Transcoder Video Data Island Packet GMP Data 1
ShortName:	VIDEO_DIP_GMP_DATA_1_B
Reset:	soft
Address:	612E8h-612EBh
Name:	Transcoder Video Data Island Packet GMP Data 2
ShortName:	VIDEO_DIP_GMP_DATA_2_B
Reset:	soft
Address:	612ECh-612EFh
Name:	Transcoder Video Data Island Packet GMP Data 3
ShortName:	VIDEO_DIP_GMP_DATA_3_B
Reset:	soft
Address:	612F0h-612F3h
Name:	Transcoder Video Data Island Packet GMP Data 4

ShortName:	VIDEO_DIP_GMP_DATA_4_B
Reset:	soft
Address:	612F4h-612F7h
Name:	Transcoder Video Data Island Packet GMP Data 5
ShortName:	VIDEO_DIP_GMP_DATA_5_B
Reset:	soft
Address:	612F8h-612FBh
Name:	Transcoder Video Data Island Packet GMP Data 6
ShortName:	VIDEO_DIP_GMP_DATA_6_B
Reset:	soft
Address:	612FCh-612FFh
Name:	Transcoder Video Data Island Packet GMP Data 7
ShortName:	VIDEO_DIP_GMP_DATA_7_B
Reset:	soft
Address:	61300h-61303h
Name:	Transcoder Video Data Island Packet GMP Data 8
ShortName:	VIDEO_DIP_GMP_DATA_8_B
Reset:	soft
Address:	61320h-61323h
Name:	Transcoder Video Data Island Packet VSC Data 0
ShortName:	VIDEO_DIP_VSC_DATA_0_B
Reset:	soft
Address:	61324h-61327h
Name:	Transcoder Video Data Island Packet VSC Data 1
ShortName:	VIDEO_DIP_VSC_DATA_1_B
Reset:	soft
Address:	61328h-6132Bh
Name:	Transcoder Video Data Island Packet VSC Data 2
ShortName:	VIDEO_DIP_VSC_DATA_2_B
Reset:	soft
Address:	6132Ch-6132Fh
Name:	Transcoder Video Data Island Packet VSC Data 3
ShortName:	VIDEO_DIP_VSC_DATA_3_B
Reset:	soft
Address:	61330h-61333h
Name:	Transcoder Video Data Island Packet VSC Data 4
ShortName:	VIDEO_DIP_VSC_DATA_4_B

Reset:	soft
Address:	61334h-61337h
Name:	Transcoder Video Data Island Packet VSC Data 5
ShortName:	VIDEO_DIP_VSC_DATA_5_B
Reset:	soft
Address:	61338h-6133Bh
Name:	Transcoder Video Data Island Packet VSC Data 6
ShortName:	VIDEO_DIP_VSC_DATA_6_B
Reset:	soft
Address:	6133Ch-6133Fh
Name:	Transcoder Video Data Island Packet VSC Data 7
ShortName:	VIDEO_DIP_VSC_DATA_7_B
Reset:	soft
Address:	61340h-61343h
Name:	Transcoder Video Data Island Packet VSC Data 8
ShortName:	VIDEO_DIP_VSC_DATA_8_B
Reset:	soft
Address:	61484h-61487h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 0
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_0_B
Reset:	soft
Address:	61488h-6148Bh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 1
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_1_B
Reset:	soft
Address:	6148Ch-6148Fh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 2
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_2_B
Reset:	soft
Address:	61490h-61493h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 3
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_3_B
Reset:	soft
Address:	61494h-61497h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 4
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_4_B
Reset:	soft

Address:	61498h-6149Bh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 5
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_5_B
Reset:	soft
Address:	6149Ch-6149Fh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 6
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_6_B
Reset:	soft
Address:	614A0h-614A3h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 7
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_7_B
Reset:	soft
Address:	614A4h-614A7h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 8
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_8_B
Reset:	soft
Address:	62220h-62223h
Name:	Transcoder Video Data Island Packet AVI Data 0
ShortName:	VIDEO_DIP_AVI_DATA_0_C
Reset:	soft
Address:	62224h-62227h
Name:	Transcoder Video Data Island Packet AVI Data 1
ShortName:	VIDEO_DIP_AVI_DATA_1_C
Reset:	soft
Address:	62228h-6222Bh
Name:	Transcoder Video Data Island Packet AVI Data 2
ShortName:	VIDEO_DIP_AVI_DATA_2_C
Reset:	soft
Address:	6222Ch-6222Fh
Name:	Transcoder Video Data Island Packet AVI Data 3
ShortName:	VIDEO_DIP_AVI_DATA_3_C
Reset:	soft
Address:	62230h-62233h
Name:	Transcoder Video Data Island Packet AVI Data 4
ShortName:	VIDEO_DIP_AVI_DATA_4_C
Reset:	soft
Address:	62234h-62237h

Name:	Transcoder Video Data Island Packet AVI Data 5
ShortName:	VIDEO_DIP_AVI_DATA_5_C
Reset:	soft
Address:	62238h-6223Bh
Name:	Transcoder Video Data Island Packet AVI Data 6
ShortName:	VIDEO_DIP_AVI_DATA_6_C
Reset:	soft
Address:	6223Ch-6223Fh
Name:	Transcoder Video Data Island Packet AVI Data 7
ShortName:	VIDEO_DIP_AVI_DATA_7_C
Reset:	soft
Address:	62260h-62263h
Name:	Transcoder Video Data Island Packet VS Data 0
ShortName:	VIDEO_DIP_VS_DATA_0_C
Reset:	soft
Address:	62264h-62267h
Name:	Transcoder Video Data Island Packet VS Data 1
ShortName:	VIDEO_DIP_VS_DATA_1_C
Reset:	soft
Address:	62268h-6226Bh
Name:	Transcoder Video Data Island Packet VS Data 2
ShortName:	VIDEO_DIP_VS_DATA_2_C
Reset:	soft
Address:	6226Ch-6226Fh
Name:	Transcoder Video Data Island Packet VS Data 3
ShortName:	VIDEO_DIP_VS_DATA_3_C
Reset:	soft
Address:	62270h-62273h
Name:	Transcoder Video Data Island Packet VS Data 4
ShortName:	VIDEO_DIP_VS_DATA_4_C
Reset:	soft
Address:	62274h-62277h
Name:	Transcoder Video Data Island Packet VS Data 5
ShortName:	VIDEO_DIP_VS_DATA_5_C
Reset:	soft
Address:	62278h-6227Bh
Name:	Transcoder Video Data Island Packet VS Data 6

ShortName:	VIDEO_DIP_VS_DATA_6_C
Reset:	soft
Address:	6227Ch-6227Fh
Name:	Transcoder Video Data Island Packet VS Data 7
ShortName:	VIDEO_DIP_VS_DATA_7_C
Reset:	soft
Address:	622A0h-622A3h
Name:	Transcoder Video Data Island Packet SPD Data 0
ShortName:	VIDEO_DIP_SPD_DATA_0_C
Reset:	soft
Address:	622A4h-622A7h
Name:	Transcoder Video Data Island Packet SPD Data 1
ShortName:	VIDEO_DIP_SPD_DATA_1_C
Reset:	soft
Address:	622A8h-622ABh
Name:	Transcoder Video Data Island Packet SPD Data 2
ShortName:	VIDEO_DIP_SPD_DATA_2_C
Reset:	soft
Address:	622ACh-622AFh
Name:	Transcoder Video Data Island Packet SPD Data 3
ShortName:	VIDEO_DIP_SPD_DATA_3_C
Reset:	soft
Address:	622B0h-622B3h
Name:	Transcoder Video Data Island Packet SPD Data 4
ShortName:	VIDEO_DIP_SPD_DATA_4_C
Reset:	soft
Address:	622B4h-622B7h
Name:	Transcoder Video Data Island Packet SPD Data 5
ShortName:	VIDEO_DIP_SPD_DATA_5_C
Reset:	soft
Address:	622B8h-622BBh
Name:	Transcoder Video Data Island Packet SPD Data 6
ShortName:	VIDEO_DIP_SPD_DATA_6_C
Reset:	soft
Address:	622BCh-622BFh
Name:	Transcoder Video Data Island Packet SPD Data 7
ShortName:	VIDEO_DIP_SPD_DATA_7_C

Reset:	soft
Address:	622E0h-622E3h
Name:	Transcoder Video Data Island Packet GMP Data 0
ShortName:	VIDEO_DIP_GMP_DATA_0_C
Reset:	soft
Address:	622E4h-622E7h
Name:	Transcoder Video Data Island Packet GMP Data 1
ShortName:	VIDEO_DIP_GMP_DATA_1_C
Reset:	soft
Address:	622E8h-622EBh
Name:	Transcoder Video Data Island Packet GMP Data 2
ShortName:	VIDEO_DIP_GMP_DATA_2_C
Reset:	soft
Address:	622ECh-622EFh
Name:	Transcoder Video Data Island Packet GMP Data 3
ShortName:	VIDEO_DIP_GMP_DATA_3_C
Reset:	soft
Address:	622F0h-622F3h
Name:	Transcoder Video Data Island Packet GMP Data 4
ShortName:	VIDEO_DIP_GMP_DATA_4_C
Reset:	soft
Address:	622F4h-622F7h
Name:	Transcoder Video Data Island Packet GMP Data 5
ShortName:	VIDEO_DIP_GMP_DATA_5_C
Reset:	soft
Address:	622F8h-622FBh
Name:	Transcoder Video Data Island Packet GMP Data 6
ShortName:	VIDEO_DIP_GMP_DATA_6_C
Reset:	soft
Address:	622FCh-622FFh
Name:	Transcoder Video Data Island Packet GMP Data 7
ShortName:	VIDEO_DIP_GMP_DATA_7_C
Reset:	soft
Address:	62300h-62303h
Name:	Transcoder Video Data Island Packet GMP Data 8
ShortName:	VIDEO_DIP_GMP_DATA_8_C
Reset:	soft

Address:	62320h-62323h
Name:	Transcoder Video Data Island Packet VSC Data 0
ShortName:	VIDEO_DIP_VSC_DATA_0_C
Reset:	soft
Address:	62324h-62327h
Name:	Transcoder Video Data Island Packet VSC Data 1
ShortName:	VIDEO_DIP_VSC_DATA_1_C
Reset:	soft
Address:	62328h-6232Bh
Name:	Transcoder Video Data Island Packet VSC Data 2
ShortName:	VIDEO_DIP_VSC_DATA_2_C
Reset:	soft
Address:	6232Ch-6232Fh
Name:	Transcoder Video Data Island Packet VSC Data 3
ShortName:	VIDEO_DIP_VSC_DATA_3_C
Reset:	soft
Address:	62330h-62333h
Name:	Transcoder Video Data Island Packet VSC Data 4
ShortName:	VIDEO_DIP_VSC_DATA_4_C
Reset:	soft
Address:	62334h-62337h
Name:	Transcoder Video Data Island Packet VSC Data 5
ShortName:	VIDEO_DIP_VSC_DATA_5_C
Reset:	soft
Address:	62338h-6233Bh
Name:	Transcoder Video Data Island Packet VSC Data 6
ShortName:	VIDEO_DIP_VSC_DATA_6_C
Reset:	soft
Address:	6233Ch-6233Fh
Name:	Transcoder Video Data Island Packet VSC Data 7
ShortName:	VIDEO_DIP_VSC_DATA_7_C
Reset:	soft
Address:	62340h-62343h
Name:	Transcoder Video Data Island Packet VSC Data 8
ShortName:	VIDEO_DIP_VSC_DATA_8_C
Reset:	soft
Address:	62484h-62487h

Name:	Transcoder Video Data Island Packet Adaptive Sync Data 0
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_0_C
Reset:	soft
Address:	62488h-6248Bh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 1
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_1_C
Reset:	soft
Address:	6248Ch-6248Fh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 2
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_2_C
Reset:	soft
Address:	62490h-62493h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 3
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_3_C
Reset:	soft
Address:	62494h-62497h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 4
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_4_C
Reset:	soft
Address:	62498h-6249Bh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 5
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_5_C
Reset:	soft
Address:	6249Ch-6249Fh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 6
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_6_C
Reset:	soft
Address:	624A0h-624A3h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 7
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_7_C
Reset:	soft
Address:	624A4h-624A7h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 8
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_8_C
Reset:	soft

Address:	63220h-63223h
Name:	Transcoder Video Data Island Packet AVI Data 0
ShortName:	VIDEO_DIP_AVI_DATA_0_D
Reset:	soft
Address:	63224h-63227h
Name:	Transcoder Video Data Island Packet AVI Data 1
ShortName:	VIDEO_DIP_AVI_DATA_1_D
Reset:	soft
Address:	63228h-6322Bh
Name:	Transcoder Video Data Island Packet AVI Data 2
ShortName:	VIDEO_DIP_AVI_DATA_2_D
Reset:	soft
Address:	6322Ch-6322Fh
Name:	Transcoder Video Data Island Packet AVI Data 3
ShortName:	VIDEO_DIP_AVI_DATA_3_D
Reset:	soft
Address:	63230h-63233h
Name:	Transcoder Video Data Island Packet AVI Data 4
ShortName:	VIDEO_DIP_AVI_DATA_4_D
Reset:	soft
Address:	63234h-63237h
Name:	Transcoder Video Data Island Packet AVI Data 5
ShortName:	VIDEO_DIP_AVI_DATA_5_D
Reset:	soft
Address:	63238h-6323Bh
Name:	Transcoder Video Data Island Packet AVI Data 6
ShortName:	VIDEO_DIP_AVI_DATA_6_D
Reset:	soft
Address:	6323Ch-6323Fh
Name:	Transcoder Video Data Island Packet AVI Data 7
ShortName:	VIDEO_DIP_AVI_DATA_7_D
Reset:	soft
Address:	63260h-63263h
Name:	Transcoder Video Data Island Packet VS Data 0
ShortName:	VIDEO_DIP_VS_DATA_0_D
Reset:	soft

Address:	63264h-63267h
Name:	Transcoder Video Data Island Packet VS Data 1
ShortName:	VIDEO_DIP_VS_DATA_1_D
Reset:	soft
Address:	63268h-6326Bh
Name:	Transcoder Video Data Island Packet VS Data 2
ShortName:	VIDEO_DIP_VS_DATA_2_D
Reset:	soft
Address:	6326Ch-6326Fh
Name:	Transcoder Video Data Island Packet VS Data 3
ShortName:	VIDEO_DIP_VS_DATA_3_D
Reset:	soft
Address:	63270h-63273h
Name:	Transcoder Video Data Island Packet VS Data 4
ShortName:	VIDEO_DIP_VS_DATA_4_D
Reset:	soft
Address:	63274h-63277h
Name:	Transcoder Video Data Island Packet VS Data 5
ShortName:	VIDEO_DIP_VS_DATA_5_D
Reset:	soft
Address:	63278h-6327Bh
Name:	Transcoder Video Data Island Packet VS Data 6
ShortName:	VIDEO_DIP_VS_DATA_6_D
Reset:	soft
Address:	6327Ch-6327Fh
Name:	Transcoder Video Data Island Packet VS Data 7
ShortName:	VIDEO_DIP_VS_DATA_7_D
Reset:	soft
Address:	632A0h-632A3h
Name:	Transcoder Video Data Island Packet SPD Data 0
ShortName:	VIDEO_DIP_SPD_DATA_0_D
Reset:	soft
Address:	632A4h-632A7h
Name:	Transcoder Video Data Island Packet SPD Data 1
ShortName:	VIDEO_DIP_SPD_DATA_1_D
Reset:	soft
Address:	632A8h-632ABh

Name:	Transcoder Video Data Island Packet SPD Data 2
ShortName:	VIDEO_DIP_SPD_DATA_2_D
Reset:	soft
Address:	632ACh-632AFh
Name:	Transcoder Video Data Island Packet SPD Data 3
ShortName:	VIDEO_DIP_SPD_DATA_3_D
Reset:	soft
Address:	632B0h-632B3h
Name:	Transcoder Video Data Island Packet SPD Data 4
ShortName:	VIDEO_DIP_SPD_DATA_4_D
Reset:	soft
Address:	632B4h-632B7h
Name:	Transcoder Video Data Island Packet SPD Data 5
ShortName:	VIDEO_DIP_SPD_DATA_5_D
Reset:	soft
Address:	632B8h-632BBh
Name:	Transcoder Video Data Island Packet SPD Data 6
ShortName:	VIDEO_DIP_SPD_DATA_6_D
Reset:	soft
Address:	632BCh-632BFh
Name:	Transcoder Video Data Island Packet SPD Data 7
ShortName:	VIDEO_DIP_SPD_DATA_7_D
Reset:	soft
Address:	632E0h-632E3h
Name:	Transcoder Video Data Island Packet GMP Data 0
ShortName:	VIDEO_DIP_GMP_DATA_0_D
Reset:	soft
Address:	632E4h-632E7h
Name:	Transcoder Video Data Island Packet GMP Data 1
ShortName:	VIDEO_DIP_GMP_DATA_1_D
Reset:	soft
Address:	632E8h-632EBh
Name:	Transcoder Video Data Island Packet GMP Data 2
ShortName:	VIDEO_DIP_GMP_DATA_2_D
Reset:	soft
Address:	632ECh-632EFh
Name:	Transcoder Video Data Island Packet GMP Data 3

ShortName:	VIDEO_DIP_GMP_DATA_3_D
Reset:	soft
Address:	632F0h-632F3h
Name:	Transcoder Video Data Island Packet GMP Data 4
ShortName:	VIDEO_DIP_GMP_DATA_4_D
Reset:	soft
Address:	632F4h-632F7h
Name:	Transcoder Video Data Island Packet GMP Data 5
ShortName:	VIDEO_DIP_GMP_DATA_5_D
Reset:	soft
Address:	632F8h-632FBh
Name:	Transcoder Video Data Island Packet GMP Data 6
ShortName:	VIDEO_DIP_GMP_DATA_6_D
Reset:	soft
Address:	632FCh-632FFh
Name:	Transcoder Video Data Island Packet GMP Data 7
ShortName:	VIDEO_DIP_GMP_DATA_7_D
Reset:	soft
Address:	63300h-63303h
Name:	Transcoder Video Data Island Packet GMP Data 8
ShortName:	VIDEO_DIP_GMP_DATA_8_D
Reset:	soft
Address:	63320h-63323h
Name:	Transcoder Video Data Island Packet VSC Data 0
ShortName:	VIDEO_DIP_VSC_DATA_0_D
Reset:	soft
Address:	63324h-63327h
Name:	Transcoder Video Data Island Packet VSC Data 1
ShortName:	VIDEO_DIP_VSC_DATA_1_D
Reset:	soft
Address:	63328h-6332Bh
Name:	Transcoder Video Data Island Packet VSC Data 2
ShortName:	VIDEO_DIP_VSC_DATA_2_D
Reset:	soft
Address:	6332Ch-6332Fh
Name:	Transcoder Video Data Island Packet VSC Data 3
ShortName:	VIDEO_DIP_VSC_DATA_3_D

Reset:	soft
Address:	63330h-63333h
Name:	Transcoder Video Data Island Packet VSC Data 4
ShortName:	VIDEO_DIP_VSC_DATA_4_D
Reset:	soft
Address:	63334h-63337h
Name:	Transcoder Video Data Island Packet VSC Data 5
ShortName:	VIDEO_DIP_VSC_DATA_5_D
Reset:	soft
Address:	63338h-6333Bh
Name:	Transcoder Video Data Island Packet VSC Data 6
ShortName:	VIDEO_DIP_VSC_DATA_6_D
Reset:	soft
Address:	6333Ch-6333Fh
Name:	Transcoder Video Data Island Packet VSC Data 7
ShortName:	VIDEO_DIP_VSC_DATA_7_D
Reset:	soft
Address:	63340h-63343h
Name:	Transcoder Video Data Island Packet VSC Data 8
ShortName:	VIDEO_DIP_VSC_DATA_8_D
Reset:	soft
Address:	63484h-63487h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 0
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_0_D
Reset:	soft
Address:	63488h-6348Bh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 1
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_1_D
Reset:	soft
Address:	6348Ch-6348Fh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 2
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_2_D
Reset:	soft
Address:	63490h-63493h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 3
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_3_D
Reset:	soft

Address:	63494h-63497h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 4
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_4_D
Reset:	soft
Address:	63498h-6349Bh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 5
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_5_D
Reset:	soft
Address:	6349Ch-6349Fh
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 6
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_6_D
Reset:	soft
Address:	634A0h-634A3h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 7
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_7_D
Reset:	soft
Address:	634A4h-634A7h
Name:	Transcoder Video Data Island Packet Adaptive Sync Data 8
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_DATA_8_D
Reset:	soft

There are multiple instances of this register format per DIP type and per transcoder.

DWord	Bit	Description
0	31:0	**Video DIP DATA** Access: Double Buffered This field contains the video DIP data to be transmitted. **Restriction** Data should be loaded before enabling the transmission through the DIP type enable bit.

VIDEO_DIP_DRM_DATA

VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60440h-60443h
Name:	Transcoder Video Data Island Packet for DRM 0
ShortName:	VIDEO_DIP_DRM_DATA_0_A
Reset:	soft
Address:	60444h-60447h
Name:	Transcoder Video Data Island Packet for DRM 1
ShortName:	VIDEO_DIP_DRM_DATA_1_A
Reset:	soft
Address:	60448h-6044Bh
Name:	Transcoder Video Data Island Packet for DRM 2
ShortName:	VIDEO_DIP_DRM_DATA_2_A
Reset:	soft
Address:	6044Ch-6044Fh
Name:	Transcoder Video Data Island Packet for DRM 3
ShortName:	VIDEO_DIP_DRM_DATA_3_A
Reset:	soft
Address:	60450h-60453h
Name:	Transcoder Video Data Island Packet for DRM 4
ShortName:	VIDEO_DIP_DRM_DATA_4_A
Reset:	soft
Address:	60454h-60457h
Name:	Transcoder Video Data Island Packet for DRM 5
ShortName:	VIDEO_DIP_DRM_DATA_5_A
Reset:	soft
Address:	60458h-6045Bh
Name:	Transcoder Video Data Island Packet for DRM 6
ShortName:	VIDEO_DIP_DRM_DATA_6_A
Reset:	soft
Address:	6045Ch-6045Fh
Name:	Transcoder Video Data Island Packet for DRM 7

VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA	
ShortName:	VIDEO_DIP_DRM_DATA_7_A
Reset:	soft
Address:	61440h-61443h
Name:	Transcoder Video Data Island Packet for DRM 0
ShortName:	VIDEO_DIP_DRM_DATA_0_B
Reset:	soft
Address:	61444h-61447h
Name:	Transcoder Video Data Island Packet for DRM 1
ShortName:	VIDEO_DIP_DRM_DATA_1_B
Reset:	soft
Address:	61448h-6144Bh
Name:	Transcoder Video Data Island Packet for DRM 2
ShortName:	VIDEO_DIP_DRM_DATA_2_B
Reset:	soft
Address:	6144Ch-6144Fh
Name:	Transcoder Video Data Island Packet for DRM 3
ShortName:	VIDEO_DIP_DRM_DATA_3_B
Reset:	soft
Address:	61450h-61453h
Name:	Transcoder Video Data Island Packet for DRM 4
ShortName:	VIDEO_DIP_DRM_DATA_4_B
Reset:	soft
Address:	61454h-61457h
Name:	Transcoder Video Data Island Packet for DRM 5
ShortName:	VIDEO_DIP_DRM_DATA_5_B
Reset:	soft
Address:	61458h-6145Bh
Name:	Transcoder Video Data Island Packet for DRM 6
ShortName:	VIDEO_DIP_DRM_DATA_6_B
Reset:	soft
Address:	6145Ch-6145Fh
Name:	Transcoder Video Data Island Packet for DRM 7
ShortName:	VIDEO_DIP_DRM_DATA_7_B
Reset:	soft
Address:	62440h-62443h
Name:	Transcoder Video Data Island Packet for DRM 0

VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA	
ShortName:	VIDEO_DIP_DRM_DATA_0_C
Reset:	soft
Address:	62444h-62447h
Name:	Transcoder Video Data Island Packet for DRM 1
ShortName:	VIDEO_DIP_DRM_DATA_1_C
Reset:	soft
Address:	62448h-6244Bh
Name:	Transcoder Video Data Island Packet for DRM 2
ShortName:	VIDEO_DIP_DRM_DATA_2_C
Reset:	soft
Address:	6244Ch-6244Fh
Name:	Transcoder Video Data Island Packet for DRM 3
ShortName:	VIDEO_DIP_DRM_DATA_3_C
Reset:	soft
Address:	62450h-62453h
Name:	Transcoder Video Data Island Packet for DRM 4
ShortName:	VIDEO_DIP_DRM_DATA_4_C
Reset:	soft
Address:	62454h-62457h
Name:	Transcoder Video Data Island Packet for DRM 5
ShortName:	VIDEO_DIP_DRM_DATA_5_C
Reset:	soft
Address:	62458h-6245Bh
Name:	Transcoder Video Data Island Packet for DRM 6
ShortName:	VIDEO_DIP_DRM_DATA_6_C
Reset:	soft
Address:	6245Ch-6245Fh
Name:	Transcoder Video Data Island Packet for DRM 7
ShortName:	VIDEO_DIP_DRM_DATA_7_C
Reset:	soft
Address:	63440h-63443h
Name:	Transcoder Video Data Island Packet for DRM 0
ShortName:	VIDEO_DIP_DRM_DATA_0_D
Reset:	soft
Address:	63444h-63447h
Name:	Transcoder Video Data Island Packet for DRM 1

VIDEO_DIP_DRM_DATA - VIDEO_DIP_DRM_DATA

ShortName:	VIDEO_DIP_DRM_DATA_1_D
Reset:	soft

Address:	63448h-6344Bh
Name:	Transcoder Video Data Island Packet for DRM 2
ShortName:	VIDEO_DIP_DRM_DATA_2_D
Reset:	soft

Address:	6344Ch-6344Fh
Name:	Transcoder Video Data Island Packet for DRM 3
ShortName:	VIDEO_DIP_DRM_DATA_3_D
Reset:	soft

Address:	63450h-63453h
Name:	Transcoder Video Data Island Packet for DRM 4
ShortName:	VIDEO_DIP_DRM_DATA_4_D
Reset:	soft

Address:	63454h-63457h
Name:	Transcoder Video Data Island Packet for DRM 5
ShortName:	VIDEO_DIP_DRM_DATA_5_D
Reset:	soft

Address:	63458h-6345Bh
Name:	Transcoder Video Data Island Packet for DRM 6
ShortName:	VIDEO_DIP_DRM_DATA_6_D
Reset:	soft

Address:	6345Ch-6345Fh
Name:	Transcoder Video Data Island Packet for DRM 7
ShortName:	VIDEO_DIP_DRM_DATA_7_D
Reset:	soft

HDMI 2.0 DRM Infoframe DIP data.

DWord	Bit	Description
0	31:0	**DRM DIP data** Access: Double Buffered

VIDEO_DIP_DRM_ECC

VIDEO_DIP_DRM_ECC - VIDEO_DIP_DRM_ECC	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	60460h-60463h
Name:	Transcoder Video Data Island Packet for DRM ECC 0
ShortName:	VIDEO_DIP_DRM_ECC_0_A
Reset:	soft
Address:	60464h-60467h
Name:	Transcoder Video Data Island Packet for DRM ECC 1
ShortName:	VIDEO_DIP_DRM_ECC_1_A
Reset:	soft
Address:	61460h-61463h
Name:	Transcoder Video Data Island Packet for DRM ECC 0
ShortName:	VIDEO_DIP_DRM_ECC_0_B
Reset:	soft
Address:	61464h-61467h
Name:	Transcoder Video Data Island Packet for DRM ECC 1
ShortName:	VIDEO_DIP_DRM_ECC_1_B
Reset:	soft
Address:	62460h-62463h
Name:	Transcoder Video Data Island Packet for DRM ECC 0
ShortName:	VIDEO_DIP_DRM_ECC_0_C
Reset:	soft
Address:	62464h-62467h
Name:	Transcoder Video Data Island Packet for DRM ECC 1
ShortName:	VIDEO_DIP_DRM_ECC_1_C
Reset:	soft
Address:	63460h-63463h
Name:	Transcoder Video Data Island Packet for DRM ECC 0
ShortName:	VIDEO_DIP_DRM_ECC_0_D
Reset:	soft
Address:	63464h-63467h
Name:	Transcoder Video Data Island Packet for DRM ECC 1

VIDEO_DIP_DRM_ECC - VIDEO_DIP_DRM_ECC

ShortName: VIDEO_DIP_DRM_ECC_1_D

Reset: soft

HDMI 2.0 DRM Infoframe ECC data.

DWord	Bit	Description
0	31:0	**DRM ECC data** Access: RO

VIDEO_DIP_ECC

VIDEO_DIP_ECC	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	60240h-60243h
Name:	Transcoder Video Data Island Packet AVI ECC 0
ShortName:	VIDEO_DIP_AVI_ECC_0_A
Reset:	soft
Address:	60244h-60247h
Name:	Transcoder Video Data Island Packet AVI ECC 1
ShortName:	VIDEO_DIP_AVI_ECC_1_A
Reset:	soft
Address:	60280h-60283h
Name:	Transcoder Video Data Island Packet VS ECC 0
ShortName:	VIDEO_DIP_VS_ECC_0_A
Reset:	soft
Address:	60284h-60287h
Name:	Transcoder Video Data Island Packet VS ECC 1
ShortName:	VIDEO_DIP_VS_ECC_1_A
Reset:	soft
Address:	602C0h-602C3h
Name:	Transcoder Video Data Island Packet SPD ECC 0
ShortName:	VIDEO_DIP_SPD_ECC_0_A
Reset:	soft
Address:	602C4h-602C7h
Name:	Transcoder Video Data Island Packet SPD ECC 1
ShortName:	VIDEO_DIP_SPD_ECC_1_A
Reset:	soft
Address:	602D0h-602D3h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 0
ShortName:	VIDEO_DIP_VSC_ECC_COG2_0_A
Reset:	soft
Address:	602D4h-602D7h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 1

VIDEO_DIP_ECC	
ShortName:	VIDEO_DIP_VSC_ECC_COG2_1_A
Reset:	soft
Address:	602D8h-602DBh
Name:	Transcoder Video Data Island Packet VSC ECC COG2 2
ShortName:	VIDEO_DIP_VSC_ECC_COG2_2_A
Reset:	soft
Address:	60304h-60307h
Name:	Transcoder Video Data Island Packet GMP ECC 0
ShortName:	VIDEO_DIP_GMP_ECC_0_A
Reset:	soft
Address:	60308h-6030Bh
Name:	Transcoder Video Data Island Packet GMP ECC 1
ShortName:	VIDEO_DIP_GMP_ECC_1_A
Reset:	soft
Address:	6030Ch-6030Fh
Name:	Transcoder Video Data Island Packet GMP ECC 2
ShortName:	VIDEO_DIP_GMP_ECC_2_A
Reset:	soft
Address:	60310h-60313h
Name:	Transcoder Video Data Island Packet GMP ECC 3
ShortName:	VIDEO_DIP_GMP_ECC_3_A
Reset:	soft
Address:	60314h-60317h
Name:	Transcoder Video Data Island Packet GMP ECC 4
ShortName:	VIDEO_DIP_GMP_ECC_4_A
Reset:	soft
Address:	60344h-60347h
Name:	Transcoder Video Data Island Packet VSC ECC 0
ShortName:	VIDEO_DIP_VSC_ECC_0_A
Reset:	soft
Address:	60348h-6034Bh
Name:	Transcoder Video Data Island Packet VSC ECC 1
ShortName:	VIDEO_DIP_VSC_ECC_1_A
Reset:	soft
Address:	6034Ch-6034Fh
Name:	Transcoder Video Data Island Packet VSC ECC 2

VIDEO_DIP_ECC	
ShortName:	VIDEO_DIP_VSC_ECC_2_A
Reset:	soft
Address:	604A8h-604ABh
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 0
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_0_A
Reset:	soft
Address:	604ACh-604AFh
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 1
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_1_A
Reset:	soft
Address:	604B0h-604B3h
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 2
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_2_A
Reset:	soft
Address:	61240h-61243h
Name:	Transcoder Video Data Island Packet AVI ECC 0
ShortName:	VIDEO_DIP_AVI_ECC_0_B
Reset:	soft
Address:	61244h-61247h
Name:	Transcoder Video Data Island Packet AVI ECC 1
ShortName:	VIDEO_DIP_AVI_ECC_1_B
Reset:	soft
Address:	61280h-61283h
Name:	Transcoder Video Data Island Packet VS ECC 0
ShortName:	VIDEO_DIP_VS_ECC_0_B
Reset:	soft
Address:	61284h-61287h
Name:	Transcoder Video Data Island Packet VS ECC 1
ShortName:	VIDEO_DIP_VS_ECC_1_B
Reset:	soft
Address:	612C0h-612C3h
Name:	Transcoder Video Data Island Packet SPD ECC 0
ShortName:	VIDEO_DIP_SPD_ECC_0_B
Reset:	soft
Address:	612C4h-612C7h
Name:	Transcoder Video Data Island Packet SPD ECC 1

VIDEO_DIP_ECC	
ShortName:	VIDEO_DIP_SPD_ECC_1_B
Reset:	soft
Address:	612D0h-612D3h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 0
ShortName:	VIDEO_DIP_VSC_ECC_COG2_0_B
Reset:	soft
Address:	612D4h-612D7h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 1
ShortName:	VIDEO_DIP_VSC_ECC_COG2_1_B
Reset:	soft
Address:	612D8h-612DBh
Name:	Transcoder Video Data Island Packet VSC ECC COG2 2
ShortName:	VIDEO_DIP_VSC_ECC_COG2_2_B
Reset:	soft
Address:	61304h-61307h
Name:	Transcoder Video Data Island Packet GMP ECC 0
ShortName:	VIDEO_DIP_GMP_ECC_0_B
Reset:	soft
Address:	61308h-6130Bh
Name:	Transcoder Video Data Island Packet GMP ECC 1
ShortName:	VIDEO_DIP_GMP_ECC_1_B
Reset:	soft
Address:	6130Ch-6130Fh
Name:	Transcoder Video Data Island Packet GMP ECC 2
ShortName:	VIDEO_DIP_GMP_ECC_2_B
Reset:	soft
Address:	61310h-61313h
Name:	Transcoder Video Data Island Packet GMP ECC 3
ShortName:	VIDEO_DIP_GMP_ECC_3_B
Reset:	soft
Address:	61314h-61317h
Name:	Transcoder Video Data Island Packet GMP ECC 4
ShortName:	VIDEO_DIP_GMP_ECC_4_B
Reset:	soft
Address:	61344h-61347h
Name:	Transcoder Video Data Island Packet VSC ECC 0

VIDEO_DIP_ECC	
ShortName:	VIDEO_DIP_VSC_ECC_0_B
Reset:	soft
Address:	61348h-6134Bh
Name:	Transcoder Video Data Island Packet VSC ECC 1
ShortName:	VIDEO_DIP_VSC_ECC_1_B
Reset:	soft
Address:	6134Ch-6134Fh
Name:	Transcoder Video Data Island Packet VSC ECC 2
ShortName:	VIDEO_DIP_VSC_ECC_2_B
Reset:	soft
Address:	614A8h-614ABh
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 0
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_0_B
Reset:	soft
Address:	614ACh-614AFh
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 1
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_1_B
Reset:	soft
Address:	614B0h-614B3h
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 2
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_2_B
Reset:	soft
Address:	62240h-62243h
Name:	Transcoder Video Data Island Packet AVI ECC 0
ShortName:	VIDEO_DIP_AVI_ECC_0_C
Reset:	soft
Address:	62244h-62247h
Name:	Transcoder Video Data Island Packet AVI ECC 1
ShortName:	VIDEO_DIP_AVI_ECC_1_C
Reset:	soft
Address:	62280h-62283h
Name:	Transcoder Video Data Island Packet VS ECC 0
ShortName:	VIDEO_DIP_VS_ECC_0_C
Reset:	soft

Address:	62284h-62287h
Name:	Transcoder Video Data Island Packet VS ECC 1
ShortName:	VIDEO_DIP_VS_ECC_1_C
Reset:	soft
Address:	622C0h-622C3h
Name:	Transcoder Video Data Island Packet SPD ECC 0
ShortName:	VIDEO_DIP_SPD_ECC_0_C
Reset:	soft
Address:	622C4h-622C7h
Name:	Transcoder Video Data Island Packet SPD ECC 1
ShortName:	VIDEO_DIP_SPD_ECC_1_C
Reset:	soft
Address:	622D0h-622D3h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 0
ShortName:	VIDEO_DIP_VSC_ECC_COG2_0_C
Reset:	soft
Address:	622D4h-622D7h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 1
ShortName:	VIDEO_DIP_VSC_ECC_COG2_1_C
Reset:	soft
Address:	622D8h-622DBh
Name:	Transcoder Video Data Island Packet VSC ECC COG2 2
ShortName:	VIDEO_DIP_VSC_ECC_COG2_2_C
Reset:	soft
Address:	62304h-62307h
Name:	Transcoder Video Data Island Packet GMP ECC 0
ShortName:	VIDEO_DIP_GMP_ECC_0_C
Reset:	soft
Address:	62308h-6230Bh
Name:	Transcoder Video Data Island Packet GMP ECC 1
ShortName:	VIDEO_DIP_GMP_ECC_1_C
Reset:	soft
Address:	6230Ch-6230Fh
Name:	Transcoder Video Data Island Packet GMP ECC 2
ShortName:	VIDEO_DIP_GMP_ECC_2_C
Reset:	soft

Address:	62310h-62313h
Name:	Transcoder Video Data Island Packet GMP ECC 3
ShortName:	VIDEO_DIP_GMP_ECC_3_C
Reset:	soft
Address:	62314h-62317h
Name:	Transcoder Video Data Island Packet GMP ECC 4
ShortName:	VIDEO_DIP_GMP_ECC_4_C
Reset:	soft
Address:	62344h-62347h
Name:	Transcoder Video Data Island Packet VSC ECC 0
ShortName:	VIDEO_DIP_VSC_ECC_0_C
Reset:	soft
Address:	62348h-6234Bh
Name:	Transcoder Video Data Island Packet VSC ECC 1
ShortName:	VIDEO_DIP_VSC_ECC_1_C
Reset:	soft
Address:	6234Ch-6234Fh
Name:	Transcoder Video Data Island Packet VSC ECC 2
ShortName:	VIDEO_DIP_VSC_ECC_2_C
Reset:	soft
Address:	624A8h-624ABh
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 0
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_0_C
Reset:	soft
Address:	624ACh-624AFh
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 1
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_1_C
Reset:	soft
Address:	624B0h-624B3h
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 2
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_2_C
Reset:	soft
Address:	63240h-63243h
Name:	Transcoder Video Data Island Packet AVI ECC 0
ShortName:	VIDEO_DIP_AVI_ECC_0_D
Reset:	soft

Address:	63244h-63247h
Name:	Transcoder Video Data Island Packet AVI ECC 1
ShortName:	VIDEO_DIP_AVI_ECC_1_D
Reset:	soft
Address:	63280h-63283h
Name:	Transcoder Video Data Island Packet VS ECC 0
ShortName:	VIDEO_DIP_VS_ECC_0_D
Reset:	soft
Address:	63284h-63287h
Name:	Transcoder Video Data Island Packet VS ECC 1
ShortName:	VIDEO_DIP_VS_ECC_1_D
Reset:	soft
Address:	632C0h-632C3h
Name:	Transcoder Video Data Island Packet SPD ECC 0
ShortName:	VIDEO_DIP_SPD_ECC_0_D
Reset:	soft
Address:	632C4h-632C7h
Name:	Transcoder Video Data Island Packet SPD ECC 1
ShortName:	VIDEO_DIP_SPD_ECC_1_D
Reset:	soft
Address:	632D0h-632D3h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 0
ShortName:	VIDEO_DIP_VSC_ECC_COG2_0_D
Reset:	soft
Address:	632D4h-632D7h
Name:	Transcoder Video Data Island Packet VSC ECC COG2 1
ShortName:	VIDEO_DIP_VSC_ECC_COG2_1_D
Reset:	soft
Address:	632D8h-632DBh
Name:	Transcoder Video Data Island Packet VSC ECC COG2 2
ShortName:	VIDEO_DIP_VSC_ECC_COG2_2_D
Reset:	soft
Address:	63304h-63307h
Name:	Transcoder Video Data Island Packet GMP ECC 0
ShortName:	VIDEO_DIP_GMP_ECC_0_D
Reset:	soft

Address:	63308h-6330Bh
Name:	Transcoder Video Data Island Packet GMP ECC 1
ShortName:	VIDEO_DIP_GMP_ECC_1_D
Reset:	soft
Address:	6330Ch-6330Fh
Name:	Transcoder Video Data Island Packet GMP ECC 2
ShortName:	VIDEO_DIP_GMP_ECC_2_D
Reset:	soft
Address:	63310h-63313h
Name:	Transcoder Video Data Island Packet GMP ECC 3
ShortName:	VIDEO_DIP_GMP_ECC_3_D
Reset:	soft
Address:	63314h-63317h
Name:	Transcoder Video Data Island Packet GMP ECC 4
ShortName:	VIDEO_DIP_GMP_ECC_4_D
Reset:	soft
Address:	63344h-63347h
Name:	Transcoder Video Data Island Packet VSC ECC 0
ShortName:	VIDEO_DIP_VSC_ECC_0_D
Reset:	soft
Address:	63348h-6334Bh
Name:	Transcoder Video Data Island Packet VSC ECC 1
ShortName:	VIDEO_DIP_VSC_ECC_1_D
Reset:	soft
Address:	6334Ch-6334Fh
Name:	Transcoder Video Data Island Packet VSC ECC 2
ShortName:	VIDEO_DIP_VSC_ECC_2_D
Reset:	soft
Address:	634A8h-634ABh
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 0
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_0_D
Reset:	soft
Address:	634ACh-634AFh
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 1
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_1_D
Reset:	soft

Address:	634B0h-634B3h
Name:	Transcoder Video Data Island Packet Adaptive Sync ECC 2
ShortName:	VIDEO_DIP_ADAPTIVE_SYNC_ECC_2_D
Reset:	soft

There are multiple instances of this register format per DIP type and per transcoder.

DWord	Bit	Description
0	31:0	**Video DIP ECC** Access: RO This field contains the video DIP ECC value for read back.

VIDEO_DIP_GCP

VIDEO_DIP_GCP

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32

Address:	60210h-60213h
Name:	Transcoder Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_A
Reset:	soft

Address:	61210h-61213h
Name:	Transcoder Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_B
Reset:	soft

Address:	62210h-62213h
Name:	Transcoder Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_C
Reset:	soft

Address:	63210h-63213h
Name:	Transcoder Video Data Island Packet GCP
ShortName:	VIDEO_DIP_GCP_D
Reset:	soft

DWord	Bit	Description
0	31:3	**Reserved** Access: RO Format: MBZ
	2	**GCP color indication** Access: Double Buffered **Value** / **Name** / **Description** 0b / Don't Indicate / Don't indicate color depth. CD and PP bits in GCP set to zero. 1b / Indicate / Indicate color depth using CD bits in GCP. The color depth value comes from the TRANS_DDI_FUNC_CTL register. **Restriction** This bit must be set when in HDMI deep color (>8 BPC) mode.

VIDEO_DIP_GCP

1 **GCP default phase enable**

Access:	Double Buffered

GCP default phase indicates that video timings meet alignment requirements such that the following conditions are met:

1. Htotal is a multiple of the value given in the table below
2. Hactive is an even number
3. Front and back porches for Hsync are even numbers
4. Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0)

BPC	Color Format	Htotal Multiple Requirement
8	RGB	2
8	YUV420	4
10	RGB	4
10	YUV420	8
12	RGB	2
12	YUV420	4

Value	Name	Description
0b	Clear	Default phase bit in GCP is cleared.
1b	Set	Default phase bit in GCP is set.

Restriction
Do not set this bit if these requirements are not met.

0 **Reserved**

Access:	R/W

VIDEO_DIP_PPS_DATA

VIDEO_DIP_PPS_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60350h-60353h
Name:	Transcoder Video Data Island Packet for PPS 0
ShortName:	VIDEO_DIP_PPS_DATA_0_A
Reset:	soft
Address:	60354h-60357h
Name:	Transcoder Video Data Island Packet for PPS 1
ShortName:	VIDEO_DIP_PPS_DATA_1_A
Reset:	soft
Address:	60358h-6035Bh
Name:	Transcoder Video Data Island Packet for PPS 2
ShortName:	VIDEO_DIP_PPS_DATA_2_A
Reset:	soft
Address:	6035Ch-6035Fh
Name:	Transcoder Video Data Island Packet for PPS 3
ShortName:	VIDEO_DIP_PPS_DATA_3_A
Reset:	soft
Address:	60360h-60363h
Name:	Transcoder Video Data Island Packet for PPS 4
ShortName:	VIDEO_DIP_PPS_DATA_4_A
Reset:	soft
Address:	60364h-60367h
Name:	Transcoder Video Data Island Packet for PPS 5
ShortName:	VIDEO_DIP_PPS_DATA_5_A
Reset:	soft
Address:	60368h-6036Bh
Name:	Transcoder Video Data Island Packet for PPS 6
ShortName:	VIDEO_DIP_PPS_DATA_6_A
Reset:	soft
Address:	6036Ch-6036Fh
Name:	Transcoder Video Data Island Packet for PPS 7
ShortName:	VIDEO_DIP_PPS_DATA_7_A

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	60370h-60373h
Name:	Transcoder Video Data Island Packet for PPS 8
ShortName:	VIDEO_DIP_PPS_DATA_8_A
Reset:	soft
Address:	60374h-60377h
Name:	Transcoder Video Data Island Packet for PPS 9
ShortName:	VIDEO_DIP_PPS_DATA_9_A
Reset:	soft
Address:	60378h-6037Bh
Name:	Transcoder Video Data Island Packet for PPS 10
ShortName:	VIDEO_DIP_PPS_DATA_10_A
Reset:	soft
Address:	6037Ch-6037Fh
Name:	Transcoder Video Data Island Packet for PPS 11
ShortName:	VIDEO_DIP_PPS_DATA_11_A
Reset:	soft
Address:	60380h-60383h
Name:	Transcoder Video Data Island Packet for PPS 12
ShortName:	VIDEO_DIP_PPS_DATA_12_A
Reset:	soft
Address:	60384h-60387h
Name:	Transcoder Video Data Island Packet for PPS 13
ShortName:	VIDEO_DIP_PPS_DATA_13_A
Reset:	soft
Address:	60388h-6038Bh
Name:	Transcoder Video Data Island Packet for PPS 14
ShortName:	VIDEO_DIP_PPS_DATA_14_A
Reset:	soft
Address:	6038Ch-6038Fh
Name:	Transcoder Video Data Island Packet for PPS 15
ShortName:	VIDEO_DIP_PPS_DATA_15_A
Reset:	soft
Address:	60390h-60393h
Name:	Transcoder Video Data Island Packet for PPS 16
ShortName:	VIDEO_DIP_PPS_DATA_16_A

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	60394h-60397h
Name:	Transcoder Video Data Island Packet for PPS 17
ShortName:	VIDEO_DIP_PPS_DATA_17_A
Reset:	soft
Address:	60398h-6039Bh
Name:	Transcoder Video Data Island Packet for PPS 18
ShortName:	VIDEO_DIP_PPS_DATA_18_A
Reset:	soft
Address:	6039Ch-6039Fh
Name:	Transcoder Video Data Island Packet for PPS 19
ShortName:	VIDEO_DIP_PPS_DATA_19_A
Reset:	soft
Address:	603A0h-603A3h
Name:	Transcoder Video Data Island Packet for PPS 20
ShortName:	VIDEO_DIP_PPS_DATA_20_A
Reset:	soft
Address:	603A4h-603A7h
Name:	Transcoder Video Data Island Packet for PPS 21
ShortName:	VIDEO_DIP_PPS_DATA_21_A
Reset:	soft
Address:	603A8h-603ABh
Name:	Transcoder Video Data Island Packet for PPS 22
ShortName:	VIDEO_DIP_PPS_DATA_22_A
Reset:	soft
Address:	603ACh-603AFh
Name:	Transcoder Video Data Island Packet for PPS 23
ShortName:	VIDEO_DIP_PPS_DATA_23_A
Reset:	soft
Address:	603B0h-603B3h
Name:	Transcoder Video Data Island Packet for PPS 24
ShortName:	VIDEO_DIP_PPS_DATA_24_A
Reset:	soft
Address:	603B4h-603B7h
Name:	Transcoder Video Data Island Packet for PPS 25
ShortName:	VIDEO_DIP_PPS_DATA_25_A

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	603B8h-603BBh
Name:	Transcoder Video Data Island Packet for PPS 26
ShortName:	VIDEO_DIP_PPS_DATA_26_A
Reset:	soft
Address:	603BCh-603BFh
Name:	Transcoder Video Data Island Packet for PPS 27
ShortName:	VIDEO_DIP_PPS_DATA_27_A
Reset:	soft
Address:	603C0h-603C3h
Name:	Transcoder Video Data Island Packet for PPS 28
ShortName:	VIDEO_DIP_PPS_DATA_28_A
Reset:	soft
Address:	603C4h-603C7h
Name:	Transcoder Video Data Island Packet for PPS 29
ShortName:	VIDEO_DIP_PPS_DATA_29_A
Reset:	soft
Address:	603C8h-603CBh
Name:	Transcoder Video Data Island Packet for PPS 30
ShortName:	VIDEO_DIP_PPS_DATA_30_A
Reset:	soft
Address:	603CCh-603CFh
Name:	Transcoder Video Data Island Packet for PPS 31
ShortName:	VIDEO_DIP_PPS_DATA_31_A
Reset:	soft
Address:	603D0h-603D3h
Name:	Transcoder Video Data Island Packet for PPS 32
ShortName:	VIDEO_DIP_PPS_DATA_32_A
Reset:	soft
Address:	61350h-61353h
Name:	Transcoder Video Data Island Packet for PPS 0
ShortName:	VIDEO_DIP_PPS_DATA_0_B
Reset:	soft
Address:	61354h-61357h
Name:	Transcoder Video Data Island Packet for PPS 1
ShortName:	VIDEO_DIP_PPS_DATA_1_B

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	61358h-6135Bh
Name:	Transcoder Video Data Island Packet for PPS 2
ShortName:	VIDEO_DIP_PPS_DATA_2_B
Reset:	soft
Address:	6135Ch-6135Fh
Name:	Transcoder Video Data Island Packet for PPS 3
ShortName:	VIDEO_DIP_PPS_DATA_3_B
Reset:	soft
Address:	61360h-61363h
Name:	Transcoder Video Data Island Packet for PPS 4
ShortName:	VIDEO_DIP_PPS_DATA_4_B
Reset:	soft
Address:	61364h-61367h
Name:	Transcoder Video Data Island Packet for PPS 5
ShortName:	VIDEO_DIP_PPS_DATA_5_B
Reset:	soft
Address:	61368h-6136Bh
Name:	Transcoder Video Data Island Packet for PPS 6
ShortName:	VIDEO_DIP_PPS_DATA_6_B
Reset:	soft
Address:	6136Ch-6136Fh
Name:	Transcoder Video Data Island Packet for PPS 7
ShortName:	VIDEO_DIP_PPS_DATA_7_B
Reset:	soft
Address:	61370h-61373h
Name:	Transcoder Video Data Island Packet for PPS 8
ShortName:	VIDEO_DIP_PPS_DATA_8_B
Reset:	soft
Address:	61374h-61377h
Name:	Transcoder Video Data Island Packet for PPS 9
ShortName:	VIDEO_DIP_PPS_DATA_9_B
Reset:	soft
Address:	61378h-6137Bh
Name:	Transcoder Video Data Island Packet for PPS 10
ShortName:	VIDEO_DIP_PPS_DATA_10_B

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	6137Ch-6137Fh
Name:	Transcoder Video Data Island Packet for PPS 11
ShortName:	VIDEO_DIP_PPS_DATA_11_B
Reset:	soft
Address:	61380h-61383h
Name:	Transcoder Video Data Island Packet for PPS 12
ShortName:	VIDEO_DIP_PPS_DATA_12_B
Reset:	soft
Address:	61384h-61387h
Name:	Transcoder Video Data Island Packet for PPS 13
ShortName:	VIDEO_DIP_PPS_DATA_13_B
Reset:	soft
Address:	61388h-6138Bh
Name:	Transcoder Video Data Island Packet for PPS 14
ShortName:	VIDEO_DIP_PPS_DATA_14_B
Reset:	soft
Address:	6138Ch-6138Fh
Name:	Transcoder Video Data Island Packet for PPS 15
ShortName:	VIDEO_DIP_PPS_DATA_15_B
Reset:	soft
Address:	61390h-61393h
Name:	Transcoder Video Data Island Packet for PPS 16
ShortName:	VIDEO_DIP_PPS_DATA_16_B
Reset:	soft
Address:	61394h-61397h
Name:	Transcoder Video Data Island Packet for PPS 17
ShortName:	VIDEO_DIP_PPS_DATA_17_B
Reset:	soft
Address:	61398h-6139Bh
Name:	Transcoder Video Data Island Packet for PPS 18
ShortName:	VIDEO_DIP_PPS_DATA_18_B
Reset:	soft
Address:	6139Ch-6139Fh
Name:	Transcoder Video Data Island Packet for PPS 19
ShortName:	VIDEO_DIP_PPS_DATA_19_B

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	613A0h-613A3h
Name:	Transcoder Video Data Island Packet for PPS 20
ShortName:	VIDEO_DIP_PPS_DATA_20_B
Reset:	soft
Address:	613A4h-613A7h
Name:	Transcoder Video Data Island Packet for PPS 21
ShortName:	VIDEO_DIP_PPS_DATA_21_B
Reset:	soft
Address:	613A8h-613ABh
Name:	Transcoder Video Data Island Packet for PPS 22
ShortName:	VIDEO_DIP_PPS_DATA_22_B
Reset:	soft
Address:	613ACh-613AFh
Name:	Transcoder Video Data Island Packet for PPS 23
ShortName:	VIDEO_DIP_PPS_DATA_23_B
Reset:	soft
Address:	613B0h-613B3h
Name:	Transcoder Video Data Island Packet for PPS 24
ShortName:	VIDEO_DIP_PPS_DATA_24_B
Reset:	soft
Address:	613B4h-613B7h
Name:	Transcoder Video Data Island Packet for PPS 25
ShortName:	VIDEO_DIP_PPS_DATA_25_B
Reset:	soft
Address:	613B8h-613BBh
Name:	Transcoder Video Data Island Packet for PPS 26
ShortName:	VIDEO_DIP_PPS_DATA_26_B
Reset:	soft
Address:	613BCh-613BFh
Name:	Transcoder Video Data Island Packet for PPS 27
ShortName:	VIDEO_DIP_PPS_DATA_27_B
Reset:	soft
Address:	613C0h-613C3h
Name:	Transcoder Video Data Island Packet for PPS 28
ShortName:	VIDEO_DIP_PPS_DATA_28_B

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	613C4h-613C7h
Name:	Transcoder Video Data Island Packet for PPS 29
ShortName:	VIDEO_DIP_PPS_DATA_29_B
Reset:	soft
Address:	613C8h-613CBh
Name:	Transcoder Video Data Island Packet for PPS 30
ShortName:	VIDEO_DIP_PPS_DATA_30_B
Reset:	soft
Address:	613CCh-613CFh
Name:	Transcoder Video Data Island Packet for PPS 31
ShortName:	VIDEO_DIP_PPS_DATA_31_B
Reset:	soft
Address:	613D0h-613D3h
Name:	Transcoder Video Data Island Packet for PPS 32
ShortName:	VIDEO_DIP_PPS_DATA_32_B
Reset:	soft
Address:	62350h-62353h
Name:	Transcoder Video Data Island Packet for PPS 0
ShortName:	VIDEO_DIP_PPS_DATA_0_C
Reset:	soft
Address:	62354h-62357h
Name:	Transcoder Video Data Island Packet for PPS 1
ShortName:	VIDEO_DIP_PPS_DATA_1_C
Reset:	soft
Address:	62358h-6235Bh
Name:	Transcoder Video Data Island Packet for PPS 2
ShortName:	VIDEO_DIP_PPS_DATA_2_C
Reset:	soft
Address:	6235Ch-6235Fh
Name:	Transcoder Video Data Island Packet for PPS 3
ShortName:	VIDEO_DIP_PPS_DATA_3_C
Reset:	soft
Address:	62360h-62363h
Name:	Transcoder Video Data Island Packet for PPS 4
ShortName:	VIDEO_DIP_PPS_DATA_4_C

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	62364h-62367h
Name:	Transcoder Video Data Island Packet for PPS 5
ShortName:	VIDEO_DIP_PPS_DATA_5_C
Reset:	soft
Address:	62368h-6236Bh
Name:	Transcoder Video Data Island Packet for PPS 6
ShortName:	VIDEO_DIP_PPS_DATA_6_C
Reset:	soft
Address:	6236Ch-6236Fh
Name:	Transcoder Video Data Island Packet for PPS 7
ShortName:	VIDEO_DIP_PPS_DATA_7_C
Reset:	soft
Address:	62370h-62373h
Name:	Transcoder Video Data Island Packet for PPS 8
ShortName:	VIDEO_DIP_PPS_DATA_8_C
Reset:	soft
Address:	62374h-62377h
Name:	Transcoder Video Data Island Packet for PPS 9
ShortName:	VIDEO_DIP_PPS_DATA_9_C
Reset:	soft
Address:	62378h-6237Bh
Name:	Transcoder Video Data Island Packet for PPS 10
ShortName:	VIDEO_DIP_PPS_DATA_10_C
Reset:	soft
Address:	6237Ch-6237Fh
Name:	Transcoder Video Data Island Packet for PPS 11
ShortName:	VIDEO_DIP_PPS_DATA_11_C
Reset:	soft
Address:	62380h-62383h
Name:	Transcoder Video Data Island Packet for PPS 12
ShortName:	VIDEO_DIP_PPS_DATA_12_C
Reset:	soft
Address:	62384h-62387h
Name:	Transcoder Video Data Island Packet for PPS 13
ShortName:	VIDEO_DIP_PPS_DATA_13_C

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	62388h-6238Bh
Name:	Transcoder Video Data Island Packet for PPS 14
ShortName:	VIDEO_DIP_PPS_DATA_14_C
Reset:	soft
Address:	6238Ch-6238Fh
Name:	Transcoder Video Data Island Packet for PPS 15
ShortName:	VIDEO_DIP_PPS_DATA_15_C
Reset:	soft
Address:	62390h-62393h
Name:	Transcoder Video Data Island Packet for PPS 16
ShortName:	VIDEO_DIP_PPS_DATA_16_C
Reset:	soft
Address:	62394h-62397h
Name:	Transcoder Video Data Island Packet for PPS 17
ShortName:	VIDEO_DIP_PPS_DATA_17_C
Reset:	soft
Address:	62398h-6239Bh
Name:	Transcoder Video Data Island Packet for PPS 18
ShortName:	VIDEO_DIP_PPS_DATA_18_C
Reset:	soft
Address:	6239Ch-6239Fh
Name:	Transcoder Video Data Island Packet for PPS 19
ShortName:	VIDEO_DIP_PPS_DATA_19_C
Reset:	soft
Address:	623A0h-623A3h
Name:	Transcoder Video Data Island Packet for PPS 20
ShortName:	VIDEO_DIP_PPS_DATA_20_C
Reset:	soft
Address:	623A4h-623A7h
Name:	Transcoder Video Data Island Packet for PPS 21
ShortName:	VIDEO_DIP_PPS_DATA_21_C
Reset:	soft
Address:	623A8h-623ABh
Name:	Transcoder Video Data Island Packet for PPS 22
ShortName:	VIDEO_DIP_PPS_DATA_22_C

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	623ACh-623AFh
Name:	Transcoder Video Data Island Packet for PPS 23
ShortName:	VIDEO_DIP_PPS_DATA_23_C
Reset:	soft
Address:	623B0h-623B3h
Name:	Transcoder Video Data Island Packet for PPS 24
ShortName:	VIDEO_DIP_PPS_DATA_24_C
Reset:	soft
Address:	623B4h-623B7h
Name:	Transcoder Video Data Island Packet for PPS 25
ShortName:	VIDEO_DIP_PPS_DATA_25_C
Reset:	soft
Address:	623B8h-623BBh
Name:	Transcoder Video Data Island Packet for PPS 26
ShortName:	VIDEO_DIP_PPS_DATA_26_C
Reset:	soft
Address:	623BCh-623BFh
Name:	Transcoder Video Data Island Packet for PPS 27
ShortName:	VIDEO_DIP_PPS_DATA_27_C
Reset:	soft
Address:	623C0h-623C3h
Name:	Transcoder Video Data Island Packet for PPS 28
ShortName:	VIDEO_DIP_PPS_DATA_28_C
Reset:	soft
Address:	623C4h-623C7h
Name:	Transcoder Video Data Island Packet for PPS 29
ShortName:	VIDEO_DIP_PPS_DATA_29_C
Reset:	soft
Address:	623C8h-623CBh
Name:	Transcoder Video Data Island Packet for PPS 30
ShortName:	VIDEO_DIP_PPS_DATA_30_C
Reset:	soft
Address:	623CCh-623CFh
Name:	Transcoder Video Data Island Packet for PPS 31
ShortName:	VIDEO_DIP_PPS_DATA_31_C

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	623D0h-623D3h
Name:	Transcoder Video Data Island Packet for PPS 32
ShortName:	VIDEO_DIP_PPS_DATA_32_C
Reset:	soft
Address:	63350h-63353h
Name:	Transcoder Video Data Island Packet for PPS 0
ShortName:	VIDEO_DIP_PPS_DATA_0_D
Reset:	soft
Address:	63354h-63357h
Name:	Transcoder Video Data Island Packet for PPS 1
ShortName:	VIDEO_DIP_PPS_DATA_1_D
Reset:	soft
Address:	63358h-6335Bh
Name:	Transcoder Video Data Island Packet for PPS 2
ShortName:	VIDEO_DIP_PPS_DATA_2_D
Reset:	soft
Address:	6335Ch-6335Fh
Name:	Transcoder Video Data Island Packet for PPS 3
ShortName:	VIDEO_DIP_PPS_DATA_3_D
Reset:	soft
Address:	63360h-63363h
Name:	Transcoder Video Data Island Packet for PPS 4
ShortName:	VIDEO_DIP_PPS_DATA_4_D
Reset:	soft
Address:	63364h-63367h
Name:	Transcoder Video Data Island Packet for PPS 5
ShortName:	VIDEO_DIP_PPS_DATA_5_D
Reset:	soft
Address:	63368h-6336Bh
Name:	Transcoder Video Data Island Packet for PPS 6
ShortName:	VIDEO_DIP_PPS_DATA_6_D
Reset:	soft
Address:	6336Ch-6336Fh
Name:	Transcoder Video Data Island Packet for PPS 7
ShortName:	VIDEO_DIP_PPS_DATA_7_D

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	63370h-63373h
Name:	Transcoder Video Data Island Packet for PPS 8
ShortName:	VIDEO_DIP_PPS_DATA_8_D
Reset:	soft
Address:	63374h-63377h
Name:	Transcoder Video Data Island Packet for PPS 9
ShortName:	VIDEO_DIP_PPS_DATA_9_D
Reset:	soft
Address:	63378h-6337Bh
Name:	Transcoder Video Data Island Packet for PPS 10
ShortName:	VIDEO_DIP_PPS_DATA_10_D
Reset:	soft
Address:	6337Ch-6337Fh
Name:	Transcoder Video Data Island Packet for PPS 11
ShortName:	VIDEO_DIP_PPS_DATA_11_D
Reset:	soft
Address:	63380h-63383h
Name:	Transcoder Video Data Island Packet for PPS 12
ShortName:	VIDEO_DIP_PPS_DATA_12_D
Reset:	soft
Address:	63384h-63387h
Name:	Transcoder Video Data Island Packet for PPS 13
ShortName:	VIDEO_DIP_PPS_DATA_13_D
Reset:	soft
Address:	63388h-6338Bh
Name:	Transcoder Video Data Island Packet for PPS 14
ShortName:	VIDEO_DIP_PPS_DATA_14_D
Reset:	soft
Address:	6338Ch-6338Fh
Name:	Transcoder Video Data Island Packet for PPS 15
ShortName:	VIDEO_DIP_PPS_DATA_15_D
Reset:	soft
Address:	63390h-63393h
Name:	Transcoder Video Data Island Packet for PPS 16
ShortName:	VIDEO_DIP_PPS_DATA_16_D

VIDEO_DIP_PPS_DATA	
Reset:	soft
Address:	63394h-63397h
Name:	Transcoder Video Data Island Packet for PPS 17
ShortName:	VIDEO_DIP_PPS_DATA_17_D
Reset:	soft
Address:	63398h-6339Bh
Name:	Transcoder Video Data Island Packet for PPS 18
ShortName:	VIDEO_DIP_PPS_DATA_18_D
Reset:	soft
Address:	6339Ch-6339Fh
Name:	Transcoder Video Data Island Packet for PPS 19
ShortName:	VIDEO_DIP_PPS_DATA_19_D
Reset:	soft
Address:	633A0h-633A3h
Name:	Transcoder Video Data Island Packet for PPS 20
ShortName:	VIDEO_DIP_PPS_DATA_20_D
Reset:	soft
Address:	633A4h-633A7h
Name:	Transcoder Video Data Island Packet for PPS 21
ShortName:	VIDEO_DIP_PPS_DATA_21_D
Reset:	soft
Address:	633A8h-633ABh
Name:	Transcoder Video Data Island Packet for PPS 22
ShortName:	VIDEO_DIP_PPS_DATA_22_D
Reset:	soft
Address:	633ACh-633AFh
Name:	Transcoder Video Data Island Packet for PPS 23
ShortName:	VIDEO_DIP_PPS_DATA_23_D
Reset:	soft
Address:	633B0h-633B3h
Name:	Transcoder Video Data Island Packet for PPS 24
ShortName:	VIDEO_DIP_PPS_DATA_24_D
Reset:	soft
Address:	633B4h-633B7h
Name:	Transcoder Video Data Island Packet for PPS 25
ShortName:	VIDEO_DIP_PPS_DATA_25_D

VIDEO_DIP_PPS_DATA

Reset:	soft
Address:	633B8h-633BBh
Name:	Transcoder Video Data Island Packet for PPS 26
ShortName:	VIDEO_DIP_PPS_DATA_26_D
Reset:	soft
Address:	633BCh-633BFh
Name:	Transcoder Video Data Island Packet for PPS 27
ShortName:	VIDEO_DIP_PPS_DATA_27_D
Reset:	soft
Address:	633C0h-633C3h
Name:	Transcoder Video Data Island Packet for PPS 28
ShortName:	VIDEO_DIP_PPS_DATA_28_D
Reset:	soft
Address:	633C4h-633C7h
Name:	Transcoder Video Data Island Packet for PPS 29
ShortName:	VIDEO_DIP_PPS_DATA_29_D
Reset:	soft
Address:	633C8h-633CBh
Name:	Transcoder Video Data Island Packet for PPS 30
ShortName:	VIDEO_DIP_PPS_DATA_30_D
Reset:	soft
Address:	633CCh-633CFh
Name:	Transcoder Video Data Island Packet for PPS 31
ShortName:	VIDEO_DIP_PPS_DATA_31_D
Reset:	soft
Address:	633D0h-633D3h
Name:	Transcoder Video Data Island Packet for PPS 32
ShortName:	VIDEO_DIP_PPS_DATA_32_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Video DIP PPS data** Access: Double Buffered Video data island packet for PPS data.

VIDEO_DIP_PPS_ECC

VIDEO_DIP_PPS_ECC	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	603D4h-603D7h
Name:	Transcoder Video DIP for PPS ECC 0
ShortName:	VIDEO_DIP_PPS_ECC_0_A
Reset:	soft
Address:	603D8h-603DBh
Name:	Transcoder Video DIP for PPS ECC 1
ShortName:	VIDEO_DIP_PPS_ECC_1_A
Reset:	soft
Address:	603DCh-603DFh
Name:	Transcoder Video DIP for PPS ECC 2
ShortName:	VIDEO_DIP_PPS_ECC_2_A
Reset:	soft
Address:	603E0h-603E3h
Name:	Transcoder Video DIP for PPS ECC 3
ShortName:	VIDEO_DIP_PPS_ECC_3_A
Reset:	soft
Address:	603E4h-603E7h
Name:	Transcoder Video DIP for PPS ECC 4
ShortName:	VIDEO_DIP_PPS_ECC_4_A
Reset:	soft
Address:	603E8h-603EBh
Name:	Transcoder Video DIP for PPS ECC 5
ShortName:	VIDEO_DIP_PPS_ECC_5_A
Reset:	soft
Address:	603ECh-603EFh
Name:	Transcoder Video DIP for PPS ECC 6
ShortName:	VIDEO_DIP_PPS_ECC_6_A
Reset:	soft
Address:	603F0h-603F3h
Name:	Transcoder Video DIP for PPS ECC 7
ShortName:	VIDEO_DIP_PPS_ECC_7_A

VIDEO_DIP_PPS_ECC	
Reset:	soft
Address:	603F4h-603F7h
Name:	Transcoder Video DIP for PPS ECC 8
ShortName:	VIDEO_DIP_PPS_ECC_8_A
Reset:	soft
Address:	613D4h-613D7h
Name:	Transcoder Video DIP for PPS ECC 0
ShortName:	VIDEO_DIP_PPS_ECC_0_B
Reset:	soft
Address:	613D8h-613DBh
Name:	Transcoder Video DIP for PPS ECC 1
ShortName:	VIDEO_DIP_PPS_ECC_1_B
Reset:	soft
Address:	613DCh-613DFh
Name:	Transcoder Video DIP for PPS ECC 2
ShortName:	VIDEO_DIP_PPS_ECC_2_B
Reset:	soft
Address:	613E0h-613E3h
Name:	Transcoder Video DIP for PPS ECC 3
ShortName:	VIDEO_DIP_PPS_ECC_3_B
Reset:	soft
Address:	613E4h-613E7h
Name:	Transcoder Video DIP for PPS ECC 4
ShortName:	VIDEO_DIP_PPS_ECC_4_B
Reset:	soft
Address:	613E8h-613EBh
Name:	Transcoder Video DIP for PPS ECC 5
ShortName:	VIDEO_DIP_PPS_ECC_5_B
Reset:	soft
Address:	613ECh-613EFh
Name:	Transcoder Video DIP for PPS ECC 6
ShortName:	VIDEO_DIP_PPS_ECC_6_B
Reset:	soft
Address:	613F0h-613F3h
Name:	Transcoder Video DIP for PPS ECC 7
ShortName:	VIDEO_DIP_PPS_ECC_7_B

VIDEO_DIP_PPS_ECC	
Reset:	soft
Address:	613F4h-613F7h
Name:	Transcoder Video DIP for PPS ECC 8
ShortName:	VIDEO_DIP_PPS_ECC_8_B
Reset:	soft
Address:	623D4h-623D7h
Name:	Transcoder Video DIP for PPS ECC 0
ShortName:	VIDEO_DIP_PPS_ECC_0_C
Reset:	soft
Address:	623D8h-623DBh
Name:	Transcoder Video DIP for PPS ECC 1
ShortName:	VIDEO_DIP_PPS_ECC_1_C
Reset:	soft
Address:	623DCh-623DFh
Name:	Transcoder Video DIP for PPS ECC 2
ShortName:	VIDEO_DIP_PPS_ECC_2_C
Reset:	soft
Address:	623E0h-623E3h
Name:	Transcoder Video DIP for PPS ECC 3
ShortName:	VIDEO_DIP_PPS_ECC_3_C
Reset:	soft
Address:	623E4h-623E7h
Name:	Transcoder Video DIP for PPS ECC 4
ShortName:	VIDEO_DIP_PPS_ECC_4_C
Reset:	soft
Address:	623E8h-623EBh
Name:	Transcoder Video DIP for PPS ECC 5
ShortName:	VIDEO_DIP_PPS_ECC_5_C
Reset:	soft
Address:	623ECh-623EFh
Name:	Transcoder Video DIP for PPS ECC 6
ShortName:	VIDEO_DIP_PPS_ECC_6_C
Reset:	soft
Address:	623F0h-623F3h
Name:	Transcoder Video DIP for PPS ECC 7
ShortName:	VIDEO_DIP_PPS_ECC_7_C

VIDEO_DIP_PPS_ECC	
Reset:	soft
Address:	623F4h-623F7h
Name:	Transcoder Video DIP for PPS ECC 8
ShortName:	VIDEO_DIP_PPS_ECC_8_C
Reset:	soft
Address:	633D4h-633D7h
Name:	Transcoder Video DIP for PPS ECC 0
ShortName:	VIDEO_DIP_PPS_ECC_0_D
Reset:	soft
Address:	633D8h-633DBh
Name:	Transcoder Video DIP for PPS ECC 1
ShortName:	VIDEO_DIP_PPS_ECC_1_D
Reset:	soft
Address:	633DCh-633DFh
Name:	Transcoder Video DIP for PPS ECC 2
ShortName:	VIDEO_DIP_PPS_ECC_2_D
Reset:	soft
Address:	633E0h-633E3h
Name:	Transcoder Video DIP for PPS ECC 3
ShortName:	VIDEO_DIP_PPS_ECC_3_D
Reset:	soft
Address:	633E4h-633E7h
Name:	Transcoder Video DIP for PPS ECC 4
ShortName:	VIDEO_DIP_PPS_ECC_4_D
Reset:	soft
Address:	633E8h-633EBh
Name:	Transcoder Video DIP for PPS ECC 5
ShortName:	VIDEO_DIP_PPS_ECC_5_D
Reset:	soft
Address:	633ECh-633EFh
Name:	Transcoder Video DIP for PPS ECC 6
ShortName:	VIDEO_DIP_PPS_ECC_6_D
Reset:	soft
Address:	633F0h-633F3h
Name:	Transcoder Video DIP for PPS ECC 7
ShortName:	VIDEO_DIP_PPS_ECC_7_D

VIDEO_DIP_PPS_ECC

Reset:	soft

Address:	633F4h-633F7h
Name:	Transcoder Video DIP for PPS ECC 8
ShortName:	VIDEO_DIP_PPS_ECC_8_D
Reset:	soft

This represents 36 bytes of ECC over PPS DIP.

DWord	Bit	Description
0	31:0	**Video DIP PPS ECC** Access: RO ECC for PPS DIP.

Video BIOS ROM Base Address

ROMADR_0_2_0_PCI - Video BIOS ROM Base Address

Register Space:	PCI: 0/2/0
Size (in bits):	32
Address:	00030h

Description

Gdie will have an Expansion ROM. The base address register allows access.

DWord	Bit	Description
0	31:21	**ROM Base Address** Default Value: 000h Access: R/W _Custom_GTIReset: BUS Determines the base value of the expansion ROM address.
	20:11	**Address Mask** Default Value: 000000000b Access: RO _Custom_GTIReset: BUS 1MB size expansion ROM size supported.
	10:1	**Reserved** Access: RO Format: MBZ
	0	**ROM BIOS Enable** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Expansion ROM BAR enable bit.

VIRTUALIZATION CONTROL REGISTER

VIRTUAL_CTRL_REG - VIRTUALIZATION CONTROL REGISTER

Register Space: MMIO: 0/2/0
Size (in bits): 32

Address: 10108Ch

This register is used to identify which Virtual Function, if any, is allowed to access or configure the Global GTT Entry.

DWord	Bit	Description
0	31:9	**Reserved** Access: RO Format: MBZ
	8	**Guest Direct GGTT Update Enable** Access: RO _Custom_GTIReset: BUS Determines whether a Guest VM is able to directly update GGTT entries that have been assigned to it, via the VF GTTMMADR assigned to that Guest. Hardcoded to 1
	7:0	**Reserved** Access: RO Format: MBZ

Value	Name	Description
1b	**[Default]**	Guest VM can modify allowed GGTT Entry fields.
0b		Reserved

VSC_EXT_SDP_CONF

VSC_EXT_SDP_CONF	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60288h-6028Bh
Name:	Transcoder VSD Extended SDP Configuration
ShortName:	VSC_EXT_SDP_CONF_A
Reset:	soft
Address:	61288h-6128Bh
Name:	Transcoder VSD Extended SDP Configuration
ShortName:	VSC_EXT_SDP_CONF_B
Reset:	soft
Address:	62288h-6228Bh
Name:	Transcoder VSD Extended SDP Configuration
ShortName:	VSC_EXT_SDP_CONF_C
Reset:	soft
Address:	63288h-6328Bh
Name:	Transcoder VSD Extended SDP Configuration
ShortName:	VSC_EXT_SDP_CONF_D
Reset:	soft

DWord	Bit	Description
0	31	**Chain done** Access: RO Read by software/DSB to know if it can start sending new chain. Chained metadata straddling 2 buffers need to know this status. Value: 0b — Name: HW sending previous chain Value: 1b — Name: HW completed sending previous chain
	30:25	**Reserved** Access: RO Format: MBZ

VSC_EXT_SDP_CONF

24 Buffer Replay

Access:	R/W

This field allows metadata to be replayed from the buffer without having to write the metadata buffer each time/frame.
This bit may only be changed when metadata buffer is invalidated.

Value	Name
0b	Transmit once
1b	Transmit every frame

23 SDP Active Error

Access:	R/WC

This bit represents an error condition that not all SDPs were read when video active region is reached.
HW will stop transmitting metadata once active region is reached.
This bit is set by HW and cleared by SW by writing '1'.
To avoid false indication of an error, SW can choose either of the following methods:

1. Avoid programming VSC_EXT registers and setting the buffer ready bit in VSC_EXT_SDP_CTL before vblank rises.
2. Program VSC_EXT registers and set the buffer ready bit in VSC_EXT_SDP_CTL anytime, but clear the SDP Active Error at the start of vblank, so that it can be rechecked at the end of vblank to indicate real issues.

Value	Name
0b	All SDPs transmitted in VBLANK
1b	All SDPs not transmitted in VBLANK

22 Block mode

Access:	R/W

When this bit is set to 1, it is software responsibility to set Middle Of Chaining bit [23] and Packet sequence bits [28:24] in the header packet that it programs in metadata register.
HW does not support changing this field during transmission.

Value	Name
0b	Header values from Header register
1b	Header values from SW/DSB written buffer

21:10 HBLANK early indication

Access:	R/W

In HW, this field is expressed in terms of pixels and not clocks.
It provides a guardband to stop the VSC_EXT_SDP transmission from going into Hblank region (for Audio).
For eg: If this field is programed to 20 pixels, then when horizontal counter reaches (HActive -20), VSC_EXT_SDP transmission stops.
If a packet is in the middle of transmission, then it completes before stopping. Transmission resumes on the next HActive.
In MST/DP2 this transmission can happen only when an MTP slot is available.

VSC_EXT_SDP_CONF		
		For all SST/MST/DP2 use cases, recommendation is to use 10% of HActive.
	9:0	**Packets per chain** Access: R/W This field specifies the total number of packets (each packet has 32 bytes) in the chain. = Number of bytes/32

VSC_EXT_SDP_CTL

VSC_EXT_SDP_CTL	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60290h-60293h
Name:	Transcoder VSD Extended SDP Control 0
ShortName:	VSC_EXT_SDP_CTL_0_A
Reset:	soft
Address:	60294h-60297h
Name:	Transcoder VSD Extended SDP Control 1
ShortName:	VSC_EXT_SDP_CTL_1_A
Reset:	soft
Address:	61290h-61293h
Name:	Transcoder VSD Extended SDP Control 0
ShortName:	VSC_EXT_SDP_CTL_0_B
Reset:	soft
Address:	61294h-61297h
Name:	Transcoder VSD Extended SDP Control 1
ShortName:	VSC_EXT_SDP_CTL_1_B
Reset:	soft
Address:	62290h-62293h
Name:	Transcoder VSD Extended SDP Control 0
ShortName:	VSC_EXT_SDP_CTL_0_C
Reset:	soft
Address:	62294h-62297h
Name:	Transcoder VSD Extended SDP Control 1
ShortName:	VSC_EXT_SDP_CTL_1_C
Reset:	soft
Address:	63290h-63293h
Name:	Transcoder VSD Extended SDP Control 0
ShortName:	VSC_EXT_SDP_CTL_0_D
Reset:	soft

Address:	63294h-63297h
Name:	Transcoder VSD Extended SDP Control 1
ShortName:	VSC_EXT_SDP_CTL_1_D
Reset:	soft

The VSC_EXT_VESA SDP allows a DP Source device to send video stream-related metadata aligned with the stream. A single VSC_EXT SDP is composed of four header bytes and 32 payload bytes. The VSC_EXT_VESA SDP maybe chained. Chaining framework enables a flexible metadata transportation framework to allow the transport of variable bytes of payload using a single VSC_EXT_VESA.

For transmitting frame synchronous metadata beyond 1KB, software must alternate between Buffer0 and Buffer1.

Metadata must be programmed in multiple of 32 bytes (8 dwords).

DWord	Bit	Description
0	31	**VSC extension SDP metadata enable** Access: R/W **NOTE:** This field is ignored on the register instance VSC_EXT_SDP_CTL_1. Value: 0b — Name: Disable Value: 1b — Name: Enable
	30:25	**Reserved** Access: RO Format: MBZ
	24	**Buffer Empty** Access: RO Description: This field is set by hardware when buffer is empty and reset when buffer has metadata to be sent over the link. This field is read by software (or DSB) to know when it can start writing to the buffer (buffer reuse cases included). SW needs to check "buffer clear status" status bit in this register for re-transmission use cases. Value: 1b — Name: buffer empty **[Default]** Value: 0b — Name: buffer not empty
	23:17	**Reserved** Access: RO Format: MBZ

	16	**Buffer Ready** Access: Write/Read Status This field is set by software (or DSB) to indicate that the buffer is ready for hardware use. Hardware clears this field after the buffer processing is complete. SW can also clear this bit. Both SW clear and SW set will have higher priority over HW clear. **Value** / **Name** 1b: Ready For HW Use 0b: Not ready for HW Use
	15	**Buffer Clear Status** Access: RO This field is set and reset by hardware. **Value** / **Name** / **Description** 1b: buffer is clear **[Default]**: Buffer is clear, and software can write the new HDR metadata 0b: buffer not empty: Buffer's contents are valid and software cannot update the buffer.
	14	**Index Auto Increment** Access: R/W This field controls the index auto increment.
	13:8	**Reserved** Access: RO Format: MBZ
	7:0	**Index Value** Access: R/W This field indicates the data location to be accessed through the data register. This value can be automatically incremented by a write to the data register if the index auto increment bit (14) is set. When automatically incrementing, the current automatically calculated index value can be read here, and the index will roll over to 0 after reaching the end of the allowed range. 8-bit index supports up to 1KB. Examples: 00h =Dword at location 0 FFh = Dword at location 255

VSC_EXT_SDP_DATA

VSC_EXT_SDP_DATA	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	60298h-6029Bh
Name:	Transcoder VSD Extended SDP DATA 0
ShortName:	VSC_EXT_SDP_DATA_0_A
Reset:	soft
Address:	6029Ch-6029Fh
Name:	Transcoder VSD Extended SDP DATA 1
ShortName:	VSC_EXT_SDP_DATA_1_A
Reset:	soft
Address:	61298h-6129Bh
Name:	Transcoder VSD Extended SDP DATA 0
ShortName:	VSC_EXT_SDP_DATA_0_B
Reset:	soft
Address:	6129Ch-6129Fh
Name:	Transcoder VSD Extended SDP DATA 1
ShortName:	VSC_EXT_SDP_DATA_1_B
Reset:	soft
Address:	62298h-6229Bh
Name:	Transcoder VSD Extended SDP DATA 0
ShortName:	VSC_EXT_SDP_DATA_0_C
Reset:	soft
Address:	6229Ch-6229Fh
Name:	Transcoder VSD Extended SDP DATA 1
ShortName:	VSC_EXT_SDP_DATA_1_C
Reset:	soft
Address:	63298h-6329Bh
Name:	Transcoder VSD Extended SDP DATA 0
ShortName:	VSC_EXT_SDP_DATA_0_D
Reset:	soft

Address:	6329Ch-6329Fh
Name:	Transcoder VSD Extended SDP DATA 1
ShortName:	VSC_EXT_SDP_DATA_1_D
Reset:	soft

DWord	Bit	Description
0	31:0	**Data** Access: R/W This field specifies the data for the index specified in VSC EXT SDP CTL register. Index [0-31] allows up to 1KB data. This register must be written only as a full 32 bit dword. Byte or word writes are not supported. This field can be read back only when "VSC extension SDP metadata enable" field in VSC_EXT_SDP_CTL is deasserted.

VSC_EXT_SDP_HEADER

VSC_EXT_SDP_HEADER

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6028Ch-6028Fh
Name:	Transcoder VSD Extended SDP Header
ShortName:	VSC_EXT_SDP_HEADER_A
Reset:	soft
Address:	6128Ch-6128Fh
Name:	Transcoder VSD Extended SDP Header
ShortName:	VSC_EXT_SDP_HEADER_B
Reset:	soft
Address:	6228Ch-6228Fh
Name:	Transcoder VSD Extended SDP Header
ShortName:	VSC_EXT_SDP_HEADER_C
Reset:	soft
Address:	6328Ch-6328Fh
Name:	Transcoder VSD Extended SDP Header
ShortName:	VSC_EXT_SDP_HEADER_D
Reset:	soft

DWord	Bit	Description
0	31:29	**Reserved** Access: RO Format: MBZ
	28:24	**Packet sequence** Access: R/W Range is from 0 to 31. Shall be cleared to 0 on the first SDP of a new VSC_EXT packet sequence. When bit 6 of HB2 is set to 1, this field shall increment by 1 on each subsequent chained packet. This counter rolls over to 0 when it exceeds 31.
	23	**Middle Of Chaining** Access: R/W This bit specifies if there are any chained packets to follow. This bit has to be set if block mode(VSC_EXT_SDP_CONF[block mode]) is set. 0b – No chained packets to follow 1b – Chained packet(s) to follow.

VSC_EXT_SDP_HEADER

	22	**Variable Packet Sequence Number** Access: R/W This bit specifies how the packed sequence field is used. 0b: Packet Sequence Field is fixed 1b: Packet Sequence field is incremented with chained packets
	21:18	**VSC EXT VESA SDP Framework Ver 1** Access: R/W Specifies the VSC EXT VESA SDP Framework Version, to be left at default '0'.
	17:16	**VSC EXT VESA SDP Framework Ver 0** Access: R/W Specifies the VSC EXT VESA SDP Framework Version, to be left at default '0'.
	15:8	**SDP Type** Access: R/W Specifies the Secondary Data Packet type. 20h: VESA **[Default]** 21h: CEA
	7:0	**SDP ID** Access: R/W Specifies the Secondary Data Packet ID. Specific to stream (usually 00h).

VS Invocation Counter

VS_INVOCATION_COUNT - VS Invocation Counter	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV
Address:	02320h-02327h
Name:	VS Invocation Counter
ShortName:	VS_INVOCATION_COUNT_RCSUNIT_BE_GEOMETRY
Address:	18320h-18327h
Name:	VS Invocation Counter
ShortName:	VS_INVOCATION_COUNT_POCSUNIT_BE_GEOMETRY

This register stores the value of the vertex count shaded by VS. This register is part of the context save and restore.

DWord	Bit	Description
0..1	63:32	**VS Invocation Count Report UDW** Access: R/W Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)
	31:0	**VS Invocation Count Report LDW** Access: R/W Number of vertices that are dispatched as threads by the VS stage. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)

VS Invocation Counter per Slice

VS_INVOCATION_COUNT_SLICE - VS Invocation Counter per Slice

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	64
_Custom_GTIReset:	DEV

Address:	06580h-06587h
Name:	VS Invocation Counter per Slice
ShortName:	VS_INVOCATION_COUNT_SLICE_SVGUNIT

Address:	17580h-17587h
Name:	VS Invocation Counter per Slice
ShortName:	VS_INVOCATION_COUNT_SLICE_SVGRUNIT

This register stores the value of the vertex count shaded by VS in a Slice. The value is only cleared by a write by SW.
HW will maintain a separate count which is reset for purposes of sending the value to the accumulated statistics count.

DWord	Bit	Description
0	63:32	**VS Invocation Count Report UDW in Slice** Access: R/W Number of vertices that are dispatched as threads by the VS stage within the slice. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)
	31:0	**VS Invocation Count Report LDW in Slice** Access: R/W Number of vertices that are dispatched as threads by the VS stage within the slice. Updated only when **Statistics Enable** is set in VS_STATE (see the Vertex Shader Chapter in the 3D Volume.)

VSR_PUSH_CONSTANT_BASE

VSR_PUSH_CONSTANT_BASE - VSR_PUSH_CONSTANT_BASE

Register Space:	MMIO: 0/2/0
Size (in bits):	32
Address:	0E518h
Name:	VSR_PUSH_CONSTANT_BASE
ShortName:	VSR_PUSH_CONSTANT_BASE

DWord	Bit	Description
0	31:17	**Reserved** Access: RO Format: MBZ
	16:6	**VSR PUSH CONSTANT BASE** Default Value: 200h Access: R/W **Description** This is an 64 Byte aligned offset in to the URB indicating the base of the push constant allocation space for the push constant allocation space for VSR unit. The offset and size of the VSR allocation is relative to this base address.
	5:0	**Reserved** Access: RO Format: MBZ

VTd Status

VTD_STATUS_0_2_0_PCI - VTd Status		
Register Space:	PCI: 0/2/0	
Size (in bits):	8	
Address:	0006Ch	
This register contains indicator bits for Graphics VTd mode.		
DWord	**Bit**	**Description**
0	7:1	**Reserved** Access: RO Format: MBZ
	0	**GFX VTd Active** Default Value: 0b Access: R/W _Custom_GTIReset: BUS Reflects GFX VTd Mode is active. 1 - if active, 0 if inactive. Acts as R/W register only during Punit restore - when iommu freeze bit is set. RO otherwise

Wait For Event and Display Flip Flags Register

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	022D0h-022D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_RCSUNIT_DISP

Address:	222D0h-222D3h
Name:	Wait For Event and Display Flip Flags Register
ShortName:	SYNC_FLIP_STATUS_BCSUNIT_DISP

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.

DWord	Bit	Description
0	31	**Reserved** Access: RO Format: MBZ
	30	**Display Plane 1 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 1 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	29	**Display Plane 1 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 1 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

28	**Display Plane 4 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 4 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
27	**Reserved** Access: RO Format: MBZ
26	**Display Plane 2 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 2 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
25	**Display Plane 2 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
24	**Display Plane 5 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
23	**Display Plane 1 Asynchronous Performance Flip Pending Wait Enable** Source: RenderCS Access: R/W

	Format:	Enable

This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

22 **Display Plane 1 Asynchronous Flip Pending Wait Enable**

Access:	R/W
Format:	Enable

This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

21 **Display Plane 1 Synchronous Flip Pending Wait Enable**

Access:	R/W
Format:	Enable

This field enables a wait for the duration of a Display Plane 1 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

20 **Display Plane 4 Synchronous Flip Pending Wait Enable**

Access:	R/W
Format:	Enable

This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

19 **Reserved**

Access:	RO
Format:	MBZ

18 **Display Pipe A Scan Line Wait Enable**

Access:	R/W
Format:	Enable

This field enables a wait while a Display Pipe A Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe A Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.

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	17	**Display Pipe A Vertical Blank Wait Enable** Access: R/W Format: Enable This field enables a wait until the next Display Pipe A Vertical Blank event occurs. This event is defined as the start of the next Display Pipe A vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	16	**Reserved** Access: RO Format: MBZ
	15	**Display Plane 2 Asynchronous Performance Flip Pending Wait Enable** Source: RenderCS Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 2 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	13	**Display Plane 2 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 2 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	12	**Display Plane 5 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front

SYNC_FLIP_STATUS - Wait For Event and Display Flip Flags Register

		buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	11	**Reserved** Access: RO Format: MBZ
	10	**Display Pipe B Scan Line Wait Enable** Access: R/W Format: Enable This field enables a wait while a Display Pipe B Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe B Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	9	**Display Pipe B Vertical Blank Wait Enable** Access: R/W Format: Enable This field enables a wait until the next Display Pipe B Vertical Blank event occurs. This event is defined as the start of the next Display Pipe B vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	8:0	**Reserved** Access: RO Format: MBZ

Wait For Event and Display Flip Flags Register 1

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	022D4h-022D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_RCSUNIT_DISP

Address:	222D4h-222D7h
Name:	Wait For Event and Display Flip Flags Register 1
ShortName:	SYNC_FLIP_STATUS_1_BCSUNIT_DISP

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ
	26	**Display Plane 12 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 12 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

24	**Display Plane 11 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
23	**Display Plane 11 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
22	**Display Plane 10 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
21	**Display Plane 10 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
20	**Display Plane 9 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

19	**Display Plane 9 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
18	**Display Plane 8 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
17	**Display Plane 8 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
16	**Display Plane 7 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
15	**Display Plane 7 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

14	**Display Pipe C Scan Line Event Pending** Access: R/W Format: Enable This field indicates scan line event operation is pending from Display Pipe C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.
13	**Display Pipe B Scan Line Event Pending** Access: R/W Format: Enable This field indicates scan line event operation is pending from Display Pipe B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane 3.
12	**Display Pipe A Scan Line Event Pending** Access: R/W Format: Enable This field indicates scan line event operation is pending from Display Pipe A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane 1.
11	**Reserved** Access: RO Format: MBZ
10	**Display Plane 3 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
9	**Display Plane 3 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

8	**Display Plane 6 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
7	**Display Plane 3 Asynchronous Performance Flip Pending Wait Enable** Source: RenderCS Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
6	**Display Plane 3 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 3 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
5	**Display Plane 3 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
4	**Display Plane 6 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

		Pending Condition in the Device Programming Interface chapter of MI Functions.
	3	**Reserved** Access: RO Format: MBZ
	2	**Display Pipe C Scan Line Wait Enable** Access: R/W Format: Enable This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.
	1	**Display Pipe C Vertical Blank Wait Enable** Access: R/W Format: Enable This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	0	**Reserved** Access: RO Format: MBZ

Wait For Event and Display Flip Flags Register 2

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	022ECh-022EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_RCSUNIT_DISP

Address:	222ECh-222EFh
Name:	Wait For Event and Display Flip Flags Register 2
ShortName:	SYNC_FLIP_STATUS_2_BCSUNIT_DISP

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.

DWord	Bit	Description
0	31:27	**Reserved** Access: RO Format: MBZ
	26	**Display Plane 12 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 12 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

24	**Display Plane 12 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 12 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
23	**Display Plane 11 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
22	**Display Plane 11 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
21	**Display Plane 11 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
20	**Display Plane 10 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

19	**Display Plane 10 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
18	**Display Plane 10 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
17	**Display Plane 9 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
16	**Display Plane 9 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
15	**Display Plane 9 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

14	**Display Plane 8 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
13	**Display Plane 8 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
12	**Display Plane 8 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
11	**Display Plane 7 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
10	**Display Plane 7 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

	9	**Display Plane 7 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 6 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	7	**Display Plane 6 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 6 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 5 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2

4	**Display Plane 5 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
3	**Display Plane 5 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 5 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
2	**Display Plane 4 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
1	**Display Plane 4 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
0	**Display Plane 4 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_2 - Wait For Event and Display Flip Flags Register 2		

Wait For Event and Display Flip Flags Register 3

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	022B8h-022BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_RCSUNIT_DISP

Address:	222B8h-222BBh
Name:	SYNC_FLIP_STATUS_3
ShortName:	SYNC_FLIP_STATUS_3_BCSUNIT_DISP

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**Display Plane 18 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	28	**Display Plane 18 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

	27	**Display Plane 18 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	26	**Display Plane 18 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 18 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 18 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 17 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 17 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

22	**Display Plane 17 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
21	**Display Plane 17 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
20	**Display Plane 17 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 17 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
19	**Display Plane 16 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 1616 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
18	**Display Plane 16 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

	17	**Display Plane 16 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 16 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 16 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 16 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 15 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	13	**Display Plane 15 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

12	**Display Plane 15 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
11	**Display Plane 15 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
10	**Display Plane 15 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 15 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
9	**Display Plane 14 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 4 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
8	**Display Plane 14 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

	7	**Display Plane 14 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 14 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 14 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 14 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 13 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 13 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_3 - Wait For Event and Display Flip Flags Register 3

	2	**Display Plane 13 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 13 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 13 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 13 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

Wait For Event and Display Flip Flags Register 4

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	022C0h-022C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_RCSUNIT_DISP

Address:	222C0h-222C3h
Name:	SYNC_FLIP_STATUS_4
ShortName:	SYNC_FLIP_STATUS_4_BCSUNIT_DISP

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**Display Plane 24 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	28	**Display Plane 24 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

27	**Display Plane 24 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
26	**Display Plane 24 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
25	**Display Plane 24 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 24 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
24	**Display Plane 23 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
23	**Display Plane 23 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

22	**Display Plane 23 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
21	**Display Plane 23 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
20	**Display Plane 23 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 23 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
19	**Display Plane 22 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
18	**Display Plane 22 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

17	**Display Plane 22 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
16	**Display Plane 22 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
15	**Display Plane 22 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 22 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
14	**Display Plane 21 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
13	**Display Plane 21 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

	12	**Display Plane 21 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	11	**Display Plane 21 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	10	**Display Plane 21 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 21 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	9	**Display Plane 20 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 20 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

7	**Display Plane 20 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
6	**Display Plane 20 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
5	**Display Plane 20 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 20 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
4	**Display Plane 19 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
3	**Display Plane 19 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_4 - Wait For Event and Display Flip Flags Register 4

	2	**Display Plane 19 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 19 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 19 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 19 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

Wait For Event and Display Flip Flags Register 5

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	022C4h-022C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_RCSUNIT_DISP

Address:	222C4h-222C7h
Name:	SYNC_FLIP_STATUS_5
ShortName:	SYNC_FLIP_STATUS_5_BCSUNIT_DISP

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.

DWord	Bit	Description
0	31:30	**Reserved** Access: RO Format: MBZ
	29	**Display Plane 30 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	28	**Display Plane 30 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

	27	**Display Plane 30 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	26	**Display Plane 30 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	25	**Display Plane 30 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 30 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	24	**Display Plane 29 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	23	**Display Plane 29 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

22	**Display Plane 29 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
21	**Display Plane 29 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
20	**Display Plane 29 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 29 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
19	**Display Plane 28 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
18	**Display Plane 28 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

	17	**Display Plane 28 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	16	**Display Plane 28 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	15	**Display Plane 28 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 28 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	14	**Display Plane 27 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	13	**Display Plane 27 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

12	**Display Plane 27 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
11	**Display Plane 27 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
10	**Display Plane 27 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 27 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
9	**Display Plane 26 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
8	**Display Plane 26 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

	7	**Display Plane 26 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 26 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 26 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 26 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 25 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 25 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_5 - Wait For Event and Display Flip Flags Register 5

	2	**Display Plane 25 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 25 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 25 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 25 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

Wait For Event and Display Flip Flags Register 6

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV

Address:	021F8h-021FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_RCSUNIT_DISP

Address:	221F8h-221FBh
Name:	SYNC_FLIP_STATUS_6
ShortName:	SYNC_FLIP_STATUS_6_BCSUNIT_DISP

This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.

Programming Notes

Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.

VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.

DWord	Bit	Description
0	31:19	**Reserved** Access: RO Format: MBZ
	18	**Display Pipe D Scan Line Event Pending** Access: R/W Format: Enable This field indicates scan line event operation is pending from Display Pipe D. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Pipe D and gets reset on scan line event completion for Display Plane-C.
	17	**Display Pipe D Scan Line Wait Enable** Access: R/W Format: Enable This field enables a wait while a Display Pipe D Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe D Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

	16	**Display Pipe D Vertical Blank Wait Enable** Access: R/W Format: Enable This field enables a wait until the next Display Pipe D Vertical Blank event occurs. This event is defined as the start of the next Display Pipe D vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).
	15:10	**Reserved** Access: RO Format: MBZ
	9	**Display Plane 32 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	8	**Display Plane 32 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	7	**Display Plane 32 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	6	**Display Plane 32 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

		Pending Condition in the Device Programming Interface chapter of MI Functions.
	5	**Display Plane 32 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 32 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
	4	**Display Plane 31 Asynchronous Performance Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	3	**Display Plane 31 Asynchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	2	**Display Plane 31 Asynchronous Display Flip Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions.
	1	**Display Plane 31 Synchronous Flip Pending Wait Enable** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip

SYNC_FLIP_STATUS_6 - Wait For Event and Display Flip Flags Register 6

		Pending Condition in the Device Programming Interface chapter of MI Functions.
	0	**Display Plane 31 Synchronous Flip Display Pending** Access: R/W Format: Enable This field enables a wait for the duration of a Display Plane 31 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.

Watchdog Counter

PR_CTR - Watchdog Counter	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02190h-02193h
Name:	Watchdog Counter
ShortName:	PR_CTR_RCSUNIT_CTX
Address:	22190h-22193h
Name:	Watchdog Counter
ShortName:	PR_CTR_BCSUNIT_CTX
Address:	1C0190h-1C0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT0_CTX
Address:	1C4190h-1C4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT1_CTX
Address:	1C8190h-1C8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT0_CTX
Address:	1D0190h-1D0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT2_CTX
Address:	1D4190h-1D4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT3_CTX
Address:	1D8190h-1D8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT1_CTX
Address:	1E0190h-1E0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT4_CTX
Address:	1E4190h-1E4193h
Name:	Watchdog Counter

PR_CTR - Watchdog Counter

ShortName:	PR_CTR_VCSUNIT5_CTX
Address:	1E8190h-1E8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT2_CTX
Address:	1F0190h-1F0193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT6_CTX
Address:	1F4190h-1F4193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VCSUNIT7_CTX
Address:	1F8190h-1F8193h
Name:	Watchdog Counter
ShortName:	PR_CTR_VECSUNIT3_CTX
Address:	1A190h-1A193h
Name:	Watchdog Counter
ShortName:	PR_CTR_CCSUNIT0_CTX
Address:	1C190h-1C193h
Name:	Watchdog Counter
ShortName:	PR_CTR_CCSUNIT1_CTX
Address:	1E190h-1E193h
Name:	Watchdog Counter
ShortName:	PR_CTR_CCSUNIT2_CTX
Address:	26190h-26193h
Name:	Watchdog Counter
ShortName:	PR_CTR_CCSUNIT3_CTX

DWord	Bit	Description
0	31:0	**Counter Value** Access: RO Format: U32 This register reflects the render watchdog counter value itself. It cannot be written to.

Watchdog Counter Control

PR_CTR_CTL - Watchdog Counter Control	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	02178h-0217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_RCSUNIT_CTX
Address:	22178h-2217Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_BCSUNIT_CTX
Address:	1C0178h-1C017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT0_CTX
Address:	1C4178h-1C417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT1_CTX
Address:	1C8178h-1C817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT0_CTX
Address:	1D0178h-1D017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT2_CTX
Address:	1D4178h-1D417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT3_CTX
Address:	1D8178h-1D817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT1_CTX
Address:	1E0178h-1E017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT4_CTX
Address:	1E4178h-1E417Bh
Name:	Watchdog Counter Control

PR_CTR_CTL - Watchdog Counter Control

ShortName:	PR_CTR_CTL_VCSUNIT5_CTX
Address:	1E8178h-1E817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT2_CTX
Address:	1F0178h-1F017Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT6_CTX
Address:	1F4178h-1F417Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VCSUNIT7_CTX
Address:	1F8178h-1F817Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_VECSUNIT3_CTX
Address:	1A178h-1A17Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_CCSUNIT0_CTX
Address:	1C178h-1C17Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_CCSUNIT1_CTX
Address:	1E178h-1E17Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_CCSUNIT2_CTX
Address:	26178h-2617Bh
Name:	Watchdog Counter Control
ShortName:	PR_CTR_CTL_CCSUNIT3_CTX

Programming Notes

Ring Buffer Mode of scheduling SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. Watch Dog counter once enabled doesnt stop unless it is explicitly disabled. SW must explicitly reset the watch dog counter by disabling it before enabling the watch dog counter for a new command sequence. Preemption could happen in a command sequence prior to watch dog counter getting disabled resulting in watch dog counter enabled following preemption. SW must explicitly take care of disabling the watch dog counter as part of the preemption sequence. Execution List Mode of Scheduling: SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. On a context switch Watch Dog Counter Control and Watch dog Threshold are context save restored, whereas watch dog counter gets reset to 0x0 and remains disabled until it gets enabled by another context during context restore or due to explicit programming. Watch dog counter value doesnt get accumulated across multiple submissions of a given context.

PR_CTR_CTL - Watchdog Counter Control

This register functionality is not supported and must not be programmed for Position command streamer.

DWord	Bit	Description
0	31	**Count Select** Access: R/W Format: U1 **Value / Name / Description** 0h / **[Default]** / Use eight times the time stamp base unit to increment the watch dog count. The granularity of the time stamp base unit is defined in the Time Stamp Bases subsection in Power Management chapter. 1h / / Use the fixed function clock (csclk) to increment the watchdog count
	30:0	**Counter Logic Op** Default Value: 1h Access: R/W This field specifies the action to be taken by the clock counter to generate interrupts. Writing a Zero value to this register starts the counting. Writing a Value of 0000_0001 to this counter stops the counter.

Watchdog Counter Threshold

PR_CTR_THRSH - Watchdog Counter Threshold	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0217Ch-0217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_RCSUNIT_CTX
Address:	2217Ch-2217Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_BCSUNIT_CTX
Address:	1C017Ch-1C017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT0_CTX
Address:	1C417Ch-1C417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT1_CTX
Address:	1C817Ch-1C817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT0_CTX
Address:	1D017Ch-1D017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT2_CTX
Address:	1D417Ch-1D417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT3_CTX
Address:	1D817Ch-1D817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT1_CTX
Address:	1E017Ch-1E017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT4_CTX
Address:	1E417Ch-1E417Fh
Name:	Watchdog Counter Threshold

PR_CTR_THRSH - Watchdog Counter Threshold

ShortName:	PR_CTR_THRSH_VCSUNIT5_CTX
Address:	1E817Ch-1E817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT2_CTX
Address:	1F017Ch-1F017Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT6_CTX
Address:	1F417Ch-1F417Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VCSUNIT7_CTX
Address:	1F817Ch-1F817Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_VECSUNIT3_CTX
Address:	1A17Ch-1A17Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_CCSUNIT0_CTX
Address:	1C17Ch-1C17Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_CCSUNIT1_CTX
Address:	1E17Ch-1E17Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_CCSUNIT2_CTX
Address:	2617Ch-2617Fh
Name:	Watchdog Counter Threshold
ShortName:	PR_CTR_THRSH_CCSUNIT3_CTX

Programming Notes

This register functionality is not supported and must not be programmed for Position command streamer.

This register must never be programmed with zero. This will cause the watchdog counter to exceed and not allow the engine to go into IDLE state.

DWord	Bit	Description
0	31:0	**Counter Logic Threshold** Default Value: 00145855h Access: R/W Format: U32 This field specifies the threshold that the hardware checks against for the value of the render clock counter before generating an interrupt. The counter in hardware generates an interrupt

PR_CTR_THRSH - Watchdog Counter Threshold		
		when the threshold is reached, rolls over and starts counting again. The interrupt generated is the "Media Hang Notify" interrupt since this watchdog timer is intended primarily to remedy VLD hangs on the main pipeline.

WD_FRAME_STATUS

WD_FRAME_STATUS

Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	6E568h-6E56Bh
Name:	WD0 Frame Status
ShortName:	WD_FRAME_STATUS_0
Reset:	soft
Address:	6ED68h-6ED6Bh
Name:	WD1 Frame Status
ShortName:	WD_FRAME_STATUS_1
Reset:	soft

DWord	Bit	Description
0	31	**Frame Complete** Access: R/WC This field is a sticky bit set when WD fully completes a frame. Clear by writing a 1 to it.
	30:27	**Reserved** Access: RO Format: MBZ
	26:24	**WD State** Access: RO This field indicates the live state of WD capture. Value / Name / Description: 000b / IDLE / Reset state 001b / CAPSTART / Start timing generator for normal capture 010b / FRAME_START / Send framestart to display pipe 011b / CAPACTIVE / Capturing data 100b / TG_DONE / Completed writing pixels. Waiting for frame completion. 101b / WDX_DONE / Fully completed frame. Waiting to start next frame. 110b / QUICK_CAP / Quick capture entry
	23	**Reserved** Access: RO
	22:21	**Reserved** Access: RO

WD_FRAME_STATUS			
		Format:	MBZ
	20	**Reserved**	
		Access:	RO
	19:0	**Reserved**	
		Access:	RO
		Format:	MBZ

WD_IIR

WD_IIR

Register Space:	MMIO: 0/2/0
Access:	R/WC
Size (in bits):	32
Address:	6E564h-6E567h
Name:	WD0 Interrupt Identity
ShortName:	WD_IIR_0
Reset:	soft
Address:	6ED64h-6ED67h
Name:	WD1 Interrupt Identity
ShortName:	WD_IIR_1
Reset:	soft

See the WD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Interrupt Identity Bits** Access: R/WC This field holds the persistent values of the WD interrupt bits which are unmasked by the WD_IMR. Bits set in this register will propagate to the WD interrupt in the Display Engine Miscellaneous Interrupts. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name
0b	Condition Not Detected
1b	Condition Detected

WD_IMR

WD_IMR	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	6E560h-6E563h
Name:	WD0 Interrupt Mask
ShortName:	WD_IMR_0
Reset:	soft
Address:	6ED60h-6ED63h
Name:	WD1 Interrupt Mask
ShortName:	WD_IMR_1
Reset:	soft

See the WD interrupt bit definition to find the source event for each interrupt bit.

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:0	**Interrupt Mask Bits** Access: R/W This field contains a bit mask which selects which WD events are reported in the WD_IIR. Value / Name: 0b – Not Masked 1b – Masked 0000FFFFh – All interrupts masked **[Default]**

WD_PERF_CNT

WD_PERF_CNT		
Register Space:	MMIO: 0/2/0	
Access:	Write/Read Status	
Size (in bits):	32	
Address:	6E55Ch-6E55Fh	
Name:	WD0 Performance Counter	
ShortName:	WD_PERF_CNT_0	
Reset:	soft	
Address:	6ED5Ch-6ED5Fh	
Name:	WD1 Performance Counter	
ShortName:	WD_PERF_CNT_1	
Reset:	soft	

DWord	Bit	Description
0	31:24	**Reserved** Access: RO Format: MBZ
	23:0	**WD Perf Cnt** Access: Write/Read Status This field increments every millisecond while capturing. It does not count the time after capture is completed and waiting for the next capsync. Writes to this register will set the count to the written value, then it will increment from that value onwards.

WD_STRIDE

WD_STRIDE	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of capture sync or transcoder not enabled
Address:	6E510h-6E513h
Name:	WD0 Stride
ShortName:	WD_STRIDE_0
Reset:	soft
Address:	6ED10h-6ED13h
Name:	WD1 Stride
ShortName:	WD_STRIDE_1
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:6	**WD Stride** Access: Double Buffered This field specifies the stride bits 15:6.This value is used to determine the line to line increment for the capture data writes. This field is programmed in units of 64 bytes. **Programming Notes** The stride has to be at least large enough to encompass all the pixels in a line, and rounded up to 64 byte alignment. Stride bytes >= CEILING[(Horizontal Active * WD Color Mode bytes per pixel) / 64] * 64 **Restriction** The stride is limited to a maximum of 32K bytes.
	5:0	**Reserved** Access: RO Format: MBZ

WD_SURF

WD_SURF

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of capture sync or transcoder not enabled

Address:	6E514h-6E517h
Name:	WD0 Surface Base Address
ShortName:	WD_SURF_0
Reset:	soft

Address:	6ED14h-6ED17h
Name:	WD1 Surface Base Address
ShortName:	WD_SURF_1
Reset:	soft

Writes to this register arm WD registers.

DWord	Bit	Description
0	31:12	**WD Surface Base Address** Access: Double Buffered Format: GraphicsAddress[31:12] This address specifies the surface base address bits 31:12. It is mapped to physical pages through the global GTT. **Programming Notes** The mapped pages must be located outside graphics data stolen memory. **Restriction** It must be at least 4KB aligned.It must use linear memory.
	11:0	**Reserved** Access: RO Format: MBZ

WD_TAIL_CFG

WD_TAIL_CFG

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to WD_SURF or WD not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of capture sync or transcoder not enabled; after armed

Address:	6E520h-6E523h
Name:	WD0 Tail Pointer Config
ShortName:	WD_TAIL_CFG_0
Reset:	soft

Address:	6ED20h-6ED23h
Name:	WD1 Tail Pointer Config
ShortName:	WD_TAIL_CFG_1
Reset:	soft

DWord	Bit	Description
0 If Delay < Period; first tail pointer is sent at the next multiple of Period, after the Delay. If Delay Period; first tail pointer is set at the Period. The tail pointer is also sent at the end of the frame. If Delay or Period are greater than the vertical size, only the tail pointer at the end of the frame is sent.	31:28	**Reserved** Access: RO Format: MBZ
	27:16	**Tail Initial Update Delay** Access: Double Buffered This field specifies the minimum number of scan lines that WD capture must wait for at the beginning of each frame before any tail pointer updates will be sent to media. This must be programmed smaller than the vertical active size.
	15:12	**Reserved** Access: RO Format: MBZ
	11:4	**Tail Update Period** Default Value: 01h 16 lines Access: Double Buffered This field specifies the number of scan lines that the WD capture will write back to memory before sending each tail pointer message to media. This field is programmed in multiples of 16 scan lines. **Restriction**

WD_TAIL_CFG		
		A value of 0 is not valid.
	3:0	**Reserved** Access: RO Format: MBZ

WD_TAIL_CFG2

WD_TAIL_CFG2	
Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferArmedBy:	Write to WD_SURF or WD not enabled
_Custom_Display_DoubleBufferUpdatePoint:	Start of capture sync or transcoder not enabled; after armed

Address:	6E52Ch-6E52Fh
Name:	WD0 Tail Pointer Config2
ShortName:	WD_TAIL_CFG2_0
Reset:	soft

Address:	6ED2Ch-6ED2Fh
Name:	WD1 Tail Pointer Config2
ShortName:	WD_TAIL_CFG2_1
Reset:	soft

DWord	Bit	Description
0	31:16	**Reserved** Access: RO Format: MBZ
	15:4	**Tail Pointer Offset** Access: Double Buffered This field is programmed in multiples of 16 scan lines.
	3:0	**Reserved** Access: RO Format: MBZ

WD_VFID

WD_VFID

Register Space:	MMIO: 0/2/0
Access:	Double Buffered
Size (in bits):	32
_Custom_Display_DoubleBufferUpdatePoint:	Start of capture sync or transcoder not enabled

Address:	6E518h-6E51Bh
Name:	WD0 VFID
ShortName:	WD_VFID_0
Reset:	soft

Address:	6ED18h-6ED1Bh
Name:	WD1 VFID
ShortName:	WD_VFID_1
Reset:	soft

DWord	Bit	Description
0	31:20	**Reserved** Access: RO Format: MBZ
	19:0	**VFID** Access: Double Buffered The Virtual Function ID or PASID assigned to this WD. **Restriction** This value must be set to 0 if LMTT is not enabled.

WIDI Session 0

WIDI_SESSION_0 - WIDI Session 0		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00ED0h	
DWord	**Bit**	**Description**
0	31:0	**Static Data** Default Value: 0b Access: R/W Scratch registers provided for Display/GUC WIDI Session access

WIDI Session 1

WIDI_SESSION_1 - WIDI Session 1		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00ED4h	
DWord	**Bit**	**Description**
0	31:0	**Static Data** Default Value: 0b Access: R/W Scratch registers provided for Display/GUC WIDI Session access

WIDI Session 2

WIDI_SESSION_2 - WIDI Session 2		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00ED8h	
DWord	**Bit**	**Description**
0	31:0	**Static Data** Default Value: 0b Access: R/W Scratch registers provided for Display/GUC WIDI Session access

WIDI Session 3

WIDI_SESSION_3 - WIDI Session 3		
Register Space:	MMIO: 0/2/0	
Size (in bits):	32	
_Custom_GTIReset:	BUS	
Address:	00EDCh	
DWord	**Bit**	**Description**
0	31:0	**Static Data** Default Value: 0b Access: R/W Scratch registers provided for Display/GUC WIDI Session access

WiDi VDEnc Stall counter

WIDI_VDENC_STALL_CNTR - WiDi VDEnc Stall counter	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	BUS
Address:	1C2D94h-1C2D97h
Name:	WiDi mode VDENC stall counter value
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG0
Address:	1C6D94h-1C6D97h
Name:	WiDi mode VDENC stall counter value
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG1
Address:	1D2D94h-1D2D97h
Name:	WiDi mode VDENC stall counter value
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG2
Address:	1D6D94h-1D6D97h
Name:	WiDi mode VDENC stall counter value
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG3
Address:	1E2D94h-1E2D97h
Name:	WiDi mode VDENC stall counter value
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG4
Address:	1E6D94h-1E6D97h
Name:	WiDi mode VDENC stall counter value
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG5
Address:	1F2D94h-1F2D97h
Name:	WiDi mode VDENC stall counter value
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG6
Address:	1F6D94h-1F6D97h
Name:	WiDi mode VDENC stall counter value
ShortName:	WIDI_VDENC_STALL_CNTR_VDENC_REG7

This register has stall counter for the VDENC. In an ideal case, this value should be zero.

DWord	Bit	Description
0	31:0	**WiDi Stall clock count** Access: RO

Window Hardware Generated Clear Value

WMHWCLRVAL - Window Hardware Generated Clear Value	
Register Space:	MMIO: 0/2/0
Access:	RO
Size (in bits):	32
Address:	05524h

DWord	Bit	Description
0	31:0	**WM HW Generated Clear Value** Access: RO Format: MBZ This register stores HW generated Z clear value.

WM_LINETIME

WM_LINETIME	
Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45270h-45273h
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_A
Reset:	soft
Address:	45274h-45277h
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_B
Reset:	soft
Address:	45278h-4527Bh
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_C
Reset:	soft
Address:	4527Ch-4527Fh
Name:	Pipe Watermark Line Time
ShortName:	WM_LINETIME_D
Reset:	soft

DWord	Bit	Description
0	31:9	**Reserved** Access: RO Format: MBZ
	8:0	**Line Time** Access: R/W This field specifies the line time for the current screen resolution in units of 0.125us. **Programming Notes** Line time in microseconds = Pipe horizontal total number of pixels / pixel rate in MHz. Multiply by 8 to get units of 0.125us and round to nearest integer.Program the smallest line time when using multiple refresh rates. **Restriction** The line time value must be programmed before enabling any display low power watermark.Maximum supported line time is 63.875us (111111111b).

WM_MISC

WM_MISC

Register Space:	MMIO: 0/2/0
Access:	R/W
Size (in bits):	32
Address:	45260h-45263h
Name:	Watermark Miscellaneous
ShortName:	WM_MISC
Reset:	soft

DWord	Bit	Description
0	31	**Reserved** Access: R/W Format: PBC
	30:28	**Reserved** Access: R/W
	27	**MIPI DBI Method** Access: R/W This field controls the behavior for the TTNF calculation for MIPI DBI. 0b – Calculated – TTNF calculated in active area and all 1s outside of active. TTVBI all 1s. 1b – Simple – TTNF all 0s in active area and all 1s outside of active. TTVBI all 1s.
	26:20	**Reserved** Access: R/W Format: PBC
	19:0	**Reserved** Access: RO Format: MBZ

Workload Partition Register

WPARID - Workload Partition Register	
Register Space:	MMIO: 0/2/0
Size (in bits):	32
_Custom_GTIReset:	DEV
Address:	0221Ch-0221Fh
Name:	Workload Partition ID
ShortName:	WPARID_RCSUNIT_CTX
Address:	2221Ch-2221Fh
Name:	Workload Partition ID
ShortName:	WPARID_BCSUNIT_CTX
Address:	1C021Ch-1C021Fh
Name:	Workload Partition ID
ShortName:	WPARID_VCSUNIT0_CTX
Address:	1C421Ch-1C421Fh
Name:	Workload Partition ID
ShortName:	WPARID_VCSUNIT1_CTX
Address:	1C821Ch-1C821Fh
Name:	Workload Partition ID
ShortName:	WPARID_VECSUNIT0_CTX
Address:	1D021Ch-1D021Fh
Name:	Workload Partition ID
ShortName:	WPARID_VCSUNIT2_CTX
Address:	1D421Ch-1D421Fh
Name:	Workload Partition ID
ShortName:	WPARID_VCSUNIT3_CTX
Address:	1D821Ch-1D821Fh
Name:	Workload Partition ID
ShortName:	WPARID_VECSUNIT1_CTX
Address:	1E021Ch-1E021Fh
Name:	Workload Partition ID
ShortName:	WPARID_VCSUNIT4_CTX

Address:	1E421Ch-1E421Fh
Name:	Workload Partition ID
ShortName:	WPARID_VCSUNIT5_CTX
Address:	1E821Ch-1E821Fh
Name:	Workload Partition ID
ShortName:	WPARID_VECSUNIT2_CTX
Address:	1F021Ch-1F021Fh
Name:	Workload Partition ID
ShortName:	WPARID_VCSUNIT6_CTX
Address:	1F421Ch-1F421Fh
Name:	Workload Partition ID
ShortName:	WPARID_VCSUNIT7_CTX
Address:	1F821Ch-1F821Fh
Name:	Workload Partition ID
ShortName:	WPARID_VECSUNIT3_CTX
Address:	1A21Ch-1A21Fh
Name:	Workload Partition ID
ShortName:	WPARID_CCSUNIT0_CTX
Address:	1C21Ch-1C21Fh
Name:	Workload Partition ID
ShortName:	WPARID_CCSUNIT1_CTX
Address:	1E21Ch-1E21Fh
Name:	Workload Partition ID
ShortName:	WPARID_CCSUNIT2_CTX
Address:	2621Ch-2621Fh
Name:	Workload Partition ID
ShortName:	WPARID_CCSUNIT3_CTX

In the new SW scheduling model a given applications workload is simultaneously submitted to multiple engines for concurrent execution. This is done by submitting the same workload through different contexts (LRCAs) to multiple engines. Since the same workload (batch buffer) gets executed by all the engines there is a need for mechanism to partition the workload among the concurrently executing contexts to avoid duplication and clobbering of workload execution. Due to various produce consume dependencies and for load balancing there is a need to support fine grain and dynamic workload partitioning. This is achieved by providing a Workload Partition ID (WPARID) to each of the context, this gets in the contexts LRCA and gets context save/restored. In case of static workload partitioning, WAPARID can be initialized to a unique value at the context creation time for each of the context. In case of dynamic workload balancing each context can load its WAPARID prior to a workload execution by acquiring it through atomics from a centralized location in memory.
WPARID can be referenced in MI commands to achieve a different variant of functional behavior based on its LRCA assigned "WPARID from which the command is getting executed. WPARID can be referenced in

COMPUTE_WALKER to execute a subset of the workload based on its LRCA assigned "WPARID from which the command is getting executed.
[MI_SET_PREDICATE]: Predication based on WPARID.
[MI_STORE_DATA_IMM, MI_LOAD_REGISTER_MEM, MI_STORE_REGISETR_MEM, MI_COPY_MEM_MEM, MI_ATOMIC, PIPE_COTROL]: Memory writes and reads are to an offset based on the WPARID from the memory address mentioned in the command.
[COMPUTE_WALKER]: Subset of workload gets executed based on the WAPRID value.
This is a non-privileged registers and context save/restored on a context switch.

DWord	Bit	Description
0	31:8	**Reserved** Access: RO Format: MBZ
	7:0	**Workload Partition ID** Default Value: 00h Access: R/W This field holds the workload partition ID value.